MAX25561

6 x 220mA, ASIL B LED Backlight Driver with Boost Controller

General Description

The MAX25561 is a 6-channel LED backlight driver with an integrated current-mode boost controller that operates over a switching frequency range of 400kHz to 2.2MHz and incorporates spread spectrum. Selectable phase-shifting of the output channels is included to reduce EMI. The MAX25561 provides up to 220mA per channel. The device is capable of operating down to very low battery voltages by virtue of a unique input voltage switching scheme.

Extensive diagnostics and an I^{2}C interface are included to assist with system ASIL B compliance.

The MAX25561 is available in a compact TQFN package and operates over the -40°C to +125°C temperature range.

Applications

- Automotive Instrument Clusters
- Automotive Central Information Displays
- Automotive Head-Up Displays

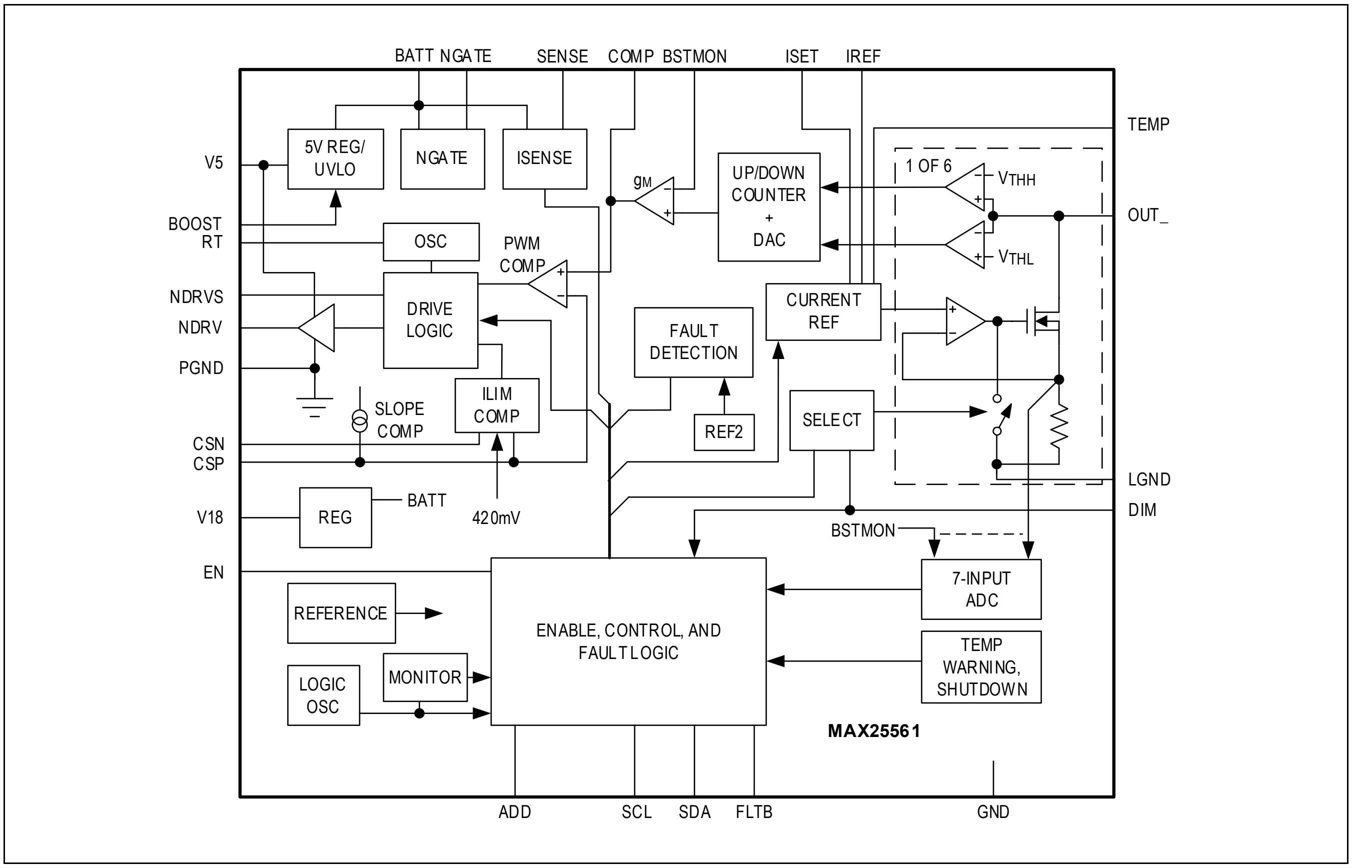
Benefits and Features

- Operates Down to 3V on Battery Input while Maintaining 5V Gate Drive
  - Wide Boost Duty-Cycle Range
- Boost or SEPIC Current-Mode DC-DC Controller
  - 400kHz to 2.2MHz Operating Frequency Range
  - Optional Spread Spectrum
  - Can Be Synchronized to an External Clock
- LED Current Sinks
  - Up to 220mA Output Current per String
  - Low OUT_ Regulation Voltage
  - Optional Phase-Shifting Between Channels
- 15000:1 Dimming Ratio at 200Hz
- External or Internal (I^{2}C) Dimming
- >15000:1 Dimming Ratio with Hybrid Dimming
- Integrated Charge-Pump to Drive Series nMOSFET
- Temperature Foldback Using External NTC Temperature Sensor
- Fast Startup Option without I^{2}C Intervention Using EN Pin Only
- FLTB Output Provides Diagnostic Information
  - Shorted or Open LEDs
  - Any OUT_ Pin Shorted to GND
  - IREF/RT Resistor Out of Range
  - Thermal Warning/Shutdown
  - Undervoltage/Overvoltage on Boost Output
  - Bandgap Out-of-Range/Internal Oscillator Failure
  - V18 Internal Supply out-of-Range
  - Input Overcurrent (Measured at Boost Input Using External Sense Resistor)
  - Input/Output PWM Comparison
  - Continuous Output Current Measurement and Current Mismatch (Shutdown/Flag)
- I^{2}C Interface with CRC
  - Readback of Measured DIM Pin Duty Cycle and Frequency
- Compact TQFN Package

***Ordering Information* appears at end of data sheet.**

19-101727; Rev 0; 10/23

Simplified Block Diagram



Absolute Maximum Ratings

BATT, BOOST, OUT1-6, BSTMON, EN to GND	-0.3V to +42V
SENSE to BATT	0.3V
FLTB, DIM, SDA, SCL to GND	-0.3V to +6V
PGND to GND	-0.3V to +0.3V
LGND1, 2 to GND	-0.3V to +0.3V
NGATE to GND	-0.3V to +42V
NGATE to BATT	6V
V18 to GND	-0.3V to +2.2V
TEMP, CSP, COMP, IREF, ISET, RT, ADD to GND	-0.3V to V18 + 0.3V
V5 to GND	-0.3V to +6V
NDRV, NDRVS to GND	-0.3V to V5 + 0.3V
NDRV Peak Current (<100ns)	3A
NDRV Continuous Current	100mA
OUT_ Continuous Current	250mA
Continuous Power Dissipation (Single Layer Board) (T_A = +70°C, derate 21.28mW/°C above +70°C)	1702mW
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 27.8mW/°C above +70°C)	2222mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T3255+6C
Outline Number	21-0140
Land Pattern Number	90-0603
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
BATT Operating Voltage Range	V_{BATT}		4.5		36	V
BATT Operating Voltage Range After Startup		Maximum duration 100ms	3		36	V
BATT Quiescent Supply Current	I_{BATT}	No switching		2.3	3	mA
BATT Shutdown Supply Current				4	10	µA
BATT Undervoltage Lockout Rising			4.1	4.25	4.35	V
BATT Undervoltage Lockout Falling			2.77	2.9	2.95	V
BATT Threshold for Low-Voltage Operation Mode, Falling	V_{BATT_LVF}		5.28	5.45	5.6	V
BATT Threshold for Low-Voltage Operation Mode, Rising	V_{BATT_LVR}		5.5	5.66	5.82	V
V18 REGULATOR						
V18 Output Voltage	V_{V18_ACC}	No load on V18	1.72	1.8	1.88	V
V18 Current Limit	I_{LIM_V18}	V_{V18} = 1V	50			mA
V18 Undervoltage Lockout	V_{V18_UVLO}	V18 voltage rising	1.6	1.65	1.7	V
V18 Undervoltage Hysteresis	$V_{V18\_UVLO\_HYS}$			150		mV
V18 Power-on-Reset Level		Design guidance		1.4		V
V18OOR Diagnostic Levels			-8		+8	%
V5 REGULATOR						
V5 Output Voltage	V_{V5}	V_{BATT} = 5.75V to 36V, I_{V5} = 10mA	4.8	5	5.2	V
V5 Dropout Voltage	V_{V5_DRP}	V_{BOOST} = 4.9V, I_{V5} = 5mA		0.18	0.3	V
V5 Undervoltage Lockout	V_{V5_UVLOR}	V5 voltage rising	3.75	3.9	4.05	V
	V_{V5_UVLOF}	V5 voltage falling	3.6	3.7	3.8	

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V5 Short-Circuit Current Limit	I_{V5_SC}	V5 shorted to GND	30			mA
V5 Overvoltage Threshold, Rising			5.6	5.75	5.85	V
V5 Overvoltage Threshold Hysteresis				100		mV
NGATE OUTPUT/INPUT CURRENT SENSING						
NGATE Output Voltage	V_{NGATE}	Above V_{BATT}, 3V < V_{BATT} < 33V, I_{NGATE} = 1µA	4.3	5.25	6.3	V
NGATE Source Current	I_{NG_SO}	V_{NGATE} = V_{BATT}	30	50		µA
NGATE Sink Current	I_{NG_SINK}	V_{NGATE} = 14V = V_{BATT}	6	10		mA
NGATE Output Voltage at High Input Voltage	V_{NGATE_HV}	Above V_{BATT}, V_{BATT} > 35.5V, I_{NGATE} = 1µA	-0.2		0	V
BATT HV Comparator Threshold	V_{LD_THR}	BATT voltage rising	33		36	V
BATT HV Comparator Hysteresis	V_{LD_HYS}			0.7		V
NGATE Start Delay	t_{NG_DEL}	Delay between NGATE charge-pump turning on and BSTMON rising		2	2.2	ms
BATT-SENSE Overcurrent Threshold	V_{BATT_SNS}		190	200	210	mV
SENSE Input Bias Current	I_{SNS}			10	16	µA
BATT-SENSE Overcurrent Turnoff Delay	t_{SD_SNS}			4		ms
RT OSCILLATOR						
Switching Frequency Range	f_{SW_RT}	Frequency dithering disabled	400		2200	kHz
Oscillator Frequency Accuracy		I_{RT} = 13.85µA (f_{SW} = 400kHz), I_{RT} = 76.1µA (f_{SW} = 2200kHz)	-10		+10	%
Boost Converter Maximum Duty Cycle, High Frequency		f_{SW} = 1.8MHz to 2.2MHz	89	92	95	%
Boost Converter Maximum Duty Cycle, Low Frequency		f_{SW} = 400kHz to 500kHz	94		98	%
Boost Minimum On-Time				60		ns
Frequency Dither, High Setting		SSL = 1		±6		%
Frequency Dither, Low Setting	SS	SSL = 1		±4		%
RT Output Voltage	V_{RT}	R_{RT} = 65kΩ or R_{RT} = 10kΩ	0.875	0.9	0.925	V
Sync Threshold	V_{RT_SYNC}	V_{RT} rising	0.77		0.84	V
Sync Frequency Duty Cycle	D_{SYNC}			50		%
Sync Frequency Range			400		2200	kHz
SLOPE COMPENSATION						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Slope Compensation Current Ramp Magnitude		Current ramp added to CS	42	50	58	µA
CURRENT-LIMIT COMPARATOR						
CSP Threshold Voltage	$V_{CSP-CSNL}$	bl_ilim = 1	275	300	325	mV
	$V_{CSP-CSN}$	bl_ilim = 0	380	410	440	
CSP Threshold Voltage During Low Voltage	V_{CSP_LV}	$V_{BATT} < V_{BATT\_LVF}$, V_{BATT} falling	560	600	640	mV
CSP Input Current	I_{CSP}	V_{EN} = 0V, V_{CSP} = 0.4V			1	µA
ERROR AMPLIFIER						
OUT_ Regulation High Threshold		$V_{OUT\_}$ falling	0.82	0.85	0.87	V
OUT_ Regulation Low Threshold		$V_{OUT\_}$ rising	0.55	0.58	0.61	V
Transconductance			410	630	890	µS
COMP Sink Current		V_{COMP} = 1V	270	380	500	µA
COMP Source Current		V_{COMP} = 1V	270	380	500	µA
MOSFET DRIVER						
NDRV On-Resistance, High Side		I_{NDRV} = 100mA		1.5	3	Ω
NDRV On-Resistance, Low Side		I_{NDRV} = -100mA		1.2	2	Ω
NDRV Rise Time		C_{NDRV} = 1nF		8		ns
NDRV Fall Time		C_{NDRV} = 1nF		8		ns
NDRVS Input Logic-Low	V_{IL_NDRVS}	V_{NDRVS} falling		2	2.4	V
NDRVS Input Logic-High	V_{IH_NDRVS}	V_{NDRVS} rising	2.55	3.3		V
NDRVS Input Current	I_{NDRVS}	V_{NDRVS} = 5V		60	80	µA
LED CURRENT SINKS						
IREF Output Voltage	V_{IREF}	I_{IREF} = 40mA	0.86	0.88	0.9	V
IREF Out-of-Range Threshold	IREFOOR		11		17.6	kΩ
Full-Scale OUT_ Output Current	I_{OUT225}	R_{IREF} = 22kΩ, 225mA setting	217	225	231	mA
	I_{OUT100}	R_{IREF} = 22kΩ, 100mA setting	97.5	100	103.5	
Current Regulation Between Strings	$I_{OUT\_MATCH225}$	$I_{OUT\_}$ = 225mA	-2.5		+2.5	%
Current-Setting Resolution	I_{OUT_LSB}			1.5		mA
OUT_ Leakage Current	I_{OUT_LEAK1}	TON_MM_DIS = 1 $V_{OUT\_}$ = 36V, DIM = 0, any OUT pin		1	3	µA
	I_{OUT_LEAK25}	TON_MM_DIS = 1 $V_{OUT\_}$ = 36V, DIM = 0, any OUT_ pin, T_A = +25°C			1	µA
	I_{OUT_LEAK0}	TON_MM_DIS = 0		75	100	µA
OUT_ Minimum Pulse Width	$t_{OUT\_}$			300		ns

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_ Minimum Negative Pulse Width				90		ns
$I_{OUT\_}$ Rise Time	I_{OUT_TR}	10% to 90% I OUT_		150		ns
$I_{OUT\_}$ Fall Time	I_{OUT_TF}	90% to 10% I OUT_		20		ns
DIM INPUT						
DIM Frequency Range			90		50000	Hz
DIM Sampling Frequency				20		MHz
FAULT DETECTION						
LED Short-Detection Threshold	V_{THSHRT}	SLDET[1:0] = 11	7.7	8	8.1	V
		SLDET[1:0] = 10	5.6	6	6.4	
		SLDET[1:0] = 01	2.8	3	3.2	
OUT_ Check-LED-Source Current	I_{OUT_CKLED}	$V_{OUT\_}$ = 0.5V	45	60	75	µA
OUT_ Short-to-GND Detection Threshold	V_{OUT_GND}	$V_{OUT\_}$ falling	230	250	270	mV
OUT_ Unused-Detection High Threshold	V_{OUT_UN}		0.8	0.85	0.9	V
OUT_ Open-LED-Detection Threshold	V_{OUT_OPEN}		230	250	270	mV
Shorted-LED-Detection Flag Delay	t_{SHRT}			6.8		µs
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
BSTMON Overvoltage Threshold	V_{BSTMON_OV}	V_{BSTMON} rising	0.92	0.95	0.98	V
BSTMON Overvoltage Hysteresis	V_{BSTMON_OVHYS}			50		mV
BSTMON Input Bias Current	I_{BSTMON}	0 < V_{BSTMON} < 1V	-1		+1	µA
BSTMON Undervoltage-Trip Threshold	$V_{OVPUVLO}$	V_{BSTMON} rising	0.38	0.4	0.412	V
Boost Undervoltage-Detection Delay	OVPUVLO_BLK			10		µs
Boost Undervoltage-Blanking Time		After soft-startup, fast_ss = 0	49	53.25	57.5	ms
		After soft-start, fast_ss = 1	26.28	28.46	30.74	
TEMP PIN						
TEMP Pin Voltage	V_{TEMP}	I_{TEMP} = -10µA	380	400	420	mV
I_{TEMP} to $I_{OUT_}$Gain		V_{TEMP} < 400mV		0.67		%/µA
TEMP Pin Disable Threshold				0.5		V
TEMP Pin Leakage Current				0.005	0.5	µA
TEMP Current for LED Current Disable	I_{TEMPD}			125		µA
LOGIC INPUTS AND OUTPUTS (EN, SCL, SDA, DIM, FLTB)						

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Inputs Logic-High	V_{IH}		1.22			V
Digital Inputs Logic-Low	V_{IL}				0.6	V
Digital Inputs Hysteresis	V_{HYS}			300		mV
EN Input Pull-Down Resistor	R_{PDEN}		100	165	240	kΩ
EN Blanking Time	t_{EN_BLK}			10		µs
DIM, ADD, and MODE Pull-up Current	I_{DIN_PUP}	V_{DIN} = 0V		2		µA
DIM Frequency Range			90			Hz
DIM Sampling Frequency			18	20	22	MHz
SCL Input Current	I_{DIN}	V_{DIN} = +5V			1	µA
FLTB, SDA Output Low Voltage	V_{OL_OUT}	I_{FLTB} = I_{SDA} = 5mA			0.4	V
FLTB, SDA Output Leakage Current	I_{OUT_LEAK}	V_{EN} = 0V, V_{FLTB} = V_{SDA} = 5.5V			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				160		°C
Thermal-Shutdown Hysteresis				17		°C
Thermal Warning Threshold				125		°C
ANALOG-TO-DIGITAL CONVERTER (ADC)						
ADC Measurement Resolution	ADC BIT			8		bits
Total Measurement Error, Current	E_ADC_I	225mA setting	-12		+12	mA
Total Measurement Error, Voltage	E_ADC_V	V_{BSTMON} = 1V, V_{BATT} - V_{SENSE} = 200mV	-50		+50	mV
ADC Gain Error	ADC GAIN	225mA setting	-4		+4	%
ADC Offset Error	ADC OFF	225mA setting	-4		+4	LSB
Measurement Resolution, Current	LSB OUT			1		mA
Measurement Resolution, BSTMON	LSB_{BSTMON}			3.92		mV
Measurement Resolution, BATT-SENSE	LSB_{SENSE}			1		mV
I²C INTERFACE						
Clock Frequency	f_{SCL}				0.4	MHz
Hold Time (Repeated) START	$t_{HD:STA}$		600			ns
SCL Low Time	t_{LOW}		1300			ns
SCL High Time	t_{HIGH}		600			ns
Setup Time (Repeated) START	$t_{SU:STA}$		600			ns

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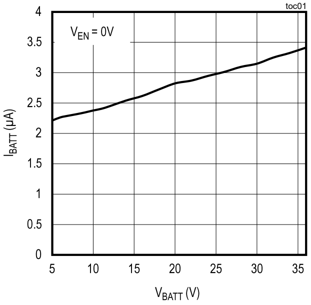
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$		0			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		600			ns
Spike Suppression				50		ns

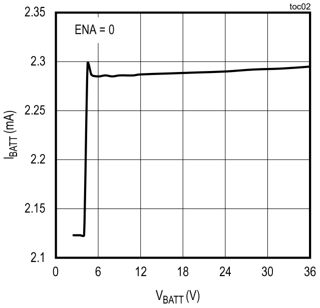
Typical Operating Characteristics

($V_{IN} = V_{EN}$ = 12V, 6x9 LED load at 200mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

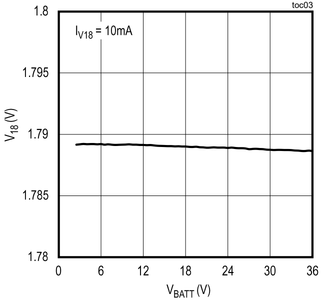
TOTAL BATT SHUTDOWN CURRENT vs. BATT SUPPLY VOLTAGE



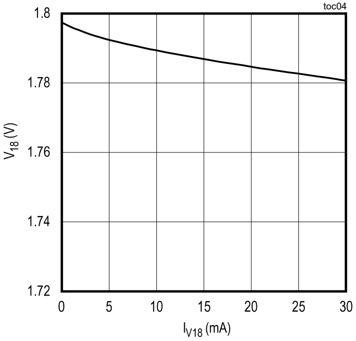
TOTAL BATT QUIESCENT CURRENT vs. BATT SUPPLY VOLTAGE



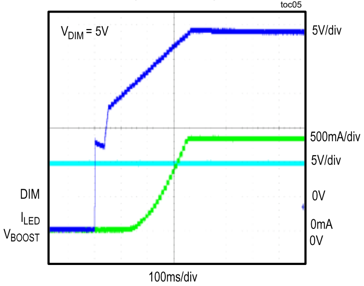
V_{18} LINE REGULATION



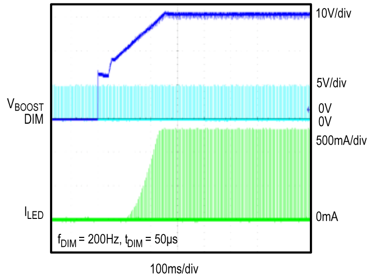
V_{18} LOAD REGULATION



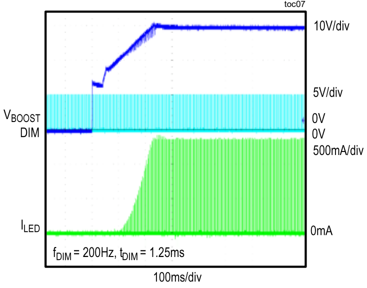
STARTUP WAVEFORM (FAST_SS = 0)



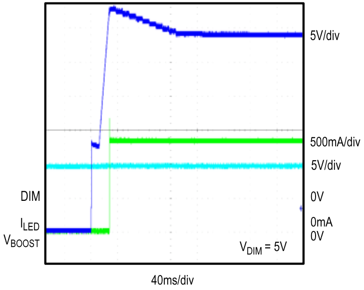
STARTUP WAVEFORM (FAST_SS = 0)



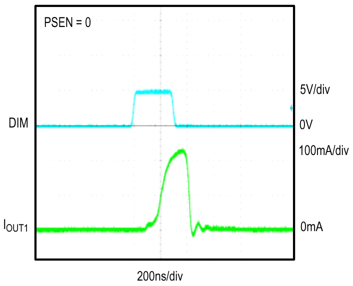
STARTUP WAVEFORM (FAST_SS = 0)



STARTUP WAVEFORM (FAST_SS = 1)

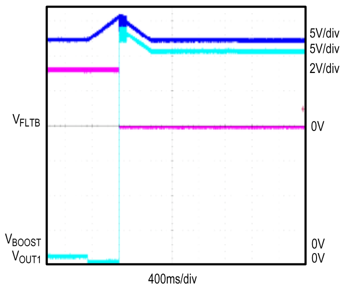


LED SWITCHING WITH DIMMING PULSE WIDTH OF 300ns

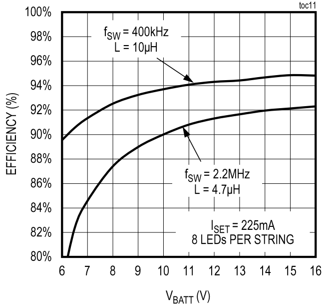


(V_{IN} = V_{EN} = 12V, 6x9 LED load at 200mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

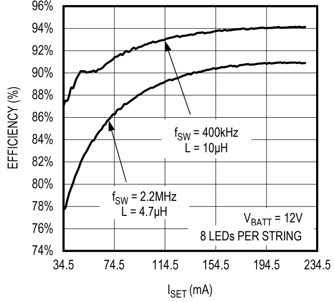
LED OPEN FAULT ON OUT1



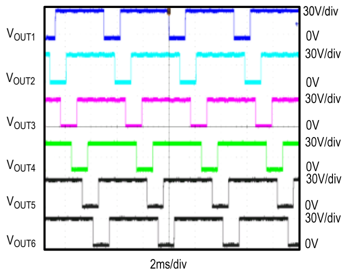
LED DRIVER EFFICIENCY vs. BATT VOLTAGE



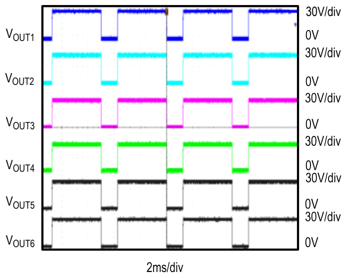
LED DRIVER EFFICIENCY vs. ISET CURRENT



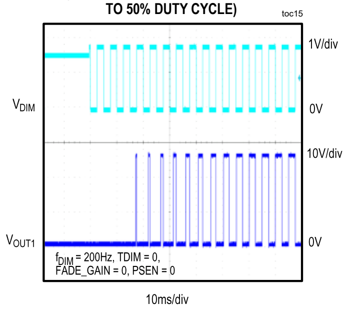
LED OUTPUTS WITH PHASE SHIFT (f_{DIM} = 200Hz, DUTY CYCLE = 25%)



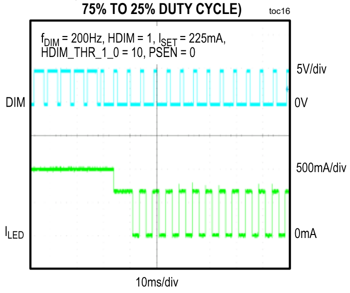
LED OUTPUTS WITHOUT PHASE SHIFT (f_{DIM} = 200Hz, DUTY CYCLE = 25%)



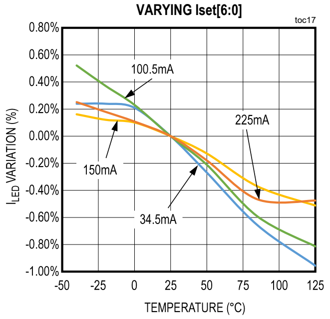
FADING WAVEFORM (DIMMING TRANSITION FROM 100% TO 50% DUTY CYCLE)



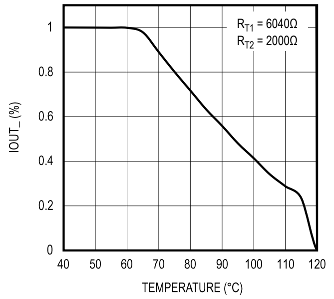
HYBRID DIMMING WAVEFORM (DIMMING TRANSITION FROM 75% TO 25% DUTY CYCLE)



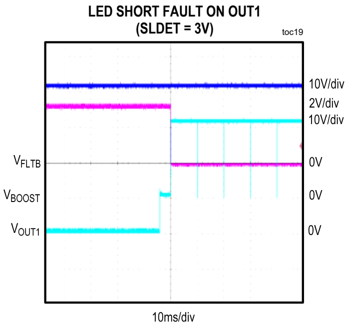
LED CURRENT VARIATION vs. TEMPERATURE VARYING Iset[6:0]

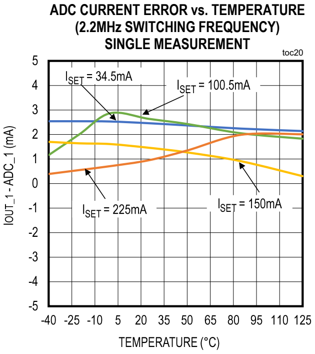


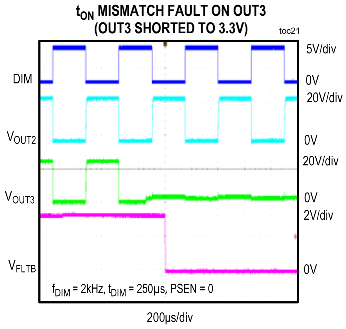
LED CURRENT vs. TEMPERATURE (TEMPERATURE FOLDBACK)

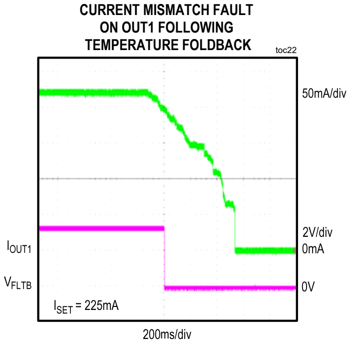


(V_{IN} = V_{EN} = 12V, 6x9 LED load at 200mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

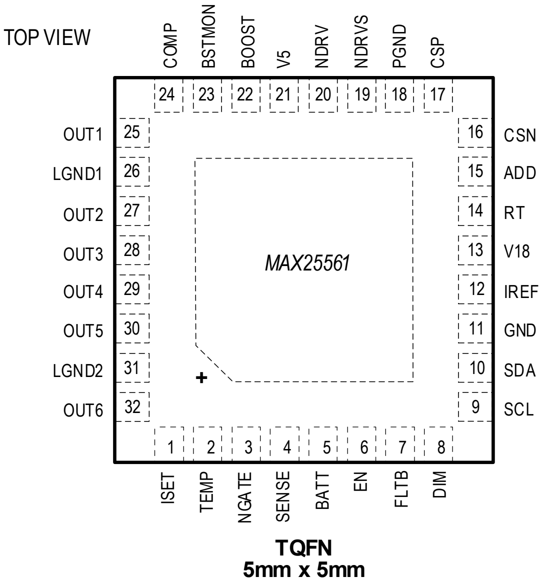








Pin Configurations

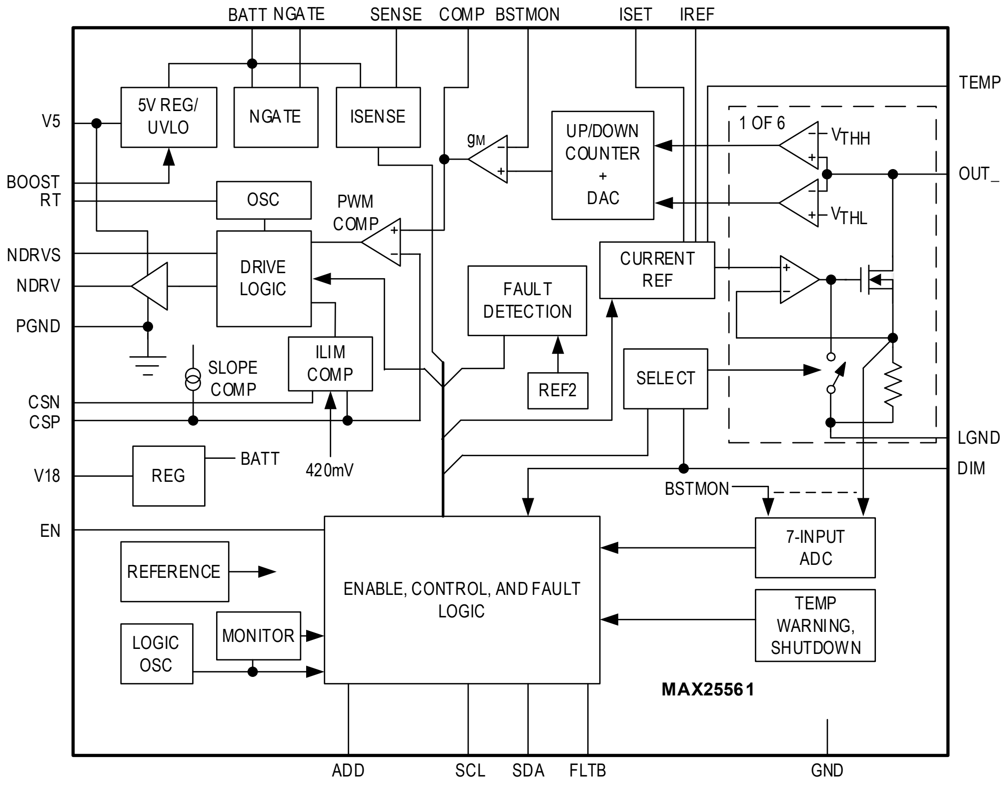


Pin Descriptions

PIN	NAME	FUNCTION
1	ISET	Startup LED Current Setting Pin. Connect a resistor to this pin to set the initial LED current in each of the channels and enable startup when the EN pin is taken high. LED current can be adjusted by writing to the ISET_REG register after startup. If using I^{2}C to set the LED current and enable the device, connect the ISET pin to V18.
2	TEMP	Temperature Sensor Input. To implement LED current reduction at high temperatures, connect an NTC temperature sensor to GND with resistors from the NTC to TEMP and V18. If unused, connect TEMP to V18.
3	NGATE	Gate Connection for External Series nMOSFET Driven by the Internal Charge Pump
4	SENSE	Boost Input Current Sense Input. Connect to a sense resistor in series with the boost input. If unused, connect SENSE to BATT.
5	BATT	LED Driver Supply Input. Connect BATT to a 4.5V to 40V supply. Bypass BATT to ground with ceramic capacitors of 2.2mF and 0.1nF.
6	EN	Enable Input. When EN is high, the device is enabled. When EN is low, the device is in shutdown with low quiescent current. EN has an internal pull-down resistor.
7	FLTB	Active-Low, Open-Drain Fault Indication Output. Connect an external pull-up resistor from FLTB to an external supply lower than 5V.
8	DIM	PWM Dimming Input. DIM has an internal pull-up to V18.
9	SCL	I^{2}C Clock Input
10	SDA	I^{2}C Data I/O
11	GND	Ground Connection
12	IREF	Reference Current Set Pin. Connect a 1% resistor of value 22kΩ from IREF to GND.
13	V18	Output of Internal 1.8V Regulator. Connect a 2.2µF capacitor from V18 to GND with an additional 100nF capacitor close to the V18 and GND pins.
14	RT	Frequency Setting Resistor for Backlight Boost Converter
15	ADD	Device Address Select Pin. Connect to GND or V18 to select the device I^{2}C address. See *Table 3*. ADD has an internal pull-up to V18.
16	CSN	LED Driver MOSFET Negative Current-Sense Connection. Connect this pin directly to the GND side of the compensation network connected to the COMP pin.
17	CSP	LED Driver MOSFET Positive Current-Sense Connection. Connect a sense resistor from the MOSFET source to PGND and a further resistor from the MOSFET source to the CSP pin to set the slope compensation (see the *Current-Sense Resistor and Slope Compensation* section).
18	PGND	Power Ground Connection
19	NDRVS	Sense Connection for Gate of External MOSFET. Connect NDRVS directly to the gate after the gate resistor.
20	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching power MOSFET. Typically, a small resistor (1Ω to 22Ω) is inserted between the NDRV output and nMOSFET gate to decrease the slew rate of the gate driver and reduce the switching noise.
21	V5	5V Regulator Output, Voltage Supply for NDRV Gate Driver. Place 2.2µF and 22nF ceramic capacitors as close as possible to the device, between V5 and GND.
22	BOOST	Boost Output Voltage Connection. BOOST is used to supply power to the V$_{CC}$ regulator when the IN voltage is too low. Bypass with a 0.1mF capacitor placed close to the pin.
23	BSTMON	LED Driver Output-Voltage-Sensing Input. This voltage is used for overvoltage and undervoltage protection. Connect a resistor-divider between the boost converter output, BSTMON pin, and GND.
24	COMP	LED Driver Switching-Converter Compensation Input. Connect an RC network from COMP to GND to compensate the backlight boost converter.
25	OUT1	LED String 1 Cathode Connection. Do not connect more than 470pF of capacitance from OUT1 to GND.
26	LGND1	LED Ground Connection
27	OUT2	LED String 2 Cathode Connection. Connect OUT2 to ground using a 9.1kΩ resistor if not used. Do not connect more than 470pF of capacitance from OUT2 to GND.

28	OUT3	LED String 3 Cathode Connection. Connect OUT3 to ground using a 9.1kΩ resistor if not used. Do not connect more than 470pF of capacitance from OUT3 to GND.
29	OUT4	LED String 4 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor if not used. Do not connect more than 470pF of capacitance from OUT4 to GND.
30	OUT5	LED String 5 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor if not used. Do not connect more than 470pF of capacitance from OUT5 to GND.
31	LGND2	LED Ground Connection
32	OUT6	LED String 6 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor if not used. Do not connect more than 470pF of capacitance from OUT6 to GND.
—	EP	Exposed Pad. Connect to a large contiguous copper-ground plane for optimal heat dissipation. Do not use EP as the only electrical ground connection.

Functional Diagrams



Detailed Description

The MAX25561 is a 6-channel LED backlight driver with an integrated current-mode boost controller that operates over a switching frequency range of 400kHz to 2.2MHz and incorporates spread spectrum. Selectable phase-shifting of the output channels is included to reduce EMI. The MAX25561 provides up to 220mA per channel. The device is capable of operating down to very low battery voltages while maintaining 5V drive for the external MOSFET at NDRV.

Extensive diagnostics and an I^2C interface are included to assist with system ASIL B compliance.

The MAX25561 is available in a compact TQFN package and operates over the -40°C to +125°C temperature range.

Undervoltage Lockout

The device features three undervoltage circuits that monitor the input voltage at BATT and the outputs of the internal LDO regulators at V5 and V18. The backlight boost can be enabled only when BATT, V5, and V18 exceed their respective UVLO thresholds.

BATT_UV Indication Bit

The BATT_UV bit in DIAG2_REG indicates when the BATT input is below the undervoltage lockout. During power-up, until the BATT input has crossed its undervoltage threshold, it is not possible to communicate with the device and thus the BATT_UV bit cannot be read.

Low-Voltage Operation

After the boost soft-start is completed, the MAX25561 continues to operate with BATT voltages lower than 5V while maintaining 5V drive for the external MOSFET at NDRV. When the voltage at BATT drops to V_{BATT_LVF}, the V5 regulator switches its input from BATT to BOOST, the boost converter current limit is automatically increased to V_{CSP_LV}, and the switching frequency is reduced if it is greater than 1.4MHz. Switchover occurs as long as the voltage on BOOST is above

V_{BATT_LVF}. In this mode, if the standard current limit is exceeded on 4 consecutive cycles, a 100ms timer is started, which returns the current limit to its original value when it expires.

When BATT returns to a voltage above V_{BATT_LVR}, the V5 regulator resumes operation from BATT and the converter current limit and switching frequency return to their former values. Bypass BATT and BOOST with ceramic capacitors placed close to the respective pins.

At very low input voltages, the efficiency of the boost converter reduces and the input current can reach very high levels as a consequence. The external boost converter components must be selected for worst-case operation. An alternative is to reduce the output power at low input voltages.

If the voltage at BATT drops below the undervoltage lockout level (V_{BATT_UVF}) at any time, the boost converter is disabled.

Input Current Monitoring

Input overcurrent protection is implemented by using an external sense resistor connected between BATT and SENSE. If the voltage across the sense resistor exceeds 200mV after the 2ms NGATE turn-on phase (Stage 1 of startup) for a time greater than 4µs, the boost converter is latched off, the ISNS_SD bit in the DIAG2_REG register is set, and the FLTB pin is asserted low. The shutdown function can be disabled by setting the DIS_ISNS_SD bit to 1. In that case, the device continues operation when an input overcurrent is detected; the ISNS_SD bit is set but FLTB does not assert low.

To reenable the device, toggle the power supply, the EN input pin, or the ENA bit.

The value of the voltage between BATT and SENSE is continuously sampled by the internal ADC, and the most recent value can be read from the VSENSE register.

Oscillator Frequency/External Synchronization

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor (R_{RT}) connected from the RT pin to GND. Use the following equation to calculate the value of R_{RT} for the desired switching frequency (f_{SW}).

$$R_{RT} = \frac{26130}{f_{SW}} + 0.33$$

where R_{RT} is in kΩ and f_{SW} is in kHz. If the value of the RT resistor is too low or if the pin is shorted to GND, the boost converter will not start and the FLTB pin will go low.

To synchronize the oscillator with an external clock, AC-couple the external clock to the RT input. The value of the capacitor used for AC-coupling is C_{SYNC} = 10pF, and the duty cycle of the external clock should be 50%. When synchronizing the converter do not apply the synchronizing signal to the RT pin at startup, as this may cause the RT resistor value check to fail.

At low input voltages and when the switching frequency is above 1MHz, the switching frequency is automatically reduced to enable high-duty-cycle operation and maintain output voltage regulation. This applies also when the device is synchronized to an external frequency.

Spread Spectrum

The IC includes spread-spectrum modulation that reduces peak electromagnetic interference (EMI) at the switching frequency and its harmonics. Spread spectrum can be enabled and disabled using the SS_OFF bit in the register SETTING_REG.

Spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the range of 94% to 106% or 96% to 104% (depending on the setting of the SSL bit) of the programmed switching frequency set through the external resistor from RT to GND. When spread spectrum is used, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the peak energy at the relevant frequency.

Spread spectrum is disabled if external synchronization is used.

LED Current Control

The IC features six identical constant-current sources used to drive multiple high-brightness LED strings. The current through each of the channels is adjustable between 34.5mA and 225mA by setting the 7-bit value iset[6:0] in the ISET_REG register.

To accelerate device startup, the initial LED current can be set by connecting a resistor from the ISET pin to GND. With this resistor present, the ENA bit is initialized to 1, and the device starts up immediately when the EN pin is taken high. A current value determined by the resistor on ISET is loaded into the iset[6:0] field in ISET_REG and can be adjusted subsequently using the I^2C interface. Select the ISET resistor value using *Table 1*.

Table 1. ISET Resistor Value for a Given LED Current

ISET RESISTOR (kΩ)	LED CURRENT PER CHANNEL (mA)	CORRESPONDING ISET REGISTER VALUE
4.3	96	0x29
9.1	106.5	0x30
15	118.5	0x38
24	130.5	0x40
33	145.5	0x4A
43	162	0x55
56	180	0x61
68	199.5	0x6E

Multiple channels can be paralleled together for string currents exceeding 225mA.

Current-Mode DC-DC Controller

The device contains a constant-frequency, current-mode controller designed to drive the LEDs in a boost or SEPIC configuration. The IC features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks to minimize power dissipation.

Programmable slope compensation is used to avoid subharmonic oscillation that can occur at > 50% duty cycles in continuous-conduction mode.

The external nMOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) connected from the source of the external nMOSFET to PGND.

The IC features leading-edge blanking to suppress the external nMOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the external nMOSFET when the voltage at CSP exceeds the error amplifier's output voltage (at the COMP pin). This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier.

The BSTMON gain (A_{OVP}) is defined as V_{OUT}/V_{BSTMON}, or (R17 + R16)/R16. The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation, while still ensuring accurate LED current. Each current sink has a window comparator with a low threshold of 0.58V and a high threshold of 0.85V. These comparators drive logic that controls an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit digital-to-analog converter (DAC), which sets the reference to the error amplifier.

9-Bit DAC

The error amplifier's reference input is controlled with an 9-bit DAC. The DAC output is ramped up during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to between 0.482V and 0.996V. Because the DAC output is limited to no less than 0.482V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum output-voltage step according to the following equation:

$$V_{STEP\_MIN} = V_{DAC\_LSB} \times A_{OVP}$$

where V_{STEP_MIN} is the minimum output-voltage step, V_{DAC_LSB} is 1.95mV (typ), and A_{OVP} is the BSTMON resistor-divider gain (1 + R6/R7).

Startup Sequence

The boost converter startup sequence occurs in three stages, as described in the Stage 1, Stage 2, and Stage 3 sections. The overall startup time can be selected using the fast_ss bit in the BL_CONFIG1 register when using the I^2C interface. The boost output voltage at the end of Stage 2 differs between the slow and fast startup modes.

Stage 1

After the ENA bit has been set to 1, the controller turns on the NGATE charge pump for the external nMOSFET if the V5 and BATT voltages are above their respective undervoltage thresholds. The output current of the charge pump charges the gate of the external nMOSFET, thus turning it on. After a 2ms timeout expires, Stage 2 of the startup begins. If NGATE is unused, set the CP_DIS bit in the DISABLE_REG register to disable the NGATE charge pump.

Stage 2

After the external MOSFET on NGATE has been enabled, the IC goes through its power-up checks, including unused string detection and OUT_ short-to-ground detection. To avoid possible damage, the converter does not start if any OUT_ is detected as shorted to ground.

Any current sinks detected as unused are disabled to prevent a false fault-flag assertion during normal operation. After these checks have been performed, the converter begins to operate and the output voltage begins to ramp up. The DAC reference to the error amplifier is stepped upwards until the OVP pin reaches 0.48V (or 0.88V in fast startup mode).

This stage duration is fixed at approximately 50ms (22ms in fast startup mode).

Stage 3

The third stage begins once the second stage is complete and the DIM input goes high. During Stage 3, the output of the converter is adjusted until the minimum OUT_ voltage falls within the window comparator limits of 0.58V (typ) and 0.85V (typ). The output ramp is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input. If the DIM input is a 100% duty cycle (DIM = high), then the DAC output is updated once every 10ms.

The total soft-start time can be calculated using the following equation in slow-startup mode:

$$t_{SS} = 50ms + \frac{V_{LED} + 0.87 - (0.48 \times A_{OVP})}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where t_{SS} is the total soft-start time, 50ms is the fixed Stage 1 duration, V_{LED} is the total forward voltage of the LED strings, 0.81V is midpoint of the window comparator, A_{OVP} is the gain of the OVP resistor-divider, f_{DIM} is the dimming frequency (use 100Hz if the DIM input duty cycle is 100%), and 0.01V is the maximum voltage step per clock cycle of the DAC.

In fast-startup mode (when the FAST_SS bit in the SET_REG register is set to 1), the following equation should be used:

$$t_{SS} = 25ms + \frac{0.88 \times A_{OVP} - (V_{LED} + 0.87)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

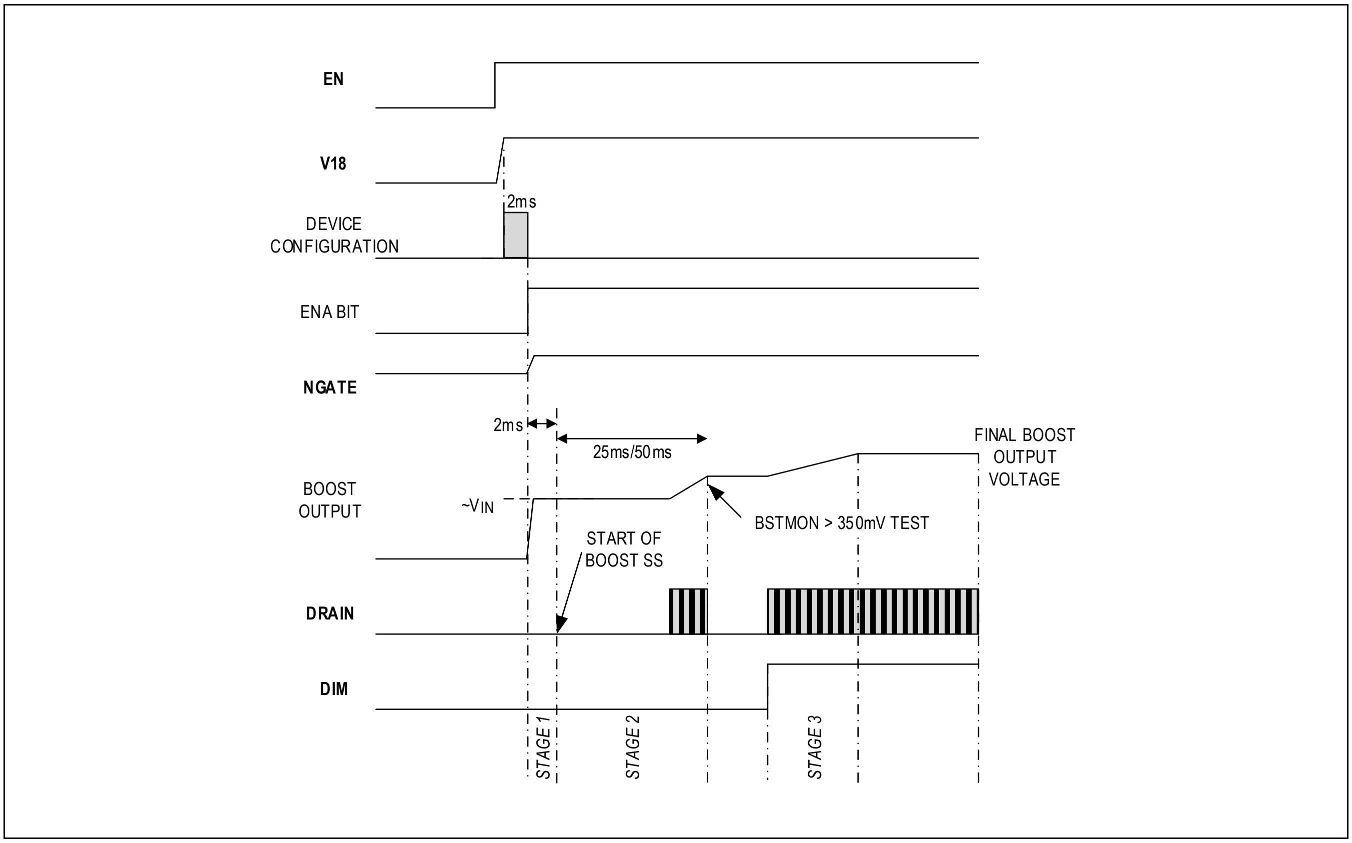


Figure 1. Start-up Sequence

Dimming

Dimming can be performed using an external PWM signal applied to the DIM pin or by writing to the TONn_REG registers, where n is the number of the OUT_ pin (after setting the DIM_EXT bit to 0). When the TON_ALL bit is set to 1, the TON1_ value is used for all active outputs.

The signal on the DIM pin is sampled with a 20MHz internal clock, except when phase-shifting is disabled, in which case the DIM signal controls the OUT_ outputs directly.

Low-Dimming Mode

The IC's operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time is lower than 50µs (typ), the device enters low-dimming mode (which is indicated by the bits in the LO_DIM register). In this state, the converter switches continuously and LED short detection is disabled. When the DIM input is greater than 51µs (typ) the device goes back into normal operation, enabling the short-LED detection and switching the power FET only when the effective dimming signal is high.

Phase-Shift Dimming

When the PSEN bit in register SET_REG is set to 1, phase-shifting of the LED strings is enabled. To achieve this, the DIM signal is sampled internally by a 20MHz clock. The device automatically sets the phase shift between strings to a value depending on the number of strings enabled.

When phase-shifting is enabled, the sampled DIM input is used to generate separate phase-shifted dimming signals for each LED string. The resolution with which the DIM signal is captured degrades at higher DIM input frequencies; therefore, dimming frequencies between 100Hz and 3kHz are recommended, although higher dimming frequencies are technically possible. The phase shift between strings is determined by the following equation:

$\Theta = 360/n$

where n is the total number of strings being used and θ is the phase shift in degrees. See *Figure 2* for a timing diagram example with phase-shifting enabled.

When phase-shifting is disabled, all strings turn on/off at the same time controlled directly by the DIM input. If multiple current sinks are being connected in parallel, phase-shifting should be disabled.

If a fault is detected, resulting in a string being disabled during normal operation, the phase-shifting adjusts to the new situation.

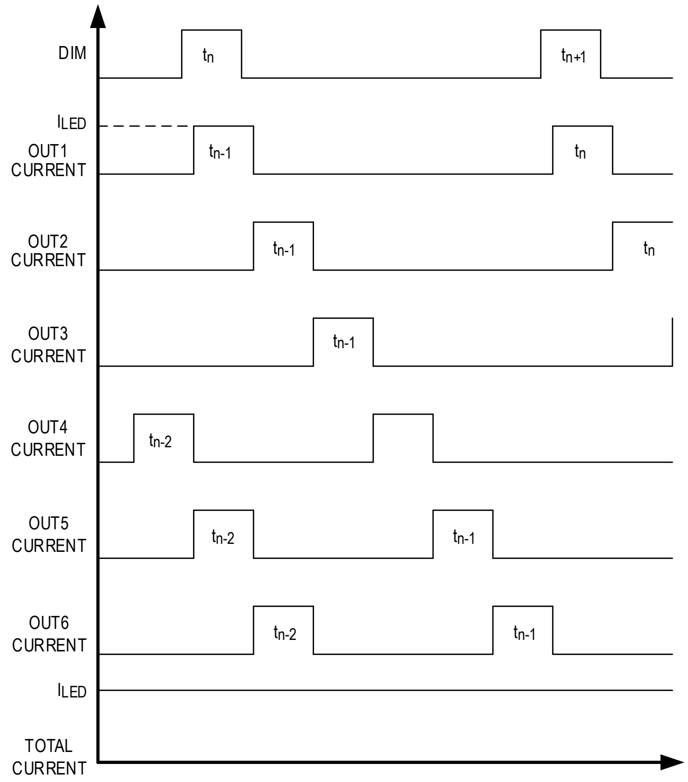


Figure 2. Phase-Shifted Outputs

Automatic Fade-In/Fade-Out During Dimming

The device can be configured to perform a smooth change in brightness even when the DIM input duty cycle or TON_ setting is changed by setting the FADE_IN_OUT bit in the FADING_REG register to 1.

When using the fade function, it is important to maintain the DIM frequency constant when entering 100% duty cycle. This is necessary in order to avoid erroneous frequency measurement, which could change the speed of the fade-in.

Disabling Individual Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 9.1kΩ resistor, or set the corresponding DIS_ bit to 1 in the DISABLE register before the ENA bit is set. During startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between the maximum value of V_{OUT_GND} and the minimum value of V_{OUT_UN} during this check.

Note: When disabling unused strings, it is necessary to start by disabling the highest numbered current sinks first (e.g., if two strings need to be disabled, disable OUT6 and OUT5. Do not disable any two strings at random). During normal operation, strings can be selectively turned off by changing the corresponding TON_ setting to 0. This is only possible when internal dimming is used (not when using the DIM input pin).

Hybrid Dimming

To invoke hybrid dimming mode, set the HDIM bit in register IMODE_REG. In hybrid dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty cycle decreases from 100% (see *Figure 3*). At the crossover level set by the HDIM_THR_1_0[1:0] bits, dimming transitions to PWM dimming where the LED current is chopped. Depending on the DIM_EXT bit, the device functions in one of two ways:

- (DIM_EXT = 1) measures the duty cycle on the DIM pin and translates it into a combined LED current value and PWM setting.
- (DIM_EXT = 0) takes the 18-bit value from the TON1 register and translates it into a combined LED current value and PWM setting.

Figure 3 illustrates the difference between standard and hybrid dimming with phase-shifting enabled.

Hybrid Dimming Operation

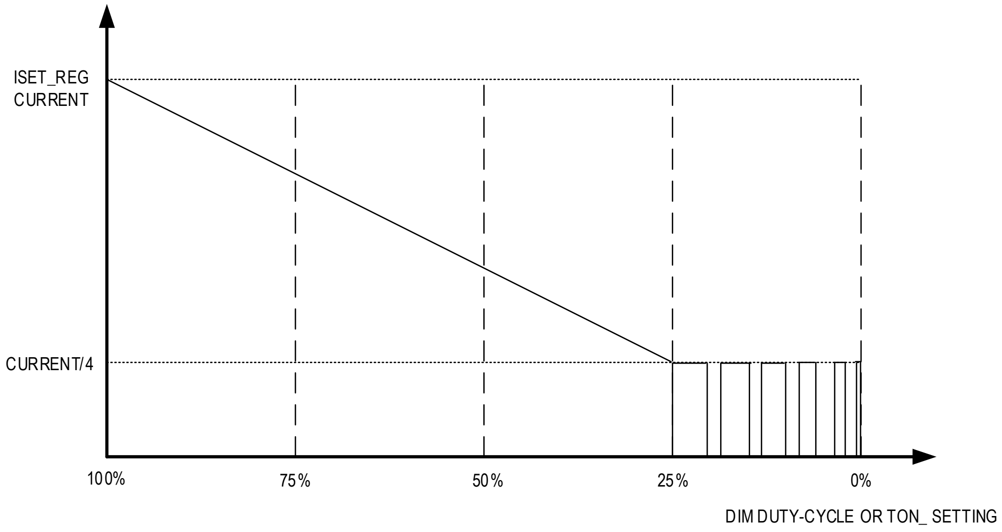


Figure 3. Hybrid Dimming Operation with HDIM[1:0] = 10 (25%)

Temperature Foldback

In standalone mode, when an NTC temperature sensor is connected between GND and a resistor (RT1) that is connected to the V18 supply, with a further resistor (RT2) connected from the junction of the NTC and RT1 to the TEMP pin, temperature foldback is implemented. When the temperature reaches the temperature T1 (set by RT1), the current in the LEDs is reduced according to the linear scheme shown in *Figure 4*. The slope of the current reduction is set by RT2. The MAX25561 is specifically designed to be used with the NTCLE100E3 or a similar NTC device. *Table 2* illustrates some examples of values of RT1 and RT2 to obtain certain values of T1 and T_{DELTA}.

Table 2. Temperature Resistor Values

RT1 (kΩ)	RT2 (kΩ)	T1 (°C)	T_{DELTA} (°C)
6.04	1.2	70	30
6.04	2	70	50

When the temperature reaches T1, the OTW bit in register DIAG_REG is asserted. When the temperature reaches T_{OFF}, the LED current is turned off, the bl_ot bit is set high, and the FLTB pin asserts low.

Temperature Foldback with OUT_ Current Mismatch Diagnostic

When temperature foldback is used in conjunction with the current mismatch, diagnostic current mismatch will be indicated at some point above T1.

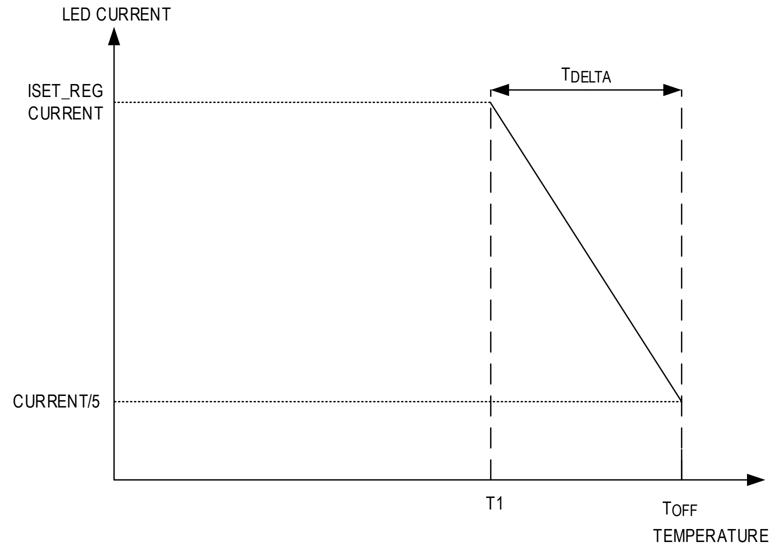


Figure 4. Temperature Foldback Curve

TEMP External Circuit

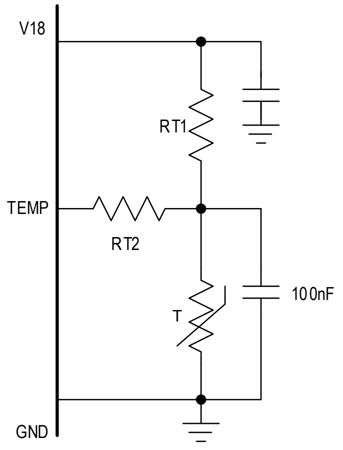


Figure 5. TEMP External Circuit

Hybrid Dimming Operation Modes

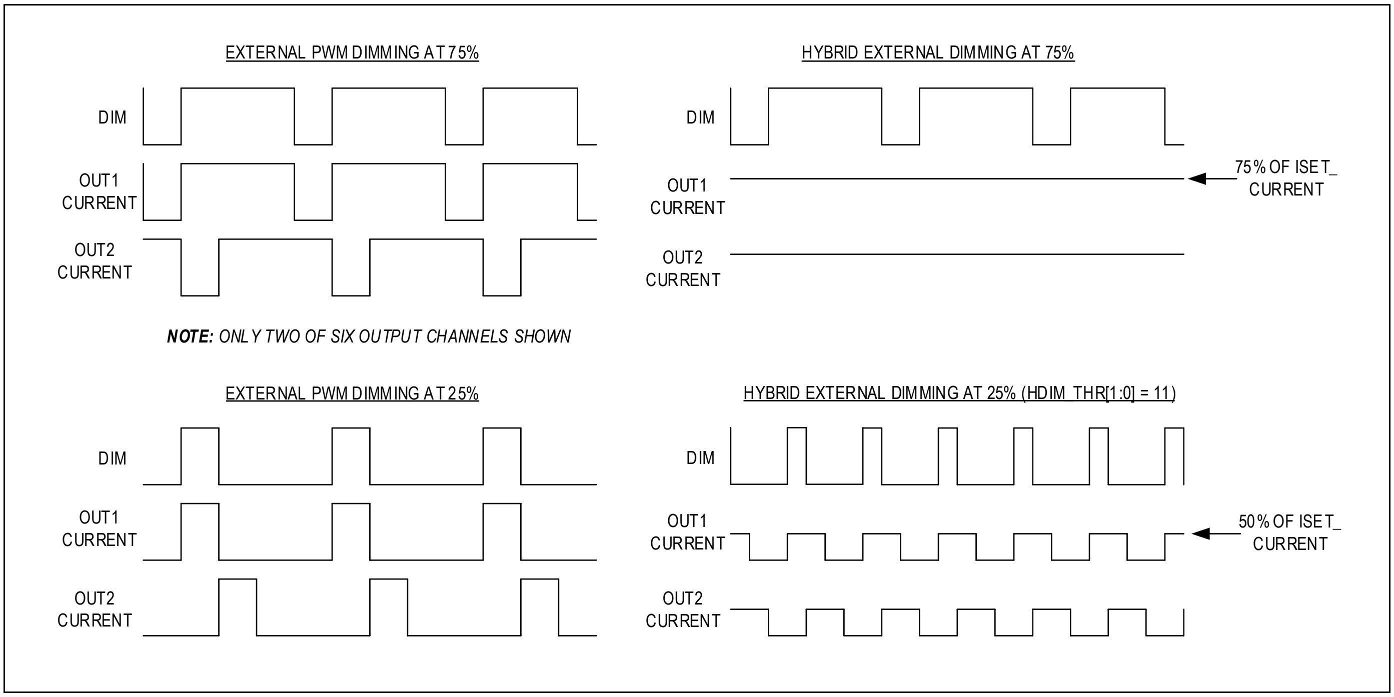


Figure 6. Hybrid Dimming Operation Modes

Diagnostics and FLTB Output

The open-drain fault flag output (FLTB) goes low when a fault is detected. Certain faults can be inhibited from causing FLTB to go low using the bits in the MASK1 and MASK2 registers.

FLTB asserts low for the following faults if not masked (note that not all faults can be masked):

- OUT_ open, shorted LED, short to ground
- OUT_ current mismatch, OUT_ TON I/O mismatch
- RT out of range, IREF out of range, ISET out of range, VREF out of range
- Boost undervoltage, V18 out-of-range, V5 out-of-range
- Interface PEC error, clock error, internal nonvolatile memory error
- Undervoltage on BATT, boost input overcurrent
- Overtemperature warning

Open-LED Management and Overvoltage Protection

After the soft-start of the boost converter, the IC detects open-LED strings and disconnects any such strings from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within correct limits and maintains high efficiency. The current in strings that have been detected open is not measured by the ADC and reads as zero.

During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, the BSTMON input, and GND. The overvoltage-protection threshold at the DC-DC converter output is determined using the following equation:

$$V_{OUT_{BSTMON}} = 0.95 \times \left(1 + \frac{R16}{R17}\right)$$

where 0.95V (typ) is the overvoltage threshold on BSTMON (see the *Functional Diagram*). Select V_{OUT_BSTMON} according to the following formula:

$$1.1 \times \left(V_{LED_{MAX}} + 0.87\right) < V_{OUT_{BSTMON}} < 2 \times \left(V_{LED_{MIN}} + 0.55\right)$$

where:
V_{LED_MAX} = Maximum expected LED string voltage

V_{LED_MIN} = Minimum expected LED string voltage

Select R16 and R17 such that the voltage at OUT_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the internal MOSFET is switched off. The overvoltage threshold should be set to less than twice the minimum LED voltage to ensure proper operation and that the BSTMON minimum regulation point of 600mV (typ) is not breached. When an open-LED overvoltage condition occurs, FLTB is latched low.

If all active OUT_ channels are detected as open, the boost converter is disabled. Toggle the EN pin or cycle the power supply to clear an open-LED condition.

Short-LED Detection

The IC checks for shorted LEDs after the current in any channel is turned on. A shorted-LED is detected at OUT_ if the following condition is met:

$V_{OUT\_} > RSDT$

Where RSDT is the programmable short-LED-detection threshold set by the SLDET[1:0] bits in the SETTING_REG register.

If a short is detected on any of the strings, the affected LED strings are disabled after a delay of one dimming cycle and the FLTB output flag asserts low after two dimming cycles until the device detects that the shorts are removed. Disable short-LED detection by setting SLDET[1:0] to 0x0. Short-LED detection is disabled in low-dimming mode. In external dimming mode with the DIM input connected continuously high, the OUT_ pins are periodically scanned to detect shorted LEDs. The scan frequency is 100Hz. Similarly, when DIM_EXT = 0 and internal dimming is being used, shorted LEDs are still detected by periodically scanning the OUT_ states at 100Hz.

Short-LED detection is also disabled in cases where all active OUT_ channels rise above 2.5V. This can occur in a boost-converter application when the input voltage becomes higher than the total LED string voltage drop, such as during a battery load dump. If a short-LED fault occurs during a load dump, the fault flag does not assert until the load dump is over and the minimum OUT_ voltage has fallen below 2.35V. If a load dump occurs after a short LED is detected, the fault flag deasserts until the load dump is over and the minimum OUT_ voltage has fallen below 2.35V, at which point, the fault flag reasserts.

LED Short-to-Ground Protection

During startup, a check is performed for OUT_ pins shorted to ground by sourcing a current of 60μA into the OUT_ pins. If the pin voltage does not exceed V_{OUT_GND}, a short to GND is declared. In this case, the device does not start. Toggle the EN pin or power to clear this condition.

Analog-to-Digital Converter (ADC)

The 8-bit ADC is used to measure the current in each of the strings, the voltage on the BSTMON pin, and the voltage between the BATT and ISENSE pins. The reference for the ADC is the second redundant bandgap. The ADC is free-running and begins operation at the beginning of Stage 3 of boost startup and is disabled whenever the boost converter is disabled (by the ENA bit or due to any fault which disables the converter). When the ADC is disabled after a fault, the last ADC conversion results are maintained in the appropriate registers.

The ADC cycles continuously between OUT1-6, V_{BSTMON}, and $V_{BATT\text{-}ISENSE}$. At the end of each cycle, the IOUT1–IOUT6 and VBSTMON registers contain the updated values. The full-scale value of the current measurement is 255mA (resolution 1mA) with an IREF resistor of 22kΩ. Conversions of channels that are in low-dim mode yield a value of 0x00. Similarly, any channels that are disabled, open-circuit, or in the shorted-LED condition will read zero current.

The full-scale value of the BSTMON pin voltage conversion is 1V with a resolution of 3.92mV. The full-scale value of the $V_{BATT\text{-}ISENSE}$ measurement is 255mV. Values higher than full scale read as 0xFF.

The duration of a complete conversion depends on whether or not phase-shifting is enabled. With phase-shifting enabled, a complete conversion can take up to two dimming cycles. With phase-shifting disabled, one dimming cycle is the worst-case latency (the conversion is initiated at the beginning of a DIM cycle and concluded < 50μs later).

Measured OUT_ Current Mismatch

Using the MM_MODE bit, the behavior of the device when an output current mismatch is detected can be selected:

- When MM_MODE is 0, a mismatch of more than 20 bits causes FLTB to assert low. No other action is taken.
- When MM_MODE is 1, a mismatch of more than 20 bits causes FLTB to assert low and the device to stop operation.

The current mismatch check is disabled during the soft-start of the boost converter and under the following conditions:

- When a channel is below the OUT_ regulation low threshold
- When a channel is in low-dim mode
- When a channel is set to zero brightness (internal dimming)
- When hybrid dimming is enabled
- After a write to the iset[6:0] field; the check is then disabled for two DIM cycles

To clear a current mismatch fault, the EN pin, ENA bit, or device power must be toggled.

V_{REF} Out-of-Range Detection

The device contains two separate bandgap references which are continuously compared to each other. If the difference between the two is greater than 8%, the FLTB pin is asserted low and the VREFOOR bit in the DIAG2_REG register is set to 1. No further action is taken; if desired, the host can disable the device using the EN pin.

V5 Out-of-Range Detection

The device monitors the V5 gate drive voltage and, if the voltage is detected to be above the overvoltage threshold or below the undervoltage threshold, device operation ceases, the FLTB pin is asserted low, and the V5OOR bit in the DIAG2_REG register is set to 1.

Clock Error

The internal device clock is monitored continuously. If the clock is inactive for more than 1ms or is out of range, the CLK_ERR bit in DIAG2_REG is set to 1 and the FLTB pin is asserted low. When this fault occurs, the FLTB pin asserts low and the local microcontroller should disable the device using the EN pin. This fault can only be cleared by power-on reset (POR).

Input/Output On-Time Comparison

The device monitors the OUT_ voltage after the output is turned off to ensure that the output duty cycle is not larger than the input duty cycle. The voltage threshold used is set by the SLDET[1.0] bits. When using this diagnostic, a resistor of value 20kΩ should be connected from each OUT_ pin to the output of the boost converter.

The timing diagram in *Figure 7* shows the sequence of events with phase-shifting disabled (though the scheme will work equally with phase-shift enabled). At time t1, the DIM input goes high and, after a short delay, the OUT_ current sink turns on and pulls the voltage at OUT_ low. A comparator monitoring OUT_ detects that the OUT_ voltage has fallen below a threshold. At time t2, DIM returns low and, if there is no malfunction, the voltage on OUT_ returns high and the comparator output goes low. At a defined time after the DIM signal has gone low (t_{DEL} = 100µs), the comparator output is continuously monitored. If the comparator output goes high, an error is detected. This check may not function at duty cycles with an off-time of less than 100µs.

When this error is detected, the corresponding bit in the TON_MISMATCH register is set and FLTB is asserted low (unless masked using the TON_MM_MASK bit). In addition, the bit MM_MODE determines whether the device is automatically disabled:

- When MM_MODE is 0, a T_{ON} mismatch is indicated, but no further action is taken.
- When MM_MODE is 1, a T_{ON} mismatch causes the device to stop operation. After device operation is stopped, it can be restarted by toggling power, the EN input pin, or the ENA bit.

This check can be disabled globally using the TON_MM_DIS bit in the MM_DIS register or individually for any of the outputs using the TONn_MM_DIS bits where n is the number of the output from 1 to 6.

To clear a T_{ON} mismatch fault, the EN pin or device power must be toggled.

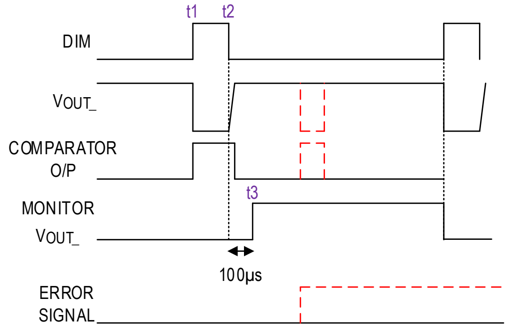


Figure 7. Input/Output On-Time Comparison

Thermal Warning/Shutdown

The IC includes thermal protection that operates at a temperature of +160°C. When the thermal-shutdown temperature is reached, the device is immediately disabled so it can cool. When the junction temperature falls by 17°C, the device is reenabled with the same settings as before (the boost converter performs a soft-start). When a thermal shutdown occurs, the FLTB pin goes low and the OT bit in the DIAG1_REG register is set to 1.

A thermal warning bit (OTW) is also implemented in the DIAG1_REG register and indicates that the junction temperature has exceeded +125°C. The OTWMASK bit in the MASK1_REG register controls whether or not an active OTW bit causes the FLTB pin to go low.

I^2C Interface

The MAX25561 features an I^2C, two-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL).

SDA and SCL facilitate communication between the device and the controller at clock rates up to 400kHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 1 shows the two-wire interface timing diagram.

A controller device communicates with the device by transmitting the correct address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The SDA line operates as both an input and an open-drain output. A pull-up resistor greater than 500Ω is required on the SDA bus. The SCL line operates as an input only. A pull-up resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the STOP and START Conditions section). SDA and SCL idle high when the I^2C bus is not busy.

STOP and START Conditions

A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 8). A START (S) condition from the controller signals the beginning of a transmission to the device. The controller terminates transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Condition

The MAX25561 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line, a process that is typically called clock stretching. The MAX25561 does not use clock stretching to hold down the clock line.

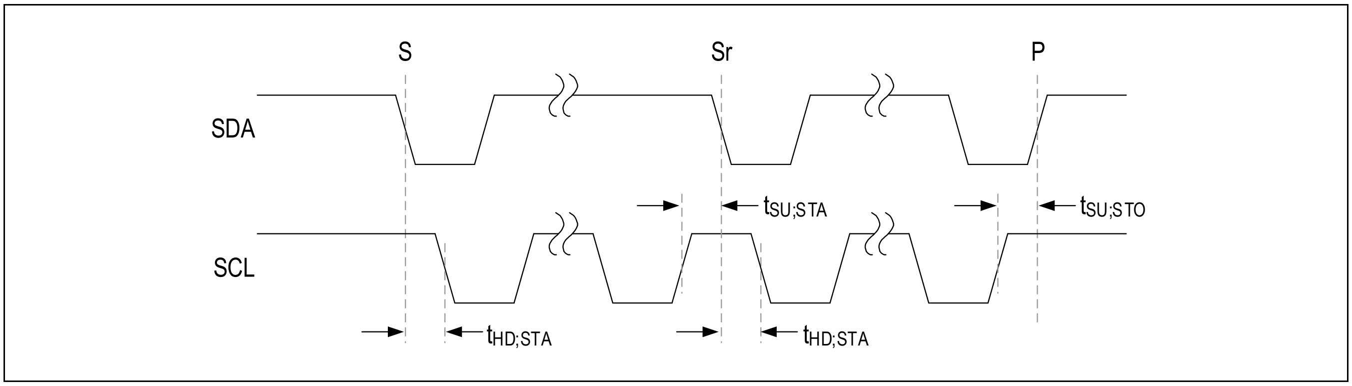


Figure 8. START, STOP, and REPEATED START Conditions

I²C General Call Address

The IC does not implement the I²C specification's general call address. The device will not issue an acknowledge to the general call address (0b0000_0000).

Packet Error Checking (PEC)

In order to increase fault coverage on the I²C interface, an optional PEC byte is supported. The PEC is enabled by setting the PEC_EN bit in the SET_REG register to 1. This follows the SMBus 3.0 implementation, which has a CRC-8 polynomial of $x^8 + x^2 + x + 1$. If the PEC byte is enabled and a supervisor system attempts to read more than 2 bytes (one data and one PEC) from the IC in a single communication packet, the IC will return 0xFF for the remaining bytes read. If a controller device transmits a byte and an incorrect PEC, the IC will reply with a NACK and discard the attempted write.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the device uses to handshake receipt of each byte of data (see *Figure 3*). The device pulls down SDA during the controller-generated ninth clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller can reattempt communication. Transmitting an incorrect PEC byte to the device (when PEC is enabled) will also result in a NACK from the IC (in addition, the PEC_ERR bit is set to 1 and FLTB is asserted low if the PEC_ERRMASK bit is 0).

Target Address

The I²C addresses are shown in *Table 3*.

Table 3. I²C Addresses

ADD PIN CONNECTION	7-BIT ADDRESS	8-BIT READ ADDRESS	8-BIT WRITE ADDRESS
GND	0x27	0x4F	0x4E
V18	0x2F	0x5F	0x5E

The address is defined as the 7 most significant bits (MSbs) followed by the R/W bit. Set the R/W bit to 1 to configure the device to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Write-Data Format

A write to the device includes transmission of a START condition, the target address with the R/W bit set to 0, one byte of data to register address, one to eight bytes of data to write to registers, and a STOP condition. *Figure 9* illustrates the proper format for one frame. If multiple bytes are transmitted, they are written to sequential registers starting at the register address transmitted. If the register address for the write reaches the end of the valid address space, the target register pointer will stay at the last valid register. If the write starts out-of-bounds, then all the bytes written will be discarded and the IC will return a NACK for each byte transmitted.

Read-Data Format

A read from the device includes the following:

- Transmission of a START condition
- Target address with the R/W bit set to 0
- 1 byte of data to register address
- Restart condition
- Target address with R/W bit set to 1
- 1-8 bytes written by the IC
- STOP condition

Figure 9 illustrates the correct frame format. The controller device must acknowledge each byte received and provide a NACK at the last byte read.

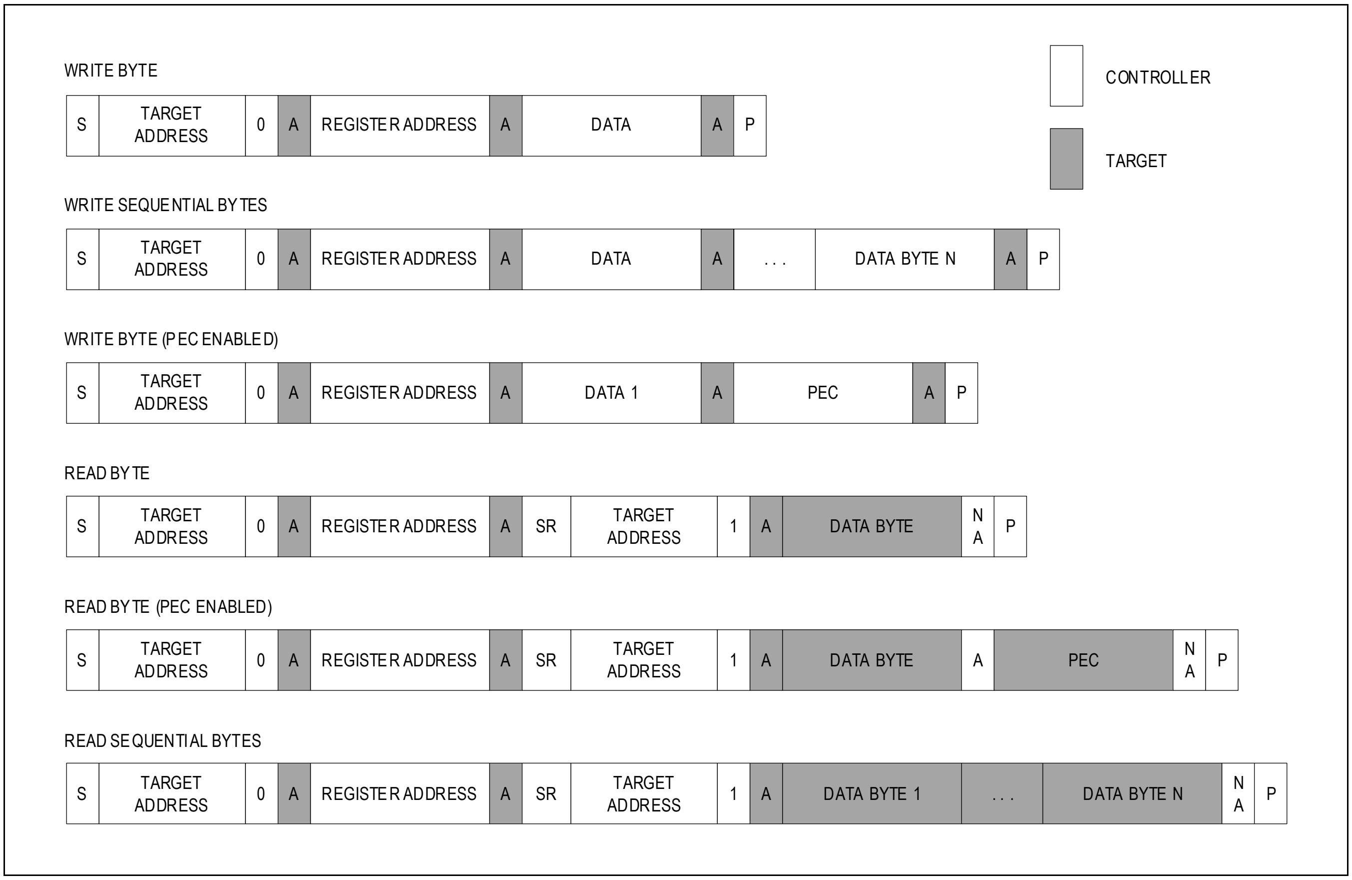


Figure 9. Data Format of I^2C Interface

Register Map

{{max_num}}

ADDRESS	NAME	MSB							LSB
USER_REGISTERS									

ADDRESS	**NAME**	**MSB**							**LSB**
0x00	DEV_ID_REG[7:0]	DEV_ID[7:0]							
0x01	REV_ID_REG[7:0]	–	–	–	–	REV_ID[3:0]			
0x02	SET_REG[7:0]	–	–	PEC_EN	BL_ILIM	BSTFORCE	FAST_SS	ENA	PSEN
0x03	IMODE_REG[7:0]	–	–	–	DIS_ISNS_SD	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
0x04	ISET_REG[7:0]	–	iset[6:0]						
0x05	TON1H_REG[7:0]	TON1H[7:0]							
0x06	TON1L_REG[7:0]	TON1L[7:0]							
0x07	TON2H_REG[7:0]	TON2H[7:0]							
0x08	TON2L_REG[7:0]	TON2L[7:0]							
0x09	TON3H_REG[7:0]	TON3H[7:0]							
0x0A	TON3L_REG[7:0]	TON3L[7:0]							
0x0B	TON4H_REG[7:0]	TON4H[7:0]							
0x0C	TON4L_REG[7:0]	TON4L[7:0]							
0x0D	TON1_4LSB_REG[7:0]	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
0x0E	TON5H_REG[7:0]	TON5H[7:0]							
0x0F	TON5L_REG[7:0]	TON5L[7:0]							
0x10	TON6H_REG[7:0]	TON6H[7:0]							
0x11	TON6L_REG[7:0]	TON6L[7:0]							
0x12	TON5_6LSB_REG[7:0]	–	–	–	TON_ALL	TON6LSB[1:0]		TON5LSB[1:0]	
0x13	SETTING_REG[7:0]	MM_MODE	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
0x14	DISABLE_REG[7:0]	–	–	CP_DIS	DIS6	DIS5	DIS4	DIS3	DIS2
0x15	FADING_REG[7:0]	–	–	–	FADE_GAIN	FADE_IN_OUT	TDIM[2:0]		
0x16	LO_DIM[7:0]	–	–	LO_DIM6	LO_DIM5	LO_DIM4	LO_DIM3	LO_DIM2	LO_DIM1

ADDRESS	NAME	MSB							LSB
0x17	OPEN_REG[7:0]	–	–	OUT6O	OUT5O	OUT4O	OUT3O	OUT2O	OUT1O
0x18	SHORTGND_REG[7:0]	–	–	OUT6SG	OUT5SG	OUT4SG	OUT3SG	OUT2SG	OUT1SG
0x19	SHORTED_LED_REG[7:0]	–	–	OUT6SL	OUT5SL	OUT4SL	OUT3SL	OUT2SL	OUT1SL
0x1A	MASK1_REG[7:0]	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
0x1B	MASK2_REG[7:0]	TON_MM_MASK	PEC_ERRMASK	BATT_UVMASK	I_MM_MASK	–	–	–	–
0x1C	DIAG1_REG[7:0]	RTOOR	ISETOOR	IREFOOR	BSTUV	BSTOV	HW_RST	OTW	OT
0x1D	DIAG2_REG[7:0]	V18OOR	PEC_ERR	BATT_UV	CLK_ERR	V5OOR	VREFOOR	NV_FLT	ISNS_SD
0x1E	I_MISMATCH[7:0]	–	–	I_MM6	I_MM5	I_MM4	I_MM3	I_MM2	I_MM1
0x1F	TON_MISMATCH[7:0]	–	–	TON6_MM	TON5_MM	TON4_MM	TON3_MM	TON2_MM	TON1_MM
0x20	MM_DIS[7:0]	I_MM_DIS	TON_MM_DIS	TON6_MM_DIS	TON5_MM_DIS	TON4_MM_DIS	TON3_MM_DIS	TON2_MM_DIS	TON1_MM_DIS
0x21	VBSTMON[7:0]	vbstmon[7:0]							
0x22	IOUT1[7:0]	iout1[7:0]							
0x23	IOUT2[7:0]	iout2[7:0]							
0x24	IOUT3[7:0]	iout3[7:0]							
0x25	IOUT4[7:0]	iout4[7:0]							
0x26	IOUT5[7:0]	iout5[7:0]							
0x27	IOUT6[7:0]	iout6[7:0]							
0x28	VSENSE[7:0]	vsense[7:0]							
0x29	DIM_TON_HI[7:0]	dim_ton_hi[7:0]							
0x2A	DIM_TON_MID[7:0]	dim_ton_mid[7:0]							
0x2B	DIM_TON_LO[7:0]	–	–	–	–	–	–	dim_ton_lo[1:0]	
0x2C	DIM_F_HI[7:0]	dim_f_hi[7:0]							
0x2D	DIM_F_MID[7:0]	dim_f_mid[7:0]							

ADDRESS	NAME	MSB							LSB
0x2E	DIM_F_LO[7:0]	–	–	–	–	–	–	dim_f_lo[1:0]	

Register Details

DEV_ID_REG (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEV_ID	7:0	Device ID {{devid}}

REV_ID_REG (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REV_ID[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
REV_ID	3:0	Device revision ID.

SET_REG (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PEC_EN	BL_ILIM	BSTFORCE	FAST_SS	ENA	PSEN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PEC_EN	5	When 1, PEC is enabled on I^{2}C transactions.	
BL_ILIM	4	Sets boost current limit to one of two levels. When 0, the higher current limit is selected.	0x0: Current limit set high 0x1: Current limit set low
BSTFORCE	3	When 1, this bit forces the boost converter to run continuously and independently of the dimming signal.	
FAST_SS	2	Selects slow or fast boost soft-start. Set to 1 for fast soft-start.	
ENA	1	Boost converter and LED outputs enable bit. Set to 1 to enable the device.	
PSEN	0	When 0, phase shifting is disabled. When 1, phase shifting is enabled.	

IMODE_REG (0x3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DIS_ISNS_SD	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
Reset	–	–	–	0x0	0b1	0b0	0b00	
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>DIS_ISNS_SD</td><td>4</td><td>When 1, this bit disables the input overcurrent shutdown function. When an overcurrent is detected, the ISNS_SD bit is asserted, but the device continues operation and FLTB does not assert low.</td></tr>
<tr><td>DIM_EXT</td><td>3</td><td>When 1, dimming through the DIM pin is enabled. When 0, dimming is controlled using the TON__ registers.</td></tr>
<tr><td>HDIM</td><td>2</td><td>When 1, hybrid dimming is enabled.</td></tr>
<tr><td>HDIM_THR_1_0</td><td>1:0</td><td>Set hybrid dimming threshold.
<table>
<tr><td>00</td><td>6.25%</td></tr>
<tr><td>10</td><td>12.5%</td></tr>
<tr><td>10</td><td>25%</td></tr>
<tr><td>11</td><td>50%</td></tr>
</table>
</td></tr>
</table>

ISET_REG (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	iset[6:0]						
Reset	–	0b0001000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
iset	6:0	The value in this register sets the OUT_ LED current in the range 93mA to 220mA.	0x00: 34.5mA 0x01: 36mA ...: ... 0x2B: 99mA 0x2C: 100.5mA 0x2D: 102mA ...: ... 0x7D: 222mA 0x7E: 223.5mA 0x7F: 225mA

TON1H_REG (0x5)

On-time setting for channel 1 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1H	7:0	High byte of 18-bit TON setting for channel 1.

TON1L_REG (0x6)

On-time setting for channel 1 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1L	7:0	Middle byte of 18-bit TON setting for channel 1.

TON2H_REG (0x7)

On-time setting for channel 2 with 50ns resolution2, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2H	7:0	High byte of 18-bit TON setting for channel 2.

TON2L_REG (0x8)

On-time setting for channel 2 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2L	7:0	Middle byte of 18-bit TON setting for channel 2.

TON3H_REG (0x9)

On-time setting for channel 3 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3H	7:0	High byte of 18-bit TON setting for channel 3.

TON3L_REG (0xA)

On-time setting for channel 3 with 50ns resolution, middle byte.

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON3L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3L	7:0	Middle byte of 18-bit TON setting for channel 3.

TON4H_REG (0xB)

On-time setting for channel 4 with 50ns resolution, high byte.

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON4H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4H	7:0	High byte of 18-bit TON setting for channel 4.

TON4L_REG (0xC)

On-time setting for channel 4 with 50ns resolution, middle byte.

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON4L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4L	7:0	Middle byte of 18-bit TON setting for channel 4.

TON1_4LSB_REG (0xD)

LSBs of on-time setting for all channels with 50ns resolution.

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
Reset	0b11		0b11		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
TON4LSB	7:6	2 least significant bits of 18-bit TON setting for channel 4.
TON3LSB	5:4	2 least significant bits of 18-bit TON setting for channel 3.
TON2LSB	3:2	2 least significant bits of 18-bit TON setting for channel 2.
TON1LSB	1:0	2 least significant bits of 18-bit TON setting for channel 1.

TON5H_REG (0xE)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON5H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON5H	7:0	High byte of 18-bit TON setting for channel 5.

TON5L_REG (0xF)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TON5L[7:0]							
Reset	0xFF							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
TON5L	7:0	Middle byte of 18-bit TON setting for channel 5.

TON6H_REG (0x10)

BIT	7	6	5	4	3	2	1	0
Field	TON6H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON6H	7:0	High byte of 18-bit TON setting for channel 6.

TON6L_REG (0x11)

BIT	7	6	5	4	3	2	1	0
Field	TON6L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON6L	7:0	Middle byte of 18-bit TON setting for channel 6.

TON5_6LSB_REG (0x12)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TON_ALL	TON6LSB[1:0]		TON5LSB[1:0]	
Reset	–	–	–	0b0	0b11		0b11	
Access Type	–	–	–	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
TON_ALL	4	When 1, this bit causes the TON1 value to be used for all active channels.
TON6LSB	3:2	2 least significant bits of 18-bit TON setting for channel 6.
TON5LSB	1:0	2 least significant bits of 18-bit TON setting for channel 5.

SETTING_REG (0x13)

BIT	7	6	5	4	3	2	1	0
Field	MM_MODE	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
Reset	0b0	0b001			0b0	0b0	0b00	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>MM_MODE</td><td>7</td><td>This bit determines the device behavior when either a TON or a current mismatch is detected on any of the active channels.</td><td>0x0: Assert FLTB output low.
0x1: Assert FLTB output low and turn off boost converter and OUT1-6 current sinks.</td></tr>
<tr><td>FPWM</td><td>6:4</td><td>These bits set the PWM frequency in internal PWM mode.
<table>
<tr><th>FPWM2</th><th>FPWM1</th><th>FPWM0</th><th>PWM FREQUENCY (Hz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>153</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>203</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>305</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>610</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>980</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1220</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1401</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1634</td></tr>
</table></td><td></td></tr>
<tr><td>SS_OFF</td><td>3</td><td>When 1, spread-spectrum switching is disabled. Default value is 0.</td><td></td></tr>
<tr><td>SSL</td><td>2</td><td>When spread spectrum is enabled, the SSL bit sets the level of spread. When 0, the spread is nominally ±6%. When 1, the spread is ±3%. When changing the percentage, disable spread spectrum using the SS_OFF bit first. Then, change the value of SSL. Finally, reenable spread spectrum using SS_OFF.</td><td></td></tr>
<tr><td>SLDET</td><td>1:0</td><td>Shorted-LED threshold Settings.</td><td></td></tr>
</table>

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td></td><td></td><td><table><tr><td>00</td><td>8V</td></tr><tr><td>01</td><td>3V</td></tr><tr><td>10</td><td>6V</td></tr><tr><td>11</td><td>8V</td></tr></table></td><td></td></tr>
</table>

DISABLE_REG (0x14)

Channel-disable bits.

BIT	7	6	5	4	3	2	1	0
Field	–	–	CP_DIS	DIS6	DIS5	DIS4	DIS3	DIS2
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CP_DIS	5	When 1, this bit disables the internal charge pump which drives the NGATE pin. Set to 1 when an external series switch is not used. Setting CP_DIS to zero during operation will cause complete shutdown of the device and is not recommended.
DIS6	4	Set bit to 1 to disable OUT6. This must be done before ENA is written to 1.
DIS5	3	Set bit to 1 to disable OUT5. This must be done before ENA is written to 1.
DIS4	2	Set bit to 1 to disable OUT4. This must be done before ENA is written to 1.
DIS3	1	Set bit to 1 to disable OUT3. This must be done before ENA is written to 1.
DIS2	0	Set bit to 1 to disable OUT2. This must be done before ENA is written to 1.

FADING_REG (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FADE_GAIN	FADE_IN_OUT	TDIM[2:0]		
Reset	–	–	–	0b0	0b0	0b000		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_GAIN	4	When this bit is set to 1, the fade-in-out function has a gain of 12.5%, otherwise 6.25%.	
FADE_IN_OUT	3	When this bit is set to 1, the fade-in-out function for the LED dimming is enabled.	
TDIM	2:0	Sets the fading update time interval according to 2^{TDIM}. TDIM can be between 0 and 5. When set to 0, fading is updated on every dimming cycle.	0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: N/A 0x7: N/A

LO_DIM (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LO_DIM6	LO_DIM5	LO_DIM4	LO_DIM3	LO_DIM2	LO_DIM1
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
LO_DIM6	5	When 1, indicates channel 6 is in low-dim mode.
LO_DIM5	4	When 1, indicates channel 5 is in low-dim mode.
LO_DIM4	3	When 1, indicates channel 4 is in low-dim mode.
LO_DIM3	2	When 1, indicates channel 3 is in low-dim mode.
LO_DIM2	1	When 1, indicates channel 2 is in low-dim mode.
LO_DIM1	0	When 1, indicates channel 1 is in low-dim mode.

OPEN_REG (0x17)

Open-string diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	OUT6O	OUT5O	OUT4O	OUT3O	OUT2O	OUT1O
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
OUT6O	5	If 1, an open is detected on channel 6.
OUT5O	4	If 1, an open is detected on channel 5.
OUT4O	3	If 1, an open is detected on channel 4.
OUT3O	2	If 1, an open is detected on channel 3.
OUT2O	1	If 1, an open is detected on channel 2.
OUT1O	0	If 1, an open is detected on channel 1.

SHORTGND_REG (0x18)

Short-to-ground diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	OUT6SG	OUT5SG	OUT4SG	OUT3SG	OUT2SG	OUT1SG
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
OUT6SG	5	If 1, a short-to-ground is detected on channel 6 at startup.
OUT5SG	4	If 1, a short-to-ground is detected on channel 5 at startup.
OUT4SG	3	If 1, a short-to-ground is detected on channel 4 at startup.
OUT3SG	2	If 1, a short-to-ground is detected on channel 3 at startup.
OUT2SG	1	If 1, a short-to-ground is detected on channel 2 at startup.
OUT1SG	0	If 1, a short-to-ground is detected on channel 1 at startup.

SHORTED_LED_REG (0x19)

Shorted-LED diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	OUT6SL	OUT5SL	OUT4SL	OUT3SL	OUT2SL	OUT1SL
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
OUT6SL	5	If 1, a shorted-LED condition is detected on channel 6.
OUT5SL	4	If 1, a shorted-LED condition is detected on channel 5.
OUT4SL	3	If 1, a shorted-LED condition is detected on channel 4.
OUT3SL	2	If 1, a shorted-LED condition is detected on channel 3.
OUT2SL	1	If 1, a shorted-LED condition is detected on channel 2.
OUT1SL	0	If 1, a shorted-LED condition is detected on channel 1.

MASK1_REG (0x1A)

Mask register for the FLTB pin.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
Reset	–	–	–	0b0	0b0	0b0	0b1	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTUVMASK	4	When 1, a boost undervoltage fault does not cause the FLTB pin to assert low.
OMASK	3	When 1, an open-LED fault does not cause the FLTB pin to assert low.
SGMASK	2	When 1, a short-to-ground LED fault does not cause the FLTB pin to assert low.
OTWMASK	1	When 1, an overtemperature warning does not cause the FLTB pin to assert low.
SLMASK	0	When 1, a shorted-LED fault does not cause the FLTB pin to assert low.

MASK2_REG (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	TON_MM_MASK	PEC_ERRMASK	BATT_UVMASK	I_MM_MASK	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION
TON_MM_MASK	7	When 1, a TON mismatch does not cause FLTB to assert low.
PEC_ERRMASK	6	When 1, an interface parity error does not cause FLTB to assert low.
BATT_UVMASK	5	When 1, an undervoltage on BATT does not cause FLTB to assert low.
I_MM_MASK	4	When 1, an OUT_ current mismatch does not cause FLTB to assert low.

DIAG1_REG (0x1C)

Boost state, overtemperature-warning/shutdown diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	RTOOR	ISETOOR	IREFOOR	BSTUV	BSTOV	HW_RST	OTW	OT
Reset	0b0	0x0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Read Clears All	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
RTOOR	7	This bit is set to 1 if the resistor on the RT pin is out of the expected range. When this happens, the device cannot operate.
ISETOOR	6	When 1, this bit indicates a short to ground on ISET. In this condition, the device does not operate. Power must be recycled to restart the device.
IREFOOR	5	When 1, this bit indicates that the IREF current is out of range. This is more than likely due to an incorrect resistor value on ISET. In this condition, the IC stops operation.
BSTUV	4	If 1, an undervoltage is detected on the boost output, and the boost is disabled.
BSTOV	3	If 1, the boost converter is at its overvoltage limit.
HW_RST	2	If 1, the device has just emerged from a hardware reset (power-up). This bit is reset after the first read from this register.
OTW	1	If 1, the junction temperature of the device is over T_{WARN}, or the temperature foldback circuit has reached the temperature T1.
OT	0	If 1, the junction temperature of the device has exceeded T_{SHDN} or the TEMP input reached the level which shuts off the LED currents.

DIAG2_REG (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	V18OOR	PEC_ERR	BATT_UV	CLK_ERR	V5OOR	VREFOOR	NV_FLT	ISNS_SD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0x0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Clears All	Read Clears All	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION
V18OOR	7	When 1, this bit indicates that the 1.8V regulator output is not in range.
PEC_ERR	6	When 1, this bit indicates an I²C communication parity error.
BATT_UV	5	When 1, this bit indicates that the BATT input is below the V_{BATT_LVF} level.
CLK_ERR	4	When this bit is 1, the internal clock has been inactive for 1µs or is out-of-range. When this fault occurs, the FLTB pin asserts low and the local host should disable the device using the EN pin. This fault can only be cleared by power-on reset (POR).
V5OOR	3	When 1, this bit indicates that the V5 supply is out of range and that the device was shut down as a consequence.
VREFOOR	2	When 1, this bit indicates a mismatch between bandgap references.
NV_FLT	1	When 1, this bit indicates a fault in the internal device nonvolatile memory. If this fault occurs, FLTB is asserted low and the device does not operate.
ISNS_SD	0	When 1, this bit indicates that the voltage between the BATT and SENSE pins exceeded 200mV and the boost converter was disabled unless DIS_ISNS_SD was set to 1.

I_MISMATCH (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	I_MM6	I_MM5	I_MM4	I_MM3	I_MM2	I_MM1
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
I_MM6	5	When 1, this bit indicates that the measured current in channel 6 does not match the iset[6:0] setting.

BITFIELD	BITS	DESCRIPTION
I_MM5	4	When 1, this bit indicates that the measured current in channel 5 does not match the iset[6:0] setting.
I_MM4	3	When 1, this bit indicates that the measured current in channel 4 does not match the iset[6:0] setting.
I_MM3	2	When 1, this bit indicates that the measured current in channel 3 does not match the iset[6:0] setting.
I_MM2	1	When 1, this bit indicates that the measured current in channel 2 does not match the iset[6:0] setting.
I_MM1	0	When 1, this bit indicates that the measured current in channel 1 does not match the iset[6:0] setting.

TON_MISMATCH (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TON6_MM	TON5_MM	TON4_MM	TON3_MM	TON2_MM	TON1_MM
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
TON6_MM	5	When 1, this bit indicates a TON mismatch on OUT6.
TON5_MM	4	When 1, this bit indicates a TON mismatch on OUT5.
TON4_MM	3	When 1, this bit indicates a TON mismatch on OUT4.
TON3_MM	2	When 1, this bit indicates a TON mismatch on OUT3.
TON2_MM	1	When 1, this bit indicates a TON mismatch on OUT2.
TON1_MM	0	When 1, this bit indicates a TON mismatch on OUT1.

MM_DIS (0x20)

BIT	7	6	5	4	3	2	1	0
Field	I_MM_DIS	TON_MM_DIS	TON6_MM_DIS	TON5_MM_DIS	TON4_MM_DIS	TON3_MM_DIS	TON2_MM_DIS	TON1_MM_DIS
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
I_MM_DIS	7	When 1, this bit disables the current mismatch check.
TON_MM_DIS	6	When 1, this bit disables the TON mismatch check on all active channels.
TON6_MM_DIS	5	When 1, this bit disables the TON mismatch check on OUT6.
TON5_MM_DIS	4	When 1, this bit disables the TON mismatch check on OUT5.
TON4_MM_DIS	3	When 1, this bit disables the TON mismatch check on OUT4.
TON3_MM_DIS	2	When 1, this bit disables the TON mismatch check on OUT3.
TON2_MM_DIS	1	When 1, this bit disables the TON mismatch check on OUT2.
TON1_MM_DIS	0	When 1, this bit disables the TON mismatch check on OUT1.

VBSTMON (0x21)

BIT	7	6	5	4	3	2	1	0
Field	vbstmon[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
vbstmon	7:0	BSTMON voltage measurement from internal ADC.

IOUT1 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	iout1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout1	7:0	OUT1 current measurement from internal ADC.

IOUT2 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	iout2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout2	7:0	OUT2 current measurement from internal ADC.

IOUT3 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	iout3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout3	7:0	OUT3 current measurement from internal ADC.

IOUT4 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	iout4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout4	7:0	OUT4 current measurement from internal ADC.

IOUT5 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	iout5[7:0]							

Reset	0x00
Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
iout5	7:0	OUT5 current measurement from internal ADC.

IOUT6 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	iout6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout6	7:0	OUT6 current measurement from internal ADC.

VSENSE (0x28)

BIT	7	6	5	4	3	2	1	0
Field	vsense[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
vsense	7:0	ADC result of conversion of voltage between BATT and SENSE pins.

DIM_TON_HI (0x29)

BIT	7	6	5	4	3	2	1	0
Field	dim_ton_hi[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
dim_ton_hi	7:0	High byte of measured on-time value at DIM pin in units of 50ns. This value is 0 when internal dimming is used.

DIM_TON_MID (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	dim_ton_mid[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
dim_ton_mid	7:0	Middle byte of measured on-time value at DIM pin in units of 50ns. This value is 0 when internal dimming is used.

DIM_TON_LO (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	dim_ton_lo[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION
dim_ton_lo	1:0	Least-significant bits of measured on-time value at DIM pin in units of 50ns. This value is 0 when internal dimming is used.

DIM_F_HI (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	dim_f_hi[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
dim_f_hi	7:0	High byte of measured frequency value at DIM pin in units of 50ns. At 100% and 0% brightness, the frequency read is approximately 80Hz. The value is 0 when internal dimming is used.

DIM_F_MID (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	dim_f_mid[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
dim_f_mid	7:0	Middle byte of measured frequency value at DIM pin in units of 50ns. At 100% and 0% brightness, the frequency read is approximately 80Hz. The value is 0 when internal dimming is used.

DIM_F_LO (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	dim_f_lo[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Read Only	

BITFIELD	BITS	DESCRIPTION
dim_f_lo	1:0	Least-significant bits of measured frequency value at DIM pin in units of 50ns. At 100% and 0% brightness, the frequency read is approximately 80Hz. The value is 0 when internal dimming is used.

Applications Information

Power-Circuit Design

First select a converter topology based on whether the total converter output voltage (LED string forward voltage + OUT_ headroom) is higher than the maximum input voltage, in which case the boost topology can be used. Otherwise, select the SEPIC configuration. Determine the total output current needed to drive the LED strings (I_{LED}) using the following equation:

$I_{LED} = I_{STRING} \times N_{STRING}$

where I_{STRING} is the LED current per string in amperes and N_{STRING} is the number of strings used. Calculate the maximum duty cycle (D_{MAX}) using the following equations:

Boost Configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN\_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.44)}$$

SEPIC Configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1})}{(V_{IN\_MIN} - V_{DS} - 0.44 + V_{LED} + V_{D1})}$$

where V_{D1} is the forward drop of the rectifier diode in volts (approximately 0.6V), V_{IN_MIN} is the minimum input supply voltage in volts, V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on, and 0.44V is the peak current-sense voltage in the high-current setting. Initially, use an approximate value of 0.2V for V_{DS} to calculate D_{MAX}. Calculate a more accurate value of D_{MAX} after the power MOSFET is selected based on the maximum inductor current.

Boost Configuration

The average inductor current varies with the input voltage, and the maximum average current occurs at the lowest input voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum desired peak-to-peak ripple on the inductor current (ΔI_L). The recommended peak-to-peak ripple is 60% of the average inductor current.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes.

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔI_L to be ±30% of the average inductor current:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

and

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

Calculate the minimum inductance value (L_{MIN}), in henries with the inductor-current ripple set to the maximum value.

$$L_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.44) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where 0.44V is the peak current-sense voltage (with bl_ilim set to 0; if bl_ilim is set to 1, use 0.325V in this equation). Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and a current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for the boost configuration.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a boost design. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see the *Typical Application Circuit*). One of the inductors (L2) has the LED current as the average current, and the other inductor (L1) has the input current as its average current. Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔI_L is ±30% of the average inductor current:

$$\Delta I_{L1} = IL1_{AVG} \times 0.3 \times 2$$

and

$$IL1_P = IL1_{AVG} + \frac{\Delta I_{L1}}{2}$$

$$\Delta I_{L2} = IL2_{AVG} \times 0.3 \times 2$$

and

$$IL2_P = IL2_{AVG} + \frac{\Delta I_{L2}}{2}$$

Calculate the minimum inductance values $L1_{MIN}$ and $L2_{MIN}$ in henries with the inductor current ripples set to the maximum value as follows:

$$L1_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.44) \times D_{MAX}}{f_{SW} \times \Delta I_{L1}}$$

$$L2_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.44) \times D_{MAX}}{f_{SW} \times \Delta I_{L2}}$$

where 0.44V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$, and current ratings greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

To simplify further calculations, consider L1 and L2 as a single inductor with L1/L2 connected in parallel. The combined inductance value and current is calculated as follows:

$$L_{MIN} = \frac{L1_{MIN} \times L2_{MIN}}{L1_{MIN} + L2_{MIN}}$$

and

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors, connected together for SEPIC configuration. Use these values in the calculations for the SEPIC configuration in the following sections. Select coupling capacitor CS so that its peak-to-peak ripple is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series resonant circuit comprising L1, CS, and L2 do not affect the operation of the converter. Use the following equation to calculate the minimum value of CS:

$$CS \geq \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where CS is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, and the factor 0.02 reflects the desired 2% ripple.

Current-Sense Resistor and Slope Compensation

The MAX25561 backlight controller generates a current ramp for slope compensation. This ramp current is synchronized to the switching frequency, starting from zero at the beginning of every clock cycle and rising linearly to reach 50μA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CSP input and the source of the external MOSFET. This adds a programmable ramp voltage to the CSP input voltage to provide slope compensation.

Use the following equations to calculate the value of slope-compensation resistance (R_{SC}):

Boost Configuration:

$$R_{SC}=\frac{\left(V_{LED}-2\times V_{IN\_MIN}\right)\times R_{CS}\times 3}{L_{MIN}\times 50\mu A\times f_{SW}\times 4}$$

SEPIC and Coupled-Inductor Configurations:

$$R_{SC}=\frac{\left(V_{LED}-V_{IN\_MIN}\right)\times R_{CS}\times 3}{L_{MIN}\times 50\mu A\times f_{SW}\times 4}$$

where V_{LED} and V_{IN_MIN} are in volts, R_{SC} and R_{CS} are in ohms, L_{MIN} is in henries, and f_{SW} is in hertz. The value of the switch current-sense resistor (R_{CS}) can be calculated as follows:

Boost Configuration:

$$R_{CS}=\frac{4\times L_{MIN}\times f_{SW}\times V_{CS\_MAX}\times 0.9}{I_{LP}\times 4\times L_{MIN}\times f_{SW}+D_{MAX}\times\left(V_{LED}-2\times V_{IN\_MIN}\right)\times 3}$$

SEPIC and Coupled-Inductor Configurations:

$$R_{CS}=\frac{4\times L_{MIN}\times f_{SW}\times V_{CS\_MAX}\times 0.9}{I_{LP}\times 4\times L_{MIN}\times f_{SW}+D_{MAX}\times\left(V_{LED}-V_{IN\_MIN}\right)\times 3}$$

where V_{CS_MAX} is the minimum value of the peak current-sense threshold or 0.38V with bl_ilim = 0 and 0.275V when bl_ilim is set to 1. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

In both converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED string voltages are stable due to their constant current. For the MAX25561, limit the peak-to-peak output-voltage ripple to 250mV in order to get stable output current.

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects, connecting multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming however, it may be desirable to limit the use of ceramic capacitors on the boost output. In such cases, an additional electrolytic or tantalum capacitor can provide the majority of the bulk capacitance.

External Switching MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum boost output voltage together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductance and capacitance. The recommended MOSFET V_{DS} voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The continuous drain-current rating of the MOSFET (ID), when the case temperature is at the maximum operating ambient temperature, should be greater than that calculated below.

$$ID_{RMS}=\left(\sqrt{{IL_{AVG}}^{2}\times D_{MAX}}\right)\times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET.

$$P_{COND}=IL^{2}_{AVG}\times D_{MAX}\times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state, drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET:

$$P_{SW}=\frac{IL_{AVG}\times {V_{LED}}^{2}\times C_{GD}\times f_{SW}}{2}\times\left(\frac{1}{I_{GON}}+\frac{1}{I_{GOFF}}\right)$$

where I_{GON} and I_{GOFF} are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a diode with a voltage rating that is 20% higher than the maximum boost-converter output voltage and a current rating greater than:

$$I_D = IL_{AVG} \times (1 - D_{MAX}) \times 1.2$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.78V and 1.03V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the previous boost output-voltage value for use during the next on cycle. The switching converter small-signal-transfer function has a right-half plane (RHP) zero in the boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate.

Worst-Case RHP Zero Frequency (f_{ZRHP}):

$$f_{ZRHP} = V_{LED} \times \frac{(1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED}}$$

SEPIC and Coupled-Inductor Configurations:

$$f_{ZRHP} = V_{LED} \times \frac{(1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

The standard way to avoid this zero is to roll off the loop gain to 0dB at a frequency of less than 1/5 of the RHP zero frequency with a -20dB/decade slope. The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}) that is calculated as follows:

Boost Configuration:

$$f_{P1} = \frac{I_{LED}}{\pi \times V_{LED} \times C_{OUT}}$$

SEPIC and Coupled-Inductor Configurations:

$$f_{P1} = I_{LED} \times \frac{D_{MAX}}{\pi \times V_{LED} \times C_{OUT}}$$

Compensation components RCOMP and CCOMP perform two functions. CCOMP introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. RCOMP flattens the gain of the error amplifier for frequencies above the zero formed by RCOMP and CCOMP. For compensation, this zero is placed at f_{P1} to provide a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response. The value of RCOMP needed to fix the total loop gain at f_{P1} so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency is calculated as follows:

Boost Configuration:

$$R_{COMP} = f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}/(5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX}))$$

SEPIC and Coupled-Inductor Buck-Boost Configurations:

$$R_{COMP} = f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP} \times D_{MAX}/(5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX}))$$

where:

- R_{COMP} = Compensation resistor in Ω
- A_{OVP} = BSTMON resistor-divider gain (a value >> 1)
- R_{CS} = Current-sense resistor in Ω

- GM_{COMP} = Transconductance of the error amplifier (600µS)

The value of CCOMP is calculated as follows:

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{Z1} \times R_{COMP}}$$

where f_{Z1} is the compensation zero placed at 1/5 the crossover frequency, which is, in turn, set at 1/5 the f_{ZRHP}.

If the output capacitors do not have low ESR, the ESR zero frequency could fall below the 0dB crossover frequency. An additional pole may be required to cancel out this zero placed at the same frequency. This can be added by connecting a capacitor from the COMP pin directly to GND with a value shown as follows:

$$C_{PAR} = GM_{COMP} \times R_{ESR} \times C_{OUT}$$

where R_{ESR} is the capacitor ESR value and C_{OUT} is the output-capacitor value.

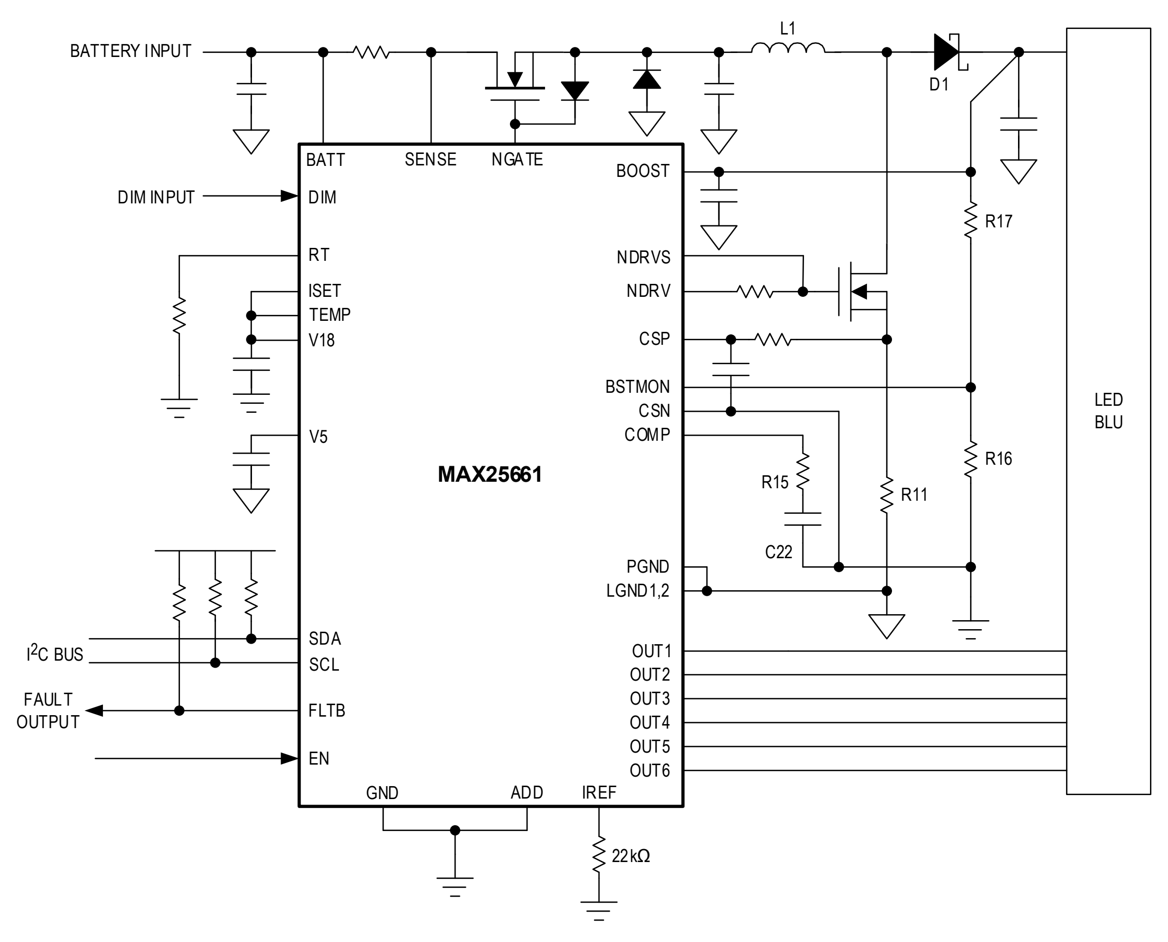
PCB Layout Considerations

The MAX25561 incorporates a high-frequency switching converter and, as such, careful circuit board layout is required to ensure correct device operation and optimize EMI performance. The switching-converter portion of the circuit contains nodes with very fast voltage transients, which could lead to undesirable effects on the sensitive parts of the circuit. Observe the following guidelines when designing a circuit board for the MAX25561:

1. Make the connections from the sense resistor to the BATT and SENSE pins as short and as wide as possible. This ensures a low-resistance connection, which enhances sensing accuracy.
2. Connect the components related to the following pins as close as possible to the device to avoid noise pickup: ISET, RT, BSTMON, and COMP. Connect their ground terminals to an analog ground plane or directly to the device GND pin. The CSN pin should be connected directly to the ground of the network connected to COMP.
3. Connect the bypass capacitors on V18 as close as possible to the device, and connect the capacitor ground to the nearest GND pin. Connect the GND of the device to the analog ground plane using a via placed close to GND.
4. Connect the bypass capacitors on V5 as close as possible to the device, and connect the capacitor ground to power GND.
5. Have a power-ground plane for the switching-converter power circuit under the power components (i.e., input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane closest to PGND. Connect all other ground connections to the power ground plane using vias placed close to the terminals.
6. There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on (from the input filter capacitor positive terminal, through the inductor, the internal MOSFET, and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power-ground plane for the switching currents on the top-layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.
7. Connect the power-ground plane for the constant-current LED-driver portion of the circuit to LEDGND as close as possible to the device. Connect GND to PGND at the same point.
8. Boost output voltage for the LED strings should be taken directly from the output capacitors and not from the boost diode anode.
9. Input and output capacitors need good grounding with wide traces and multiple vias to the ground plane.

Typical Application Circuit

Boost Configuration



Ordering Information

PART	TEMP RANGE	PACKAGE CODE	PIN-PACKAGE
MAX25561ATJ/V+	-40°C to +125°C	T3255+6C	32-TQFN-EP*
MAX25561ATJ/VY+	-40°C to +125°C	T3255+6C	32-TQFN-EP*

/V Denotes an automotive-qualified part.
+ Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
Y = Side-wettable (SW) package.
T Denotes tape-and-reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Initial release	—