Data Sheet

LT7200S

18V, Quad ±5A/ Quad Phase ±20A Silent Switcher®2 Step-Down Regulator

FEATURES

- **Silent Switcher®2 Architecture:**
  - **Ultralow EMI**
  - **Eliminated PCB Layout Sensitivity**
  - **Internal Bypass Caps Reduce Radiated EMI**
- **SV_{IN} Range: 2.9V to 18V; PV_{IN}: 1.5V to 18V**
- **Wide V_{OUT} Range: 0.5V to 0.9V_{IN}**
- **Output Current: ±20A (±5A per Channel)**
- **Accurate Reference: 0.5V ± 0.8% Over Temp**
- **High Efficiency: Up to 96%**
- **12ns Min on-time: True 12V to 1V at 2MHz**
- **Programmable Multi-phase, Synchronizable Frequency: 400kHz to 3MHz**
- **Current Mode: Excellent Line and Load Transient Response**
- User Selectable Discontinuous Mode® (DCM) or Forced Continuous Mode (FCM) Operation
- Flexible Individual Internal Compensation for Ease of Use; External for Fast Transient
- Accurate Individual 1.2V EN/ Run Pin Threshold
- Individual Output Tracking and Soft-Start
- Individual Power Good Status Output
- Low Profile 5mm x 6mm 48-Lead LQFN Package

APPLICATIONS

- Distributed Power Systems, Server Power
- Point of Load Supply for ASIC, FPGA, Etc.

DESCRIPTION

The LT®7200S is a quad-channel, high efficiency monolithic synchronous buck regulator, capable of sinking/sourcing 5A to the load per channel. Its multi-channel flexibility is ideal for powering complex systems with the compact layout. The operating supply voltage range is from 2.9V to 18V, making it suitable for various supply applications from a 3.3V, 5V to 12V supply.

The operating frequency is programmable from 400kHz to 3MHz with an external resistor, or externally synchronized for switching noise sensitive applications. The unique “phase lockable, controlled on-time, constant frequency, current mode” architecture, is ideal for high frequency, high step-down applications while demanding fast transient responses. The high frequency capability allows smaller surface mount inductors and capacitors. The MODE/SYNC pin selects low noise Forced Continuous Mode (FCM) or high efficiency Discontinuous Mode (DCM). The PHMODE pin allows to run out-of-phase among 4 channels, which lessens the required input and output capacitors. The LT7200S uses second generation Silent Switcher technology with integrated bypass capacitors to deliver a highly efficient solution at high frequencies with excellent EMI performance.

TYPICAL APPLICATION

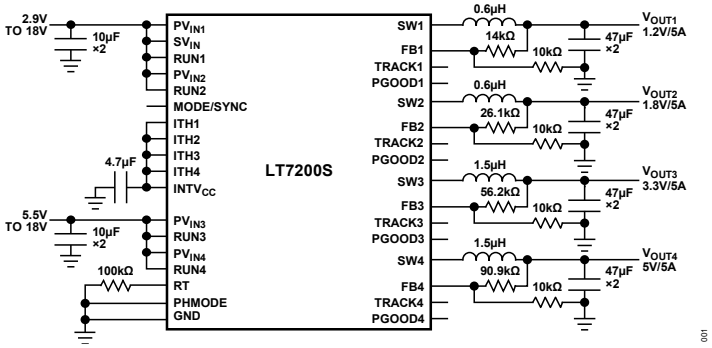

Figure 1. 1.2V/5A, 1.8V/5A, 3.3V/5A, 5V/5A (1MHz) Buck Regulator

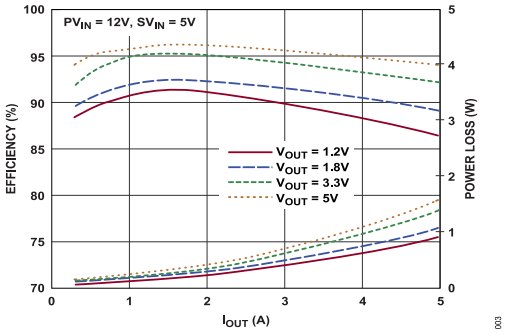

Figure 2. Efficiency and Power Loss (1MHz)

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REVISION HISTORY

Nature of Change	Page Number
10/2022 – REV 0	—
10/2023 – Rev 1 Updated Electrical Characteristics Updated Table 3	3, 4 7

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SV_{IN} Operating Voltage	SV_{IN}	-40°C ≤ T_J ≤ 125°C	2.9		18	V
PV_{IN} Operating Voltage	PV_{IN}		1.5		18	V
V_{OUT} Operating Voltage	V_{OUT}	R_{RT} = 100kΩ	0.5		$0.9V_{IN}$	V
Internal V_{CC} Voltage	V_{INTVCC}	SV_{IN} > 5.5V	4.85	4.93	5.02	V
V_{IN} Quiescent Current ([2]) Active, Single Channel	$I_{Q(ACT, 1CH)}$	R_{RT} = 100kΩ, MODE/SYNC = 0V, V_{RUN1} = 2V, $V_{RUN2,3,4}$ = 0V		2	3	mA
V_{IN} Quiescent Current ([2]) Active, All Channels	$I_{Q(ACT, 4CH)}$	R_{RT} = 100kΩ, MODE/SYNC = 0V, $V_{RUN1,2,3,4}$ = 2V		6	7	mA
V_{IN} Quiescent Current ([2]) Shutdown Mode	$I_{Q(SHDN)}$	R_{RT} = 100kΩ $V_{RUN1,2,3,4}$ = 0V		30	38	µA
Feedback Reference Voltage ([3])	V_{FB}	ITH = 1V -40°C ≤ T_J ≤ 125°C	0.496	0.5	0.504	V
Feedback Voltage Line and Load Regulation ([3])	$\Delta V_{FB(LINE+LOAD)}$		-0.1	0.07	0.2	%
Feedback Pin Input Current	I_{FB}				±50	nA
Error Amplifier Transconductance	$Gm_{(EA)}$	ITH = 1V	0.9	1.05	1.2	ms
ITH Internal Compensation Threshold	$V_{ITH-INT}$		V_{INTVCC} - 0.3			V
Minimum On-Time	$t_{ON(MIN)}$	-40°C ≤ T_J ≤ 125°C		12	20	ns
Minimum Off-Time	$t_{OFF(MIN)}$			25		ns
Positive Inductor Valley Current Limit	$I_{LIM-POS}$	FB = 0.48V -40°C ≤ T_J ≤ 125°C	5	6	7	A
Negative Inductor Valley Current Limit	$I_{LIM-NEG}$	FB = 0.52V -40°C ≤ T_J ≤ 125°C	-7.9	-6.8	-5.8	A
Current Limit at Different ITH Voltage	$I_{LIM-ITH}$	ITH = 1.3V	2.5	3	3.5	A
		ITH = 1V	-0.5	0	0.5	
		ITH = 0.7V	-3.5	-3	-2.5	
Top Power NMOS On-Resistance	R_{TOP}	$INTV_{CC}$ = 5V		37		mΩ
Bottom Power NMOS On-Resistance	R_{BOT}	$INTV_{CC}$ = 5V		12		mΩ
Top Switch Leakage	$I_{SW(TOP)}$	V_{IN} = 18V, V_{SW} = 0V		0.05	0.5	µA
Bottom Switch Leakage	$I_{SW(BOTTOM)}$	V_{IN} = 18V, V_{SW} = 18V		0.1	1.5	µA

(Specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
$INTV_{CC}$ Undervoltage Lockout Threshold	V_{UVLO}	$INTV_{CC}$ Falling	2.2	2.4	2.6	V
		$INTV_{CC}$ Hysteresis (Rising)		0.21		
RUN Threshold	V_{RUN}	RUN Rising	1.16	1.2	1.24	V
		RUN Hysteresis (Falling)		100		mV
PGOOD Pull-Down Resistance	R_{PGOOD}	1mA Load		5	10	Ω
Output Overvoltage PGOOD Upper Threshold	OV	V_{FB} Rising	4.5	6.5	8.5	%
		V_{FB} Hysteresis		2		
Output Undervoltage PGOOD Lower Threshold	UV	V_{FB} Falling	-9	-7	-5	%
		V_{FB} Hysteresis		2		
PGOOD Leakage	I_{PGOOD}	V_{FB} = 0.5V			2	µA
TRACK Pull-Up Current	I_{TRACK}	V_{TRACK} = 0V		5	10	µA
Internal Soft-Start Time	t_{ss}	0% to 90% Output Rise Time		115		µs
Oscillator Frequency	f_{osc}	R_{RT} = 100kΩ -40°C ≤ T_J ≤ 125°C	0.9	1	1.1	MHz
Oscillator Frequency Range	f_{osc_range}	R_{RT} = 249kΩ to 33.2kΩ	0.4		3	MHz
SYNC Capture Range	f_{SYNC}	% of Programmed Frequency		±30		%
MODE/SYNC Threshold	$V_{IH(MODE/SYNC)}$	MODE/SYNC HIGH	1			V
	$V_{IL(MODE/SYNC)}$	MODE/SYNC LOW			0.3	
MODE/SYNC Current	$I_{MODESYNC}$	MODE/SYNC = 0V		5	10	µA
PHMODE Threshold	$V_{PHASEMODE}$	90° (4 Phase)			0.3	V
		120° (3 Phase)	1			

[1] The LT7200S is tested under pulsed load conditions such that $T_J \approx T_A$. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT7200S is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

[2] The quiescent current in Discontinuous Mode does not include switching loss of the power FETs.

[3] V_{FB} is measured in a feedback loop that servos V_{ITH} to a specified voltage.

[4] There is additional switch current due to internal resistor to ground.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
PV_{INx}, SV_{IN}, RUNx, SWx Voltage	-0.3V to 18V
FBx, TRACKx, PGOODx Voltage	-0.3V to 6V
MODE/SYNC, PHMODE Voltage	-0.3V to $INTV_{CC}$
RT, ITHx Voltage	-0.3V to $INTV_{CC}$
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Internal Temperature	125°C
Peak Reflow Solder Body Temperature	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

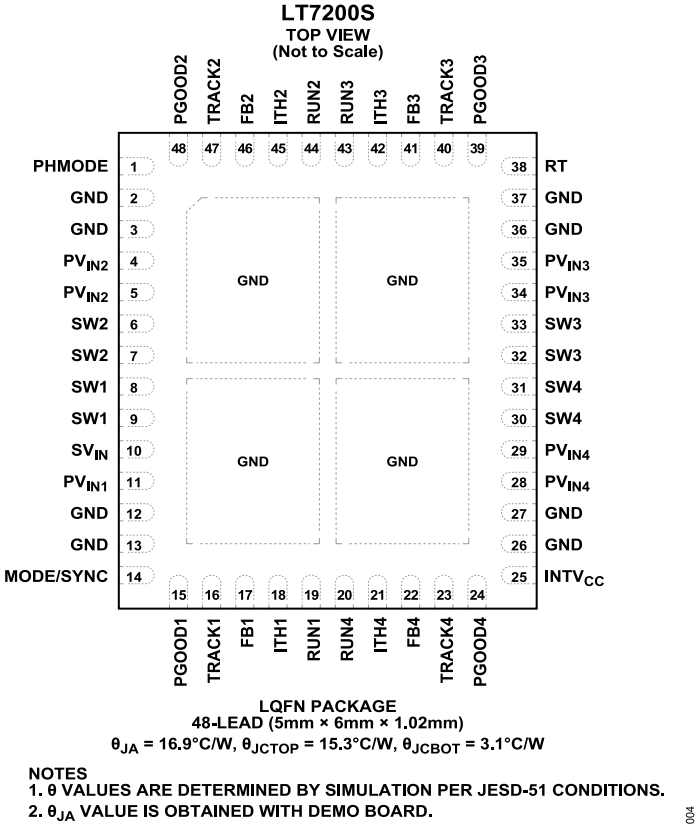


Figure 3. Pin Configurations

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	PHMODE	Control Input to Phase Selector. Determines the phase relationship of the 4 channels. Tie it to GND for 4-phase operation, tie it to $INTV_{CC}$ for 3-phase operation.
2, 3,12, 13, 26, 27, 36, 37	GND	Ground for Power and Signal Ground.
11	PV_{IN1}	Channel 1 Power V_{IN}. Input voltage to the on-chip Power MOSFETs.
4, 5	PV_{IN2}	Channel 2 Power V_{IN}. Input voltage to the on-chip Power MOSFETs.
34, 35	PV_{IN3}	Channel 3 Power V_{IN}. Input voltage to the on-chip Power MOSFETs.
28, 29	PV_{IN4}	Channel 4 Power V_{IN}. Input voltage to the on-chip Power MOSFETs.
8, 9	SW1	Channel 1 Switch Node Connection of External Inductor. Voltage swing of SW1 is from a diode voltage drop below ground to a diode voltage above PV_{IN1}.

6, 7	SW2	Channel 2 Switch Node Connection of External Inductor. Voltage swing of SW2 is from a diode voltage drop below ground to a diode voltage above PV_{IN2}.
32, 33	SW3	Channel 3 Switch Node Connection of External Inductor. Voltage swing of SW3 is from a diode voltage drop below ground to a diode voltage above PV_{IN3}.
30, 31	SW4	Channel 4 Switch Node Connection of External Inductor. Voltage swing of SW4 is from a diode voltage drop below ground to a diode voltage above PV_{IN4}.
10	SV_{IN}	Signal V_{IN}. Filtered input voltage to the on-chip 5V regulator. Bypass signal into the SV_{IN} pin with a 1µF ceramic capacitor.
14	MODE/SYNC	Mode Selection and Oscillator Synchronization Pin. Tie MODE/SYNC to GND for Discontinuous Mode (DCM). Floating MODE/SYNC or tying it to a voltage above 1V selects Forced Continuous Mode (FCM). Furthermore, connecting MODE/SYNC to an external clock synchronizes the system clock to the external clock and puts the part in Forced Continuous Mode (FCM). The synchronization is +/- 30% of the frequency set by the external resistor R_{RT} connected at RT pin.
15	PGOOD1	Channel 1 Output Power Good with Open-Drain Logic. PGOOD1 is pulled to ground when the voltage of the FB1 pin is not within +/- 7.5% of the internal 0.5V reference.
48	PGOOD2	Channel 2 Output Power Good with Open-Drain Logic. PGOOD2 is pulled to ground when the voltage of the FB2 pin is not within +/- 7.5% of the internal 0.5V reference.
39	PGOOD3	Channel 3 Output Power Good with Open-Drain Logic. PGOOD3 is pulled to ground when the voltage of the FB3 pin is not within +/- 7.5% of the internal 0.5V reference.
24	PGOOD4	Channel 4 Output Power Good with Open-Drain Logic. PGOOD4 is pulled to ground when the voltage of the FB4 pin is not within +/- 7.5% of the internal 0.5V reference.
16	TRACK1	Channel 1 Output Tracking and Soft-Start Pin. Allows to control the rise time of the output voltage. Connecting a voltage between 0V to 0.5V on this pin relative to GND bypasses error amplifier's internal reference input. Instead, it servos the FB pin to that voltage. There's an internal 5µA pullup current from $INTV_{CC}$ to this pin; putting a capacitor from this pin to GND provides soft-start function.
47	TRACK2	Channel 2 Output Tracking and Soft-Start Pin. Allows to control the rise time of the output voltage. Connecting a voltage between 0V to 0.5V on this pin relative to GND bypasses error amplifier's internal reference input. Instead, it servos the FB pin to that voltage. There's an internal 5µA pullup current from $INTV_{CC}$ to this pin; putting a capacitor from this pin to GND provides soft-start function.
40	TRACK3	Channel 3 Output Tracking and Soft-Start Pin. Allows to control the rise time of the output voltage. Connecting a voltage between 0V to 0.5V on this pin relative to GND bypasses error amplifier's internal reference input. Instead, it servos the FB pin to that voltage. There's an internal 5µA pullup current from $INTV_{CC}$ to this pin; putting a capacitor from this pin to GND provides soft-start function.
23	TRACK4	Channel 4 Output Tracking and Soft-Start Pin. Allows to control the rise time of the output voltage. Connecting a voltage between 0V to 0.5V on this pin relative to GND bypasses error amplifier's internal reference input. Instead, it servos the FB pin to that voltage. There's an internal 5µA pullup current from $INTV_{CC}$ to this pin; putting a capacitor from this pin to GND provides soft-start function.

17	FB1	Channel 1 Feedback Input to the Error Amplifier of the Step-Down Regulator. LT7200S regulates this pin to a 0.5V accurate internal reference voltage. Connect resistor divider tap to this pin. The output voltage, V_{OUT}, can be adjusted from 0.5V to 0.9 x V_{IN} by: V_{OUT} = 0.5V x [1+(R2/R1)].
46	FB2	Channel 2 Feedback Input to the Error Amplifier of the Step-Down Regulator. LT7200S regulates this pin to a 0.5V accurate internal reference voltage. Connect resistor divider tap to this pin. The output voltage, V_{OUT}, can be adjusted from 0.5V to 0.9 x V_{IN} by: V_{OUT} = 0.5V x [1+(R2/R1)].
41	FB3	Channel 3 Feedback Input to the Error Amplifier of the Step-Down Regulator. LT7200S regulates this pin to a 0.5V accurate internal reference voltage. Connect resistor divider tap to this pin. The output voltage, V_{OUT}, can be adjusted from 0.5V to 0.9 x V_{IN} by: V_{OUT} = 0.5V x [1+(R2/R1)].
22	FB4	Channel 4 Feedback Input to the Error Amplifier of the Step-Down Regulator. LT7200S regulates this pin to a 0.5V accurate internal reference voltage. Connect resistor divider tap to this pin. The output voltage, V_{OUT}, can be adjusted from 0.5V to 0.9 x V_{IN} by: V_{OUT} = 0.5V x [1+(R2/R1)].
18	ITH1	Channel 1 Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Normal range is from 0.3V to 1.6V.
45	ITH2	Channel 2 Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Normal range is from 0.3V to 1.6V.
42	ITH3	Channel 3 Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Normal range is from 0.3V to 1.6V.
21	ITH4	Channel 4 Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Normal range is from 0.3V to 1.6V.
19	RUN1	Channel 1 Logic Controlled RUN Input. Do not leave this pin floating. Logic High activates the step-down regulator.
44	RUN2	Channel 2 Logic Controlled RUN Input. Do not leave this pin floating. Logic High activates the step-down regulator.
43	RUN3	Channel 3 Logic Controlled RUN Input. Do not leave this pin floating. Logic High activates the step-down regulator.
20	RUN4	Channel 4 Logic Controlled RUN Input. Do not leave this pin floating. Logic High activates the step-down regulator.
25	$INTV_{CC}$	Internal 5V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR ceramic capacitor.
38	RT	Switching Frequency Program Pin. Connect an external resistor R_{RT} (between 249kΩ to 33.2kΩ) from this pin to GND to program the frequency from 400kHz to 3MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

TA = 25°C, V_{IN} = 12V, V_{OUT} = 1.2V, unless otherwise specified.

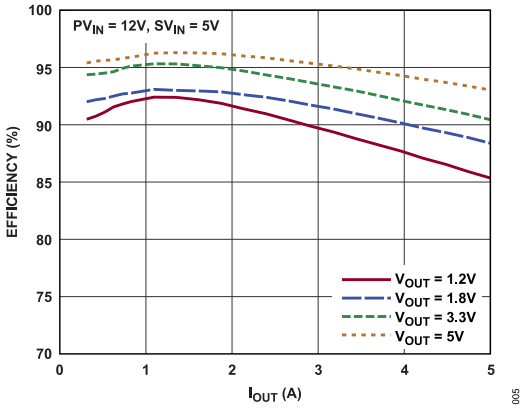


Figure 4. Efficiency vs Load Current (500kHz)

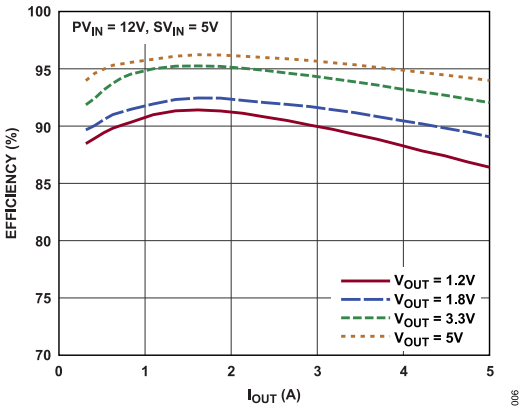


Figure 5. Efficiency vs Load Current (1MHz)

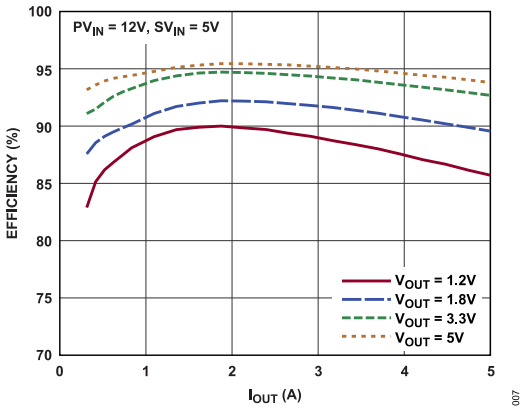


Figure 6. Efficiency vs Load Current (2MHz)

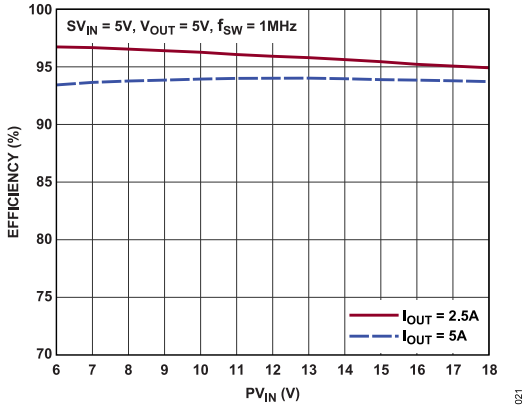


Figure 7. Efficiency vs PV_{IN}

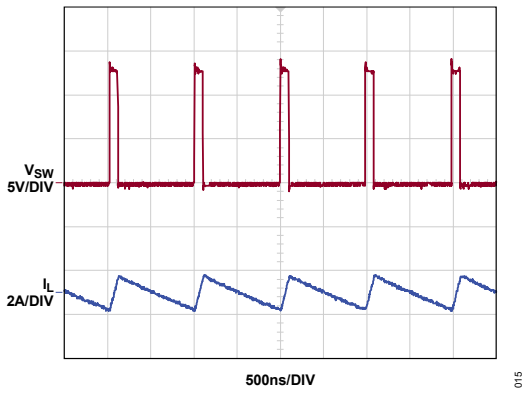


Figure 8. Forced Continuous Mode (FCM)

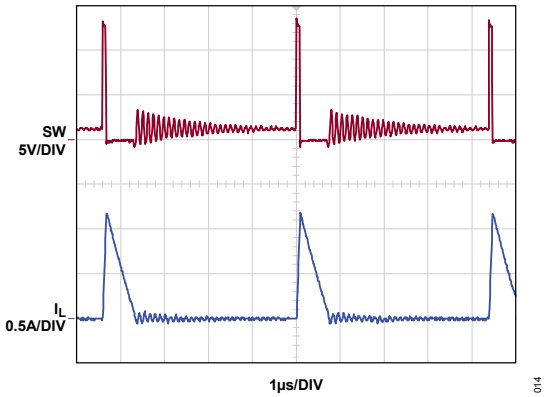
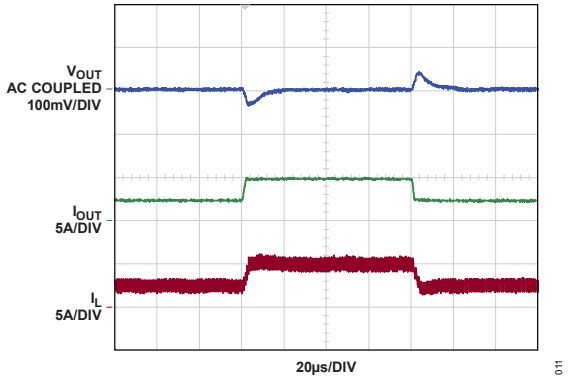
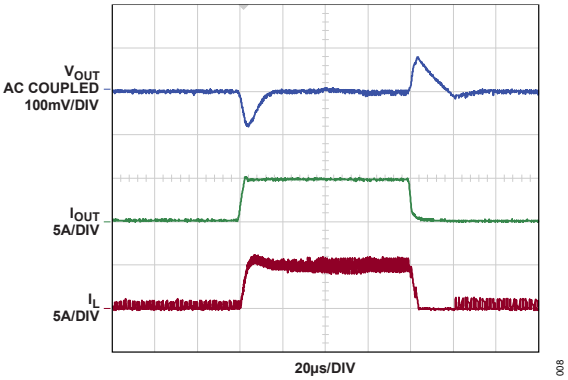


Figure 9. Discontinuous Mode (DCM)



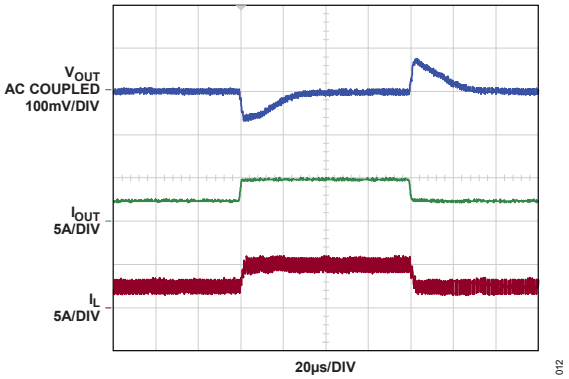
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 2.5A to 5A, f_{SW} = 1MHz
R_{ITH} = 10KΩ, C_{ITH} = 470pF, C_{ITHP} = 4.7pF
R_{FB1} = 10kΩ, R_{FB2} = 14 kΩ, C_{OUT} = 2 x 47µF, L = 0.6µH

Figure 10. Transient Response, FCM



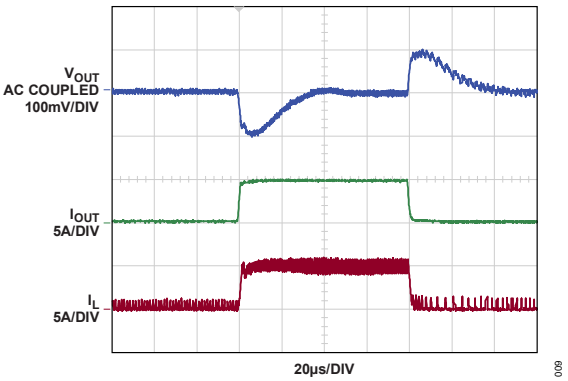
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0.3A to 5A, f_{SW} = 1MHz
R_{ITH} = 10KΩ, C_{ITH} = 470pF, C_{ITHP} = 4.7pF
R_{FB1} = 10kΩ, R_{FB2} = 14 kΩ, C_{OUT} = 2 x 47µF, L = 0.6µH

Figure 11. Transient Response, DCM



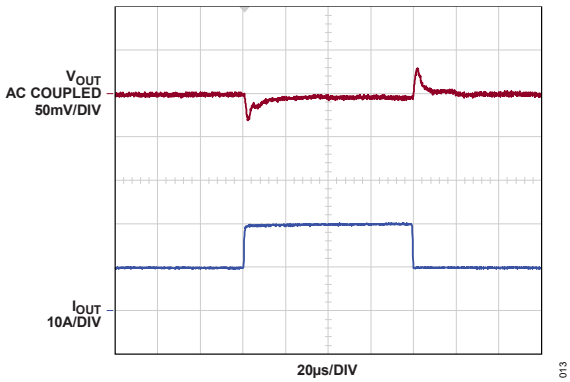
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, f_{SW} = 1MHz
R_{ITH} = 4.99KΩ, C_{ITH} = 470pF, C_{ITHP} = 4.7pF
R_{FB1} = 10kΩ, R_{FB2} = 90.9 kΩ, C_{OUT} = 2 x 47µF, L = 1.5µH

Figure 12. Transient Response, FCM



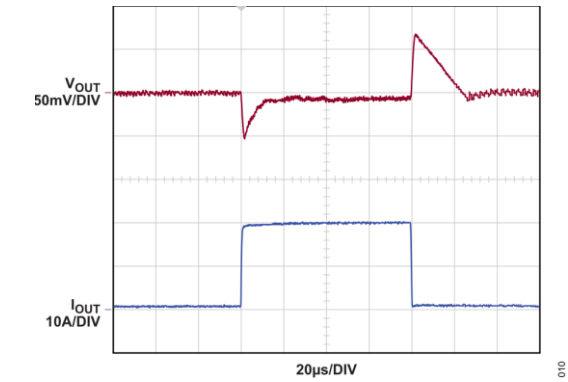
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.3A to 5A, f_{SW} = 1MHz
R_{ITH} = 13KΩ, C_{ITH} = 470pF, C_{ITHP} = 4.7pF
R_{FB1} = 10kΩ, R_{FB2} = 90.9 kΩ, C_{OUT} = 2 x 47µF, L = 1.5µH

Figure 13. Transient Response, DCM



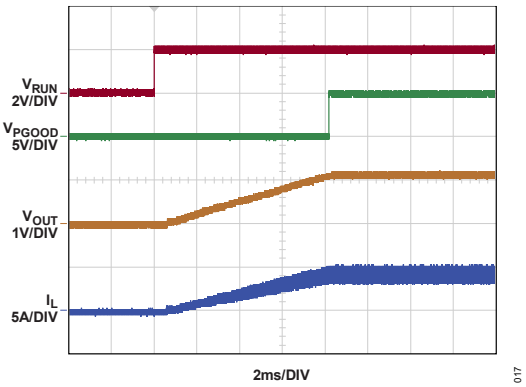
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 1A to 20A, f_{SW} = 1MHz
R_{ITH} = 4.99KΩ, C_{ITH} = 1nFpF, C_{ITHP} = 10pF
R_{FB1} = 10kΩ, R_{FB2} = 14 kΩ, C_{OUT} = 9 x 47µF, $L_{1,2,3,4}$ = 0.6µH

Figure 14. Transient Response, FCM



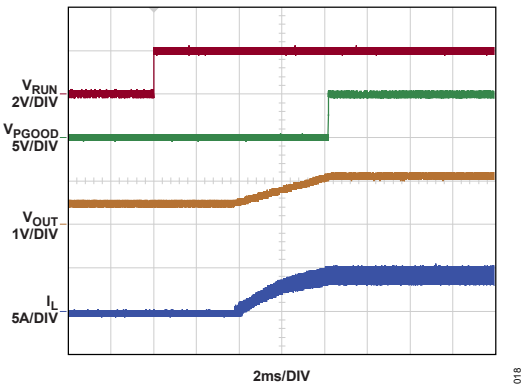
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 1A to 20A, f_{SW} = 1MHz
R_{ITH} = 4.99KΩ, C_{ITH} = 1nFpF, C_{ITHP} = 10pF
R_{FB1} = 10kΩ, R_{FB2} = 14 kΩ, C_{OUT} = 9 x 47µF, $L_{1,2,3,4}$ = 0.6µH

Figure 15. Transient Response, DCM



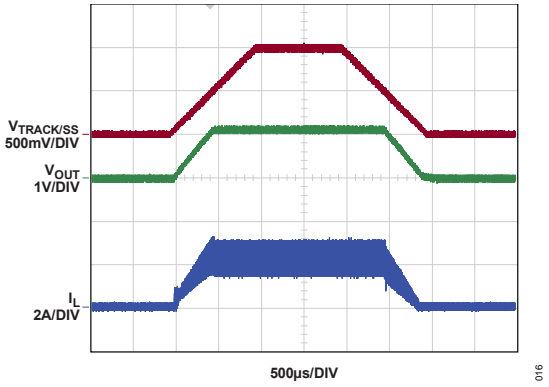
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 2.5A
R_{FB1} = 10KΩ, R_{FB2} = 14KΩ, COUT = 2 x 47µF
$V_{TRACK/SS}$ = 0.1µF

Figure 16. Start-Up Waveform



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 2.5A
R_{FB1} = 10KΩ, R_{FB2} = 14KΩ, COUT = 2 x 47µF
$V_{TRACK/SS}$ = 0.1µF

Figure 17. Start-Up Waveform (with Prebiased Output)



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 2.5A
R_{FB1} = 10KΩ, R_{FB2} = 14KΩ, COUT = 2 x 47µF
$V_{TRACK/SS}$ = 0.1µF

Figure 18. Output Tracking

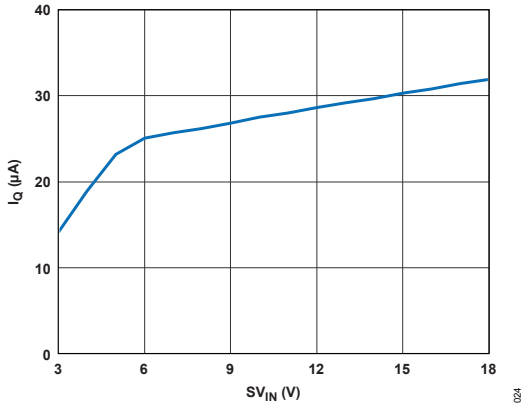


Figure 19. Shutdown Current vs SV_{IN}

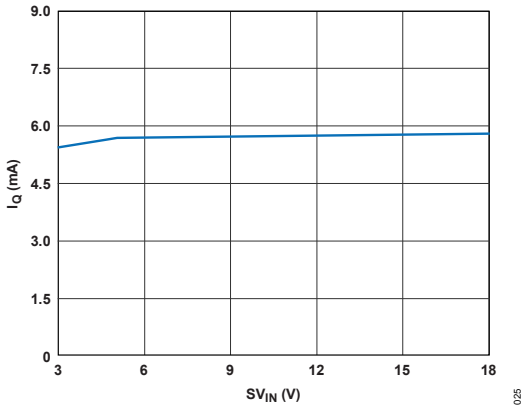


Figure 20. Active Current vs SV_{IN} DCM, No Load (CH1-4 ON)

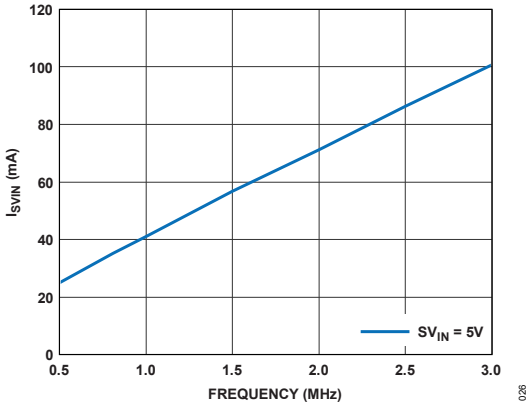


Figure 21. SV_{IN} Current vs Switching Frequency DCM, No Load (CH1-4 ON)

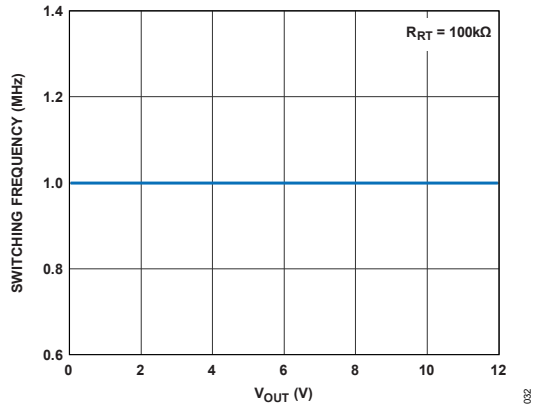


Figure 22. Switiching Frequency vs V_{OUT}

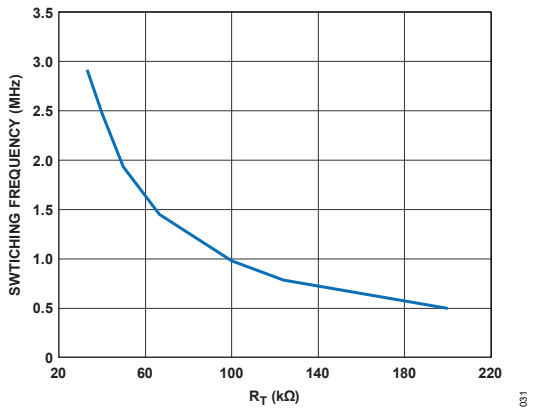


Figure 23. Switching Frequency vs R_T

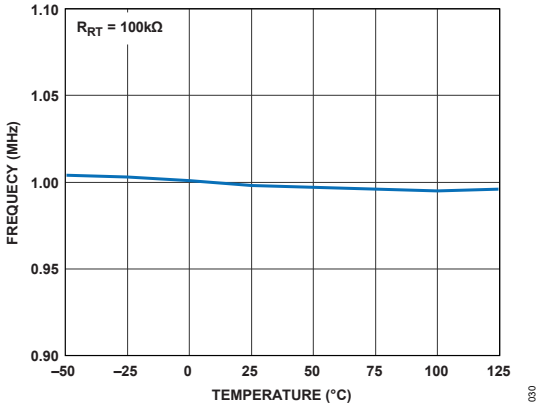


Figure 24. Switching Frequency vs Temperature

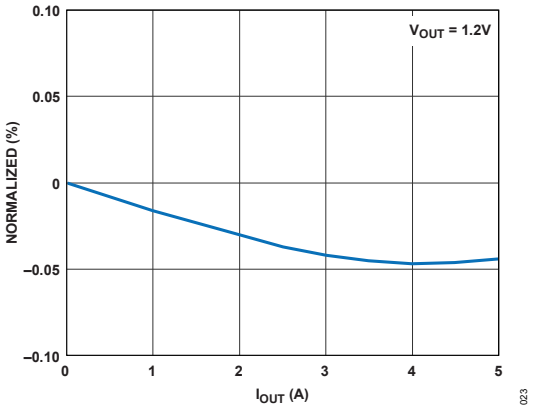


Figure 25. Load Regulation vs Load Current

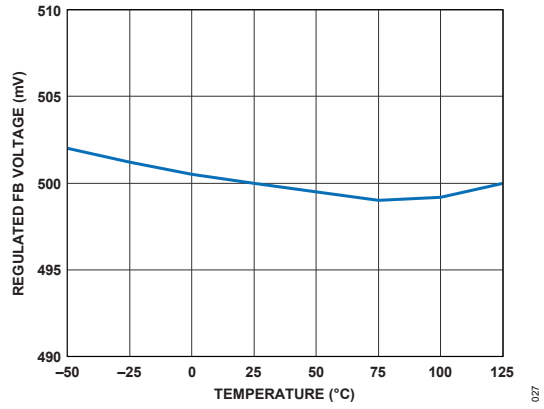


Figure 26. Regulated FB Voltage vs Temperature

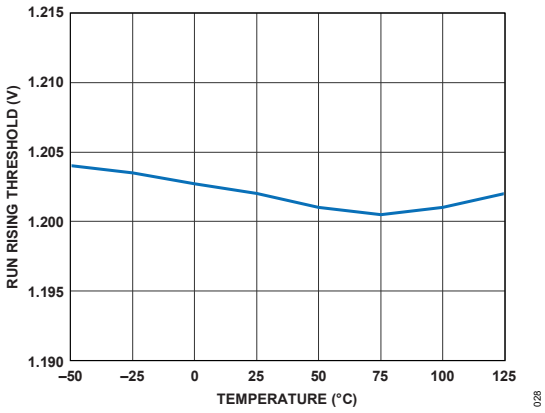


Figure 27. RUN Rising Threshold vs Temperature

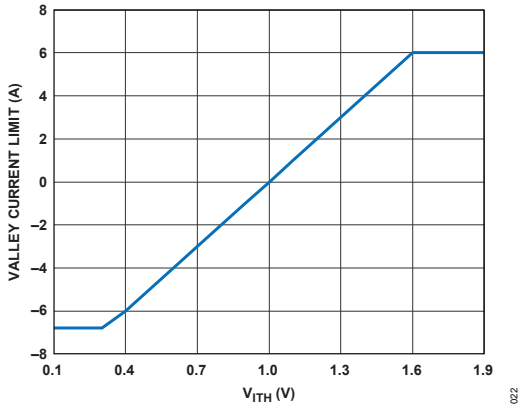


Figure 28. Valley Current Limit vs V_{ITH}

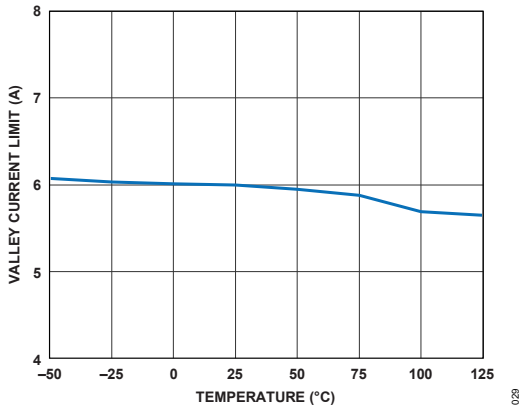
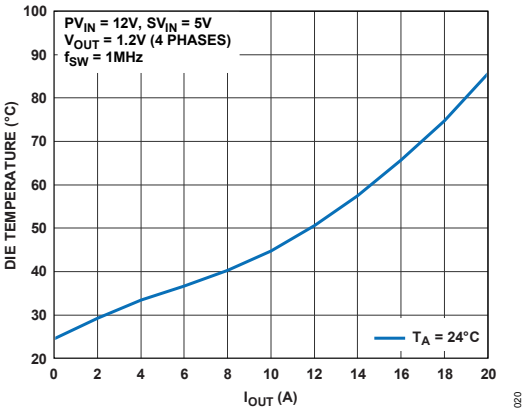


Figure 29. Valley Current Limit vs Temperature



P_{VIN} = 12V, SV_{IN} = 5V V_{OUT} = 1.2V (4 PhaseS), f_{sw} = 1MHz

Figure 30. Die Temperature vs Load

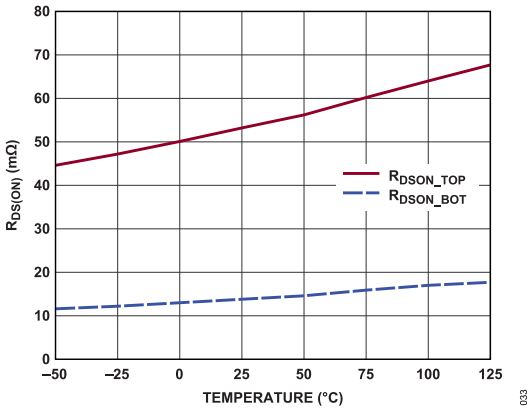


Figure 31. $R_{DS(ON)}$ vs Temperature

BLOCK DIAGRAM

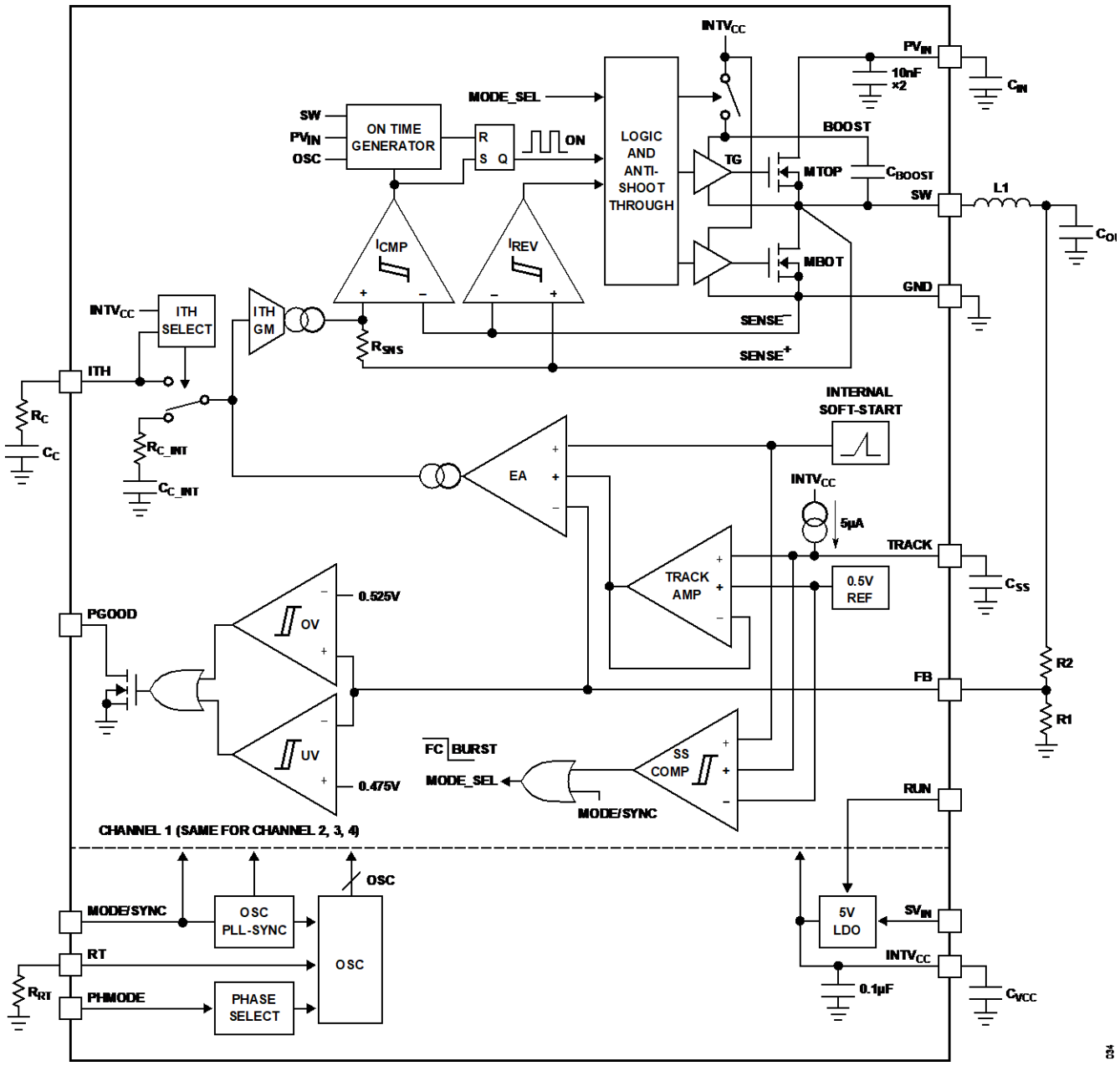


Figure 32. Block Diagram

THEORY OF OPERATION

Main Control Loop

The LT7200S is a quad-channel, current-mode monolithic step-down regulator capable of providing ±5A of output current from each channel. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer ("ON" signal in Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, I_{CMP}, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across SW and GND nodes of the bottom power MOSFET when it is on. The voltage on the ITH pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this ITH voltage by comparing the feedback signal, V_{FB}, with an internal 0.5V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference, the ITH voltage then rises until the average inductor current matches that of the load current.

At light load currents, the inductor current can drop to zero and become negative. In Discontinuous Mode (DCM) operation, this is detected by the current reversal comparator, I_{REV}, which then shuts off the bottom power MOSFET. Both power MOSFETs remain off with the output capacitor supplying the load current until the ITH voltage rises above zero current level to initiate the next cycle. If continuous mode of operation is desired, simply float the MODE/SYNC pin or tie it to $INTV_{CC}$.

The operating frequency is determined by the value of the R_{RT} resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the switching regulator on-time to track the internal oscillator and force a constant switching frequency. A clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external clock. The regulator defaults to force continuous operation once the clock signal is present.

The "S" in LTC7200S refers to the second generation Silent Switcher technology. The IC has integrated ceramic capacitors for V_{IN}, $INTV_{CC}$, and BOOST to keep all the fast AC current loops small, thus improving the EMI performance. Furthermore, it allows for faster switching edges, which greatly improves efficiency at high switching frequencies.

"Power Good" Status Output

PGOOD open-drain output is pulled low if the regulator output feedback voltage, V_{FB}, exits a ±7.5% window around the regulation point while the overvoltage (OV) or undervoltage (UV) comparator is tripped. This condition is released once regulation within a ±5.5% window is achieved.

Continuous operation is forced during OV and UV conditions, except during start-up when the TRACK pin is ramping up to 0.5V.

V_{IN} Overvoltage Protection

To protect the internal power MOSFET devices against transient voltage spikes, the LT7200S constantly monitors the PV_{IN} pin for an overvoltage condition. When the PV_{IN} rises above 20V, the regulator suspends operation by shutting off both power MOSFETs. Once PV_{IN} drops below 18V, the regulator immediately resumes normal operation. During an overvoltage event, the internal soft-start voltage is clamped to a voltage slightly higher than the feedback voltage. Thus, the soft-start feature is present upon exiting an overvoltage condition.

Overcurrent and Short-Circuit Protection

The LT7200S protects itself against output overcurrent and short-circuits by sensing the inductor valley current. When the current limit is reached, the output begins to fall, decreasing on-time of the top power MOSFET. If the short is prolonged enough for the on-time to reach its minimum, the off-time lengthens, lowering the switching frequency

and preventing excess current from being drawn from V_{IN}. After the overcurrent or short is removed, the regulator executes its soft-start function to prevent the output voltage from overshooting.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Connecting it to ground enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/ SYNC pin is tied to $INTV_{CC}$ or floated, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency. The LT7200S detects the presence of the external clock signal on the MODE/SYNC pin and synchronizes the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock places all regulators into forced continuous mode operation.

Multiphase Operation

For output loads that demand more than 5A of current, different channels of the LT7200S outputs can be tied together to run out of phase to provide more output current. Tying the PHMODE pin to GND forces 4-phase operation. Tie it to $INTV_{CC}$ for 3-phase operation.

Table 4. PHMODE Configuration Table

PHASE	PHMODE = GND	PHMODE = INTVCC
Channel 1	0°	0°
Channel 2	180°	120°
Channel 3	90°	240°
Channel 4	270°	0°

APPLICATIONS INFORMATION

The first page of the data sheet shows a general LT7200S application circuit. External component selection is largely driven by the target current ripple, load requirement, and switching frequency. Component selection typically begins with the selection of the inductor L and resistor R_{RT}. Once the inductor is chosen, select the input capacitor, C_{IN}, and the output capacitor, C_{OUT}. Next, select the feedback resistors to set the desired output voltage. Finally, select the remaining optional external components for functions such as external loop compensation, tracking/soft-start, input UVLO, and PGOOD.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Connecting a resistor, R_{RT}, from the RT pin to SGND programs the switching frequency, f, from 400kHz to 3MHz according to the following formula:

$$f(Hz) = \frac{1e^{11}}{R_{RT}(\Omega)}$$

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the R_{RT} programmed frequency.

Inductor Selection

For a given input voltage, V_{IN}, output voltage, V_{OUT}, the inductor value, L, and operating frequency, f, determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor current ripple decreases with higher inductor value and higher operating frequency. Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$, which is around 5A per channel. Exceeding 60% of $I_{OUT(MAX)}$ is not recommended. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \times \Delta I_{L(MAX)}} \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, select the type of inductor. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire leading to increased DCR and copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

To avoid overheating and poor efficiency, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of inductor ripple current:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Different core materials and shapes change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coilcraft, Toko, Vishay, NEC/Tokin, Cooper, TDK and Wurth Electronik. Refer to Table 5 for more details.

Table 5. Inductor Selection Table

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Coilcraft XEL5030 Series				
0.42	3	23.5	5.28 x 5.48	3.2
0.6	4.44	22	5.28 x 5.48	3.2
1	7	16.9	5.28 x 5.48	3.1
1.2	8.8	15.3	5.28 x 5.48	3.1
1.5	9.9	15	5.28 x 5.48	3.1

Selecting the Input Capacitor (C_{IN})

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, use a low ESR input capacitor sized for the maximum RMS current. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Selecting the Output Capacitor (C_{OUT})

The selection of C_{OUT} is determined by the effective series resistance (ESR) required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance necessary to ensure the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \times f \times C_{OUT}} + ESR\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types.

Tantalum capacitors have the highest capacitance density, but it is important to only use types that are surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Since the ESR of a ceramic capacitor is so low, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately

$$C_{OUT} = 3\frac{\Delta I_{OUT}}{f_0 \times V_{DROOP}}$$

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high Q characteristics of some types of ceramic capacitors, take care when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Choose X8R for 150°C applications.

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 47µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PV_{IN} and GND pins as possible.

$INTV_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator produces the 5V supply that powers the drivers and internal bias circuitry. The INTVCC must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. The decoupling capacitor should have low impedance electrical connections to the $INTV_{CC}$ and GND pins to provide the transient currents required by the LT7200S. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency experience an increase in die temperature due to the higher power dissipation across the LDO. In such cases, if there is another 5V supply rail available, consider using that to drive the SV_{IN} pin to lower the power dissipation across the internal LDO.

Output Voltage Programming

Each regulator's output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.5V \times (1 + \frac{R2}{R1})$$

The desired output voltage is set by the appropriate selection of resistors R1 and R2, which allow the V_{FB} pin to sense a fraction of the output voltage, as shown in Figure 33. Choosing large values for R1 and R2 results in improved zero/light load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the V_{FB} node. Take care to route the V_{FB} trace away from any noise source, such as SW trace. A feedforward compensation capacitor, C_{FF}, can also be placed between V_{OUT} and FB to improve transient performance.

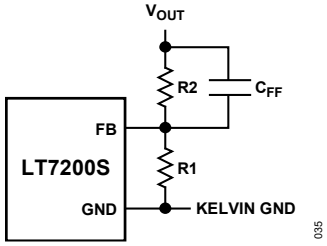


Figure 33. Setting the Output Voltage

If the output voltage is outside the V_{ON} sense range (0.5V ~ 4V), the output voltage stays in regulation, but the switching frequency may deviate from the programmed frequency.

Soft-Start and Output Voltage TRACK

An internal 5µA pulls up the TRACK pin to $INTV_{CC}$. Putting an external capacitor, C_{SS}, from TRACK to ground enables soft starting the output to prevent current surge on the input supply. The relationship between output rise time, T_{SS}, and soft-start capacitance, C_{SS}, is given by

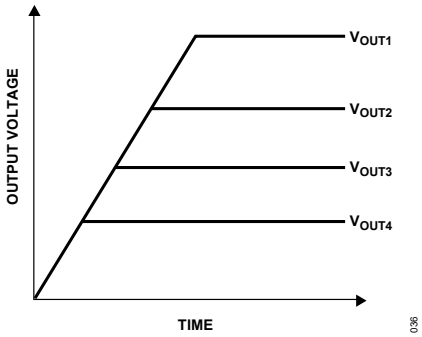
$$T_{SS} = 1e^5 \times C_{SS}$$

Upon start-up time, the LT7200S operates in discontinuous mode until track voltage is higher than 0.5V. The regulator then operates in forced continuous mode until output is above the UV threshold (V_{FB} > 0.4625V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above.

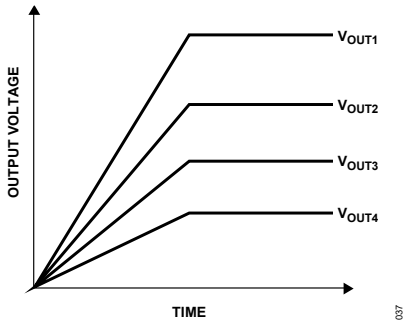
The LT7200S allows to program its output voltage ramp rate through the TRACK pin. From 0V to 0.5V, the TRACK voltage overrides the internal 0.5V reference input to the error amplifier, thus regulating the feedback voltage to that

of the TRACK pin. When TRACK is above 0.5V, tracking is disabled, and the feedback voltage regulates to the internal reference voltage.

For output tracking applications, when driving TRACK pin from another voltage source, set each channel's output to either coincidentally or ratiometrically track another supply's output, as shown in Figure 34. In the following discussions, V_{OUT1} refers to output of channel 1 as a master channel, and V_{OUT2}, V_{OUT3}, and V_{OUT4} refer to outputs of channels 2, 3, and 4 respectively. In practice, use either channel as the master.



(a) Coincident Tracking

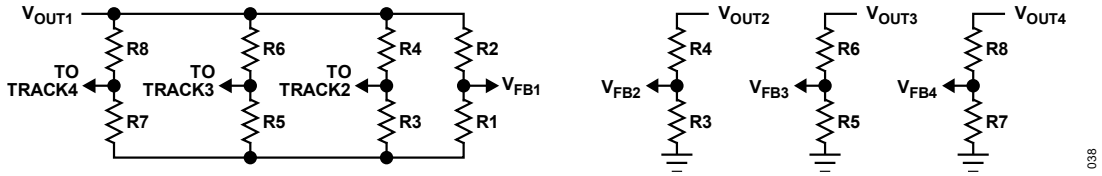


(b) Ratiometric Tracking

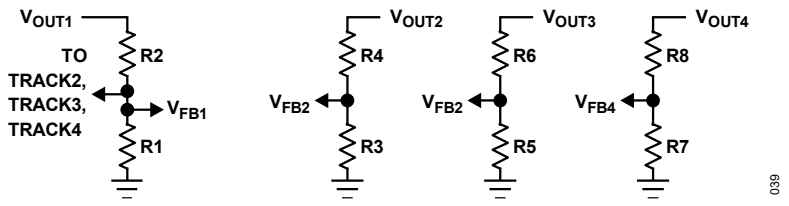
Figure 34. Output Tracking Applications

To implement the coincident tracking in Figure 34(a), connect additional resistive dividers to V_{OUT1} and connect its midpoint to the TRACK pins of the slave channels. The ratio of these dividers should be the same as those of the slave channels' feedback dividers shown in Figure 35(a). In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}, V_{OUT3}, and V_{OUT4}.

To implement the ratiometric tracking, the feedback pin of the master channel should connect to the TRACK pins of the slave channels shown in Figure 35(b).



(a) Coincident Tracking



(b) Ratiometric Tracking

Figure 35. Output Tracking Configuration

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time the LT7200S is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 40ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output drops out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \times \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 12ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of

$$DC_{MIN} = f \times t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. Reducing the operating frequency alleviates the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage remains in regulation and the switching frequency decreases from its programmed value. This is an acceptable result in many applications. So, this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of output overvoltage. As the sections on inductors and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

Internal/External ITH Compensation

The LT7200S provides the options to choose between internal and external loop compensations. By connecting the ITH pin to $INTV_{CC}$, the fixed internal loop compensation network is selected, which reduces both the required external component count and design time. To ensure stability, it is recommended that internal compensation only be used for applications with f_{SW} > 1MHz.

Alternatively, by connecting the external components to the ITH pin, choose external loop compensation to optimize the desired transient response. For multiphase, single output applications, use external compensation to tie the corresponding ITH pins together to accurately share the output current.

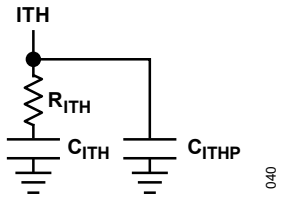


Figure 36. External Compensation Network

Select the proper ITH components for OPTI-LOOP® optimization. The compensation network is shown in Figure 36. The RC filter sets the dominant pole-zero loop compensation. The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency is kept the same, thereby keeping the phase the same in most critical frequency ranges of the feedback loop.

For a 1MHz application, an R-C network of 470pF and 10kΩ provides a good starting point. A 4.7pF bypass capacitor, C_{ITHP}, on the ITH pin is recommended to filter out high frequency coupling from stray board capacitance. Table 6 provides a basic guideline for the compensation values to use, given the frequency of the part. Slight tweaks to those values may be required depending on the application's required output capacitance.

Table 6. Compensation Values

Frequency	R_{ITH}	C_{ITH}	C_{ITHP}
500kHz	15k	470pF	4.7pF
700kHz	10k	470pF	4.7pF
1MHz	10k	470pF	4.7pF
1.5MHz	10k	470pF	4.7pF
2MHz	10k	220pF	4.7pF

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows for optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects these close loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external component shown in the Table 6 circuit provides an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested value) to optimize transient response once the final PC layout is done and the output capacitor type and value are determined. Select the output capacitors because their various types and values determine the loop feedback factor gain and phase. In addition, add a feedforward capacitor C_{FF} to improve the high frequency response, as shown in Figure 33. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

An output current pulse of 20% to 100% of full load current having a rise time of ~1µs produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop. Switching regulators may take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the ΔI_{LOAD} x ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to

charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that indicates a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance. For detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Analog Devices Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (> 47µF) input capacitors. The discharge input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change produces the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LT7200S circuits: 1) I^2R losses, 2) switching and biasing losses, 3)other losses.

- I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

  $$R_{SW} = (R_{DS(ON)TOP})\,(DC) + (R_{DS(ON)BOT})\,(1 - DC)$$

  The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

  $$I^2R \text{ losses} = I_{OUT}^2\,(R_{SW} + R_L)$$

- The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from PV_{IN} to ground. The resulting dQ/dt is a current out of IN typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs, and f is the switching frequency. The power loss is thus:

  $$\text{Switching Loss} = I_{GATECHG} \text{ x } PV_{IN}$$

  The gate charge loss shows up as current through the $INTV_{CC}$ pin as well as frequency. Thus, their effects are more pronounced in applications with higher input voltage and higher frequency.

- Other “hidden” losses such as transition loss, copper trace, and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these “system” level losses in the system design. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LT7200S internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses, which generally account for less than 2% total additional loss.

Thermal Conditions

In some applications where the LT7200S is operated at a combination of high ambient temperature, high switching frequency, high V_{IN}, and high output load, the required power dissipation might push the part to exceed its maximum junction temperature.

To avoid the LT7200S from exceeding the maximum junction temperature, maximum current rating is derated depending on the operating conditions. The temperature rise of the part varies depending on the thickness of copper on the PCB board, the number of layers of the board, and the shape of copper trace. In general, a thick continuous piece of copper on the top layer of the PCB for SW and GND pins greatly improves the thermal performance of the part.

Figure 37 shows case temperature rise curve of the LT7200S on a standard 6-layer, 2oz copper per layer PCB board (LT7200S standard demo board). V_{OUT} is set to 1.2V in all curves.

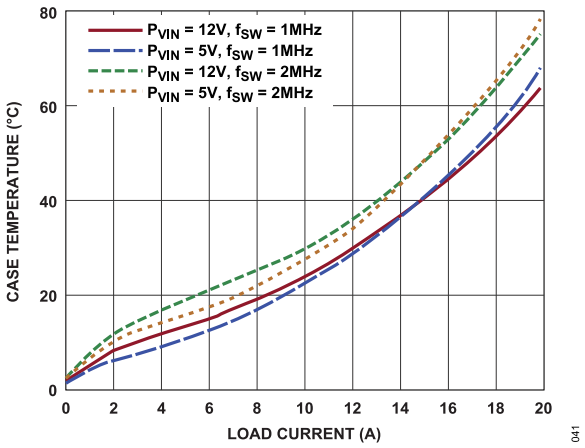


Figure 37. Case Temperature Rise

Silent Switcher Architecture

The LT7200S has integrated capacitors that allow it to operate at high switching frequencies efficiently. The internal V_{IN} bypass capacitors allow the SW edges to transition extremely fast, effectively reducing transition loss. The capacitors also greatly reduce SW overshoot during top FET turn-on, which improves the robustness of the device over time.

Board Layout Considerations

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LT7200S (see Figure 38). Check the following in the layout:

1. Do the capacitors C_{IN} connect to the PV_{IN} and GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.

3. Place the FB dividers close to the part with kelvin connections to V_{OUT} and GND at the point of load.

4. Keep sensitive components away from the SW pin. Route the FB resistors, RT resistor, compensation component, and $INTV_{CC}$ bypass caps away from the SW trace and inductor.

5. A ground plane is preferred.

6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. Connect these copper areas to GND.

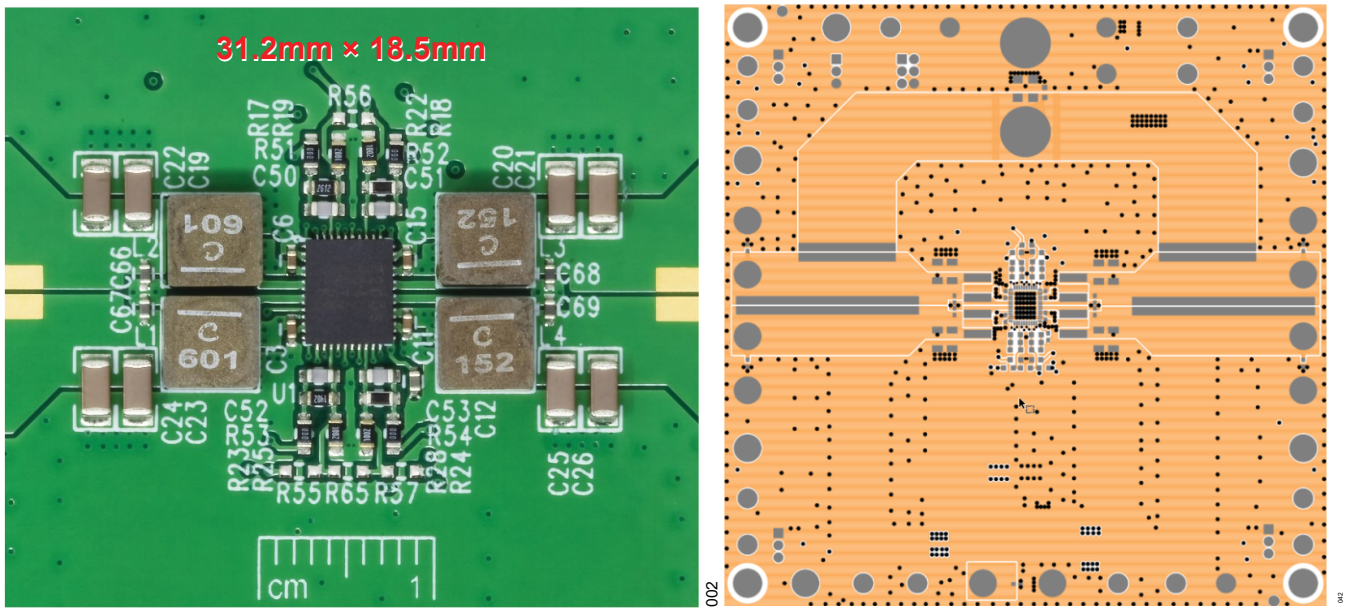


Figure 38. Example of Top Layer PCB Design

Design Example

As a design example, consider the LT7200S in an application with the following specifications:

$$V_{IN} = 12V$$

$$V_{OUT} = 1.2V$$

$$I_{OUT(MAX)} = 5A$$

$$f_{SW} = 1MHz$$

First, to program the output to 1.2V, set R_{FB1} to be 10kΩ and R_{FB2} to be 14kΩ, typical values that can be used here for both resistors is 10kΩ. For best accuracy, use a 0.1% resistor.

For a typical soft start time of 2ms (0% to 100% of final V_{OUT} value), the C_{TRACK} should be:

$$5\mu A = C_{SS} \times \frac{0.5V}{2ms}$$

$$C_{SS} = 20nF$$

Use a typical 22nF capacitor for C_{SS}.

Because efficiency is important at both high and low load current, discontinuous mode operation is utilized. Select from the characteristic curves the correct R_T resistor for the 1MHz switching frequency. Based on that, R_{RT} should be 100kΩ. Then calculate the inductor value to achieve a current ripple that is about 40% of the maximum peak current limit (5A) at maximum V_{IN}:

$$L = \frac{V_{OUT}}{f \text{ x } \Delta I_L} \text{ x } (1 - \frac{V_{OUT}}{V_{IN}})$$

$$L = \frac{1.2V}{1MHz \text{ x } 2A} \text{ x } (1 - \frac{1.2V}{15V}) = 0.55\mu H$$

The closest standard value inductor higher is 0.6µH.

Select C_{OUT} based on the ESR required to satisfy the output ripple requirement and the bulk capacitance needed for loop stability. For this design, use two 47µF ceramic capacitors.

Size C_{IN} for a maximum current rating of:

$$I_{RMS\_Channel} = 5A \text{ x } (\frac{1.2V}{15V}) \sqrt{(\frac{15V}{1.2V} - 1)} = 1.36A$$

$I_{RMS\_Total} = 36A \text{ x } 4 = 5.4A$, if connect outputs of four channels together.

Decoupling V_{IN} with two 22µF ceramic capacitor, as shown in Figure 38, is adequate for most applications.

TYPICAL APPLICATIONS

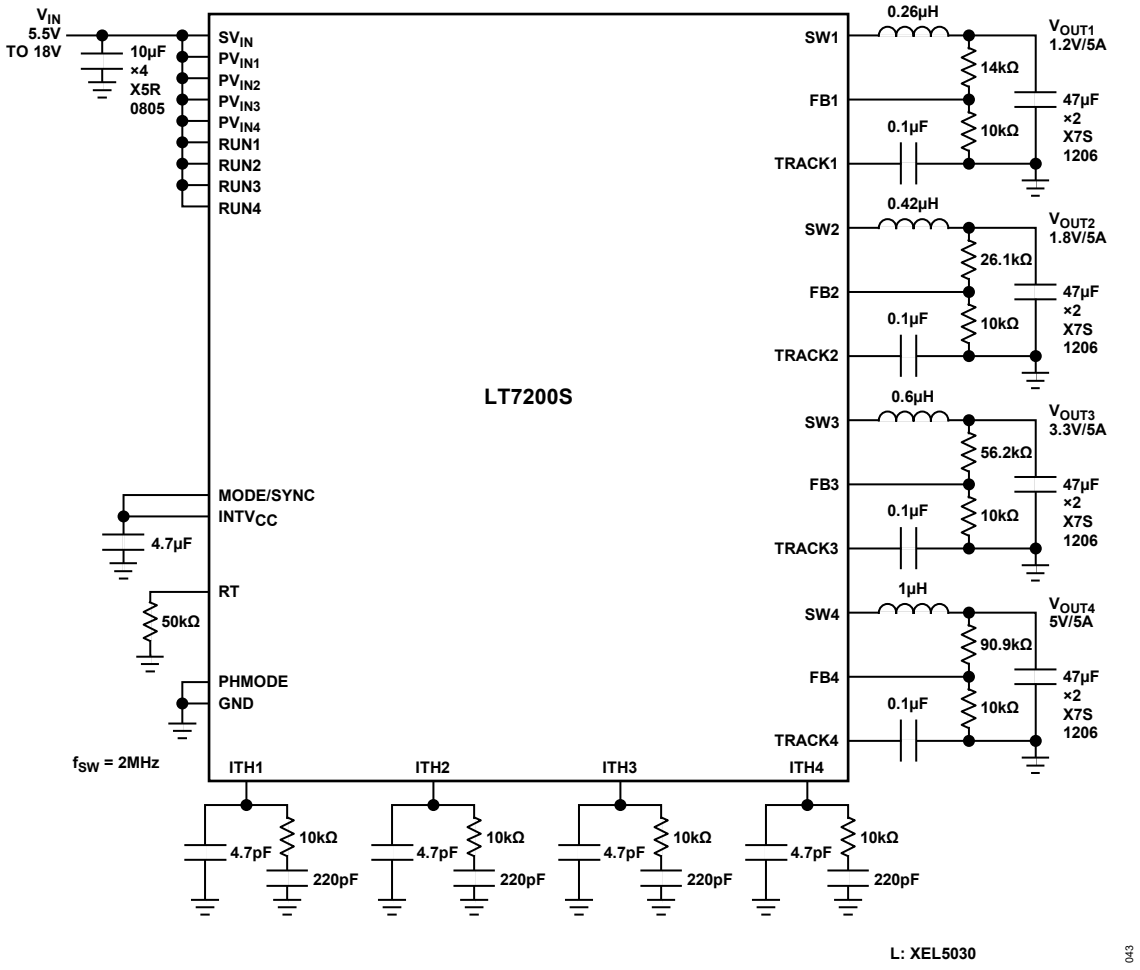


Figure 39. Quad 1.2V/5A, 1.8V/5A, 3.3V/5A, 5V/5A, 2MHz, Buck Regulator

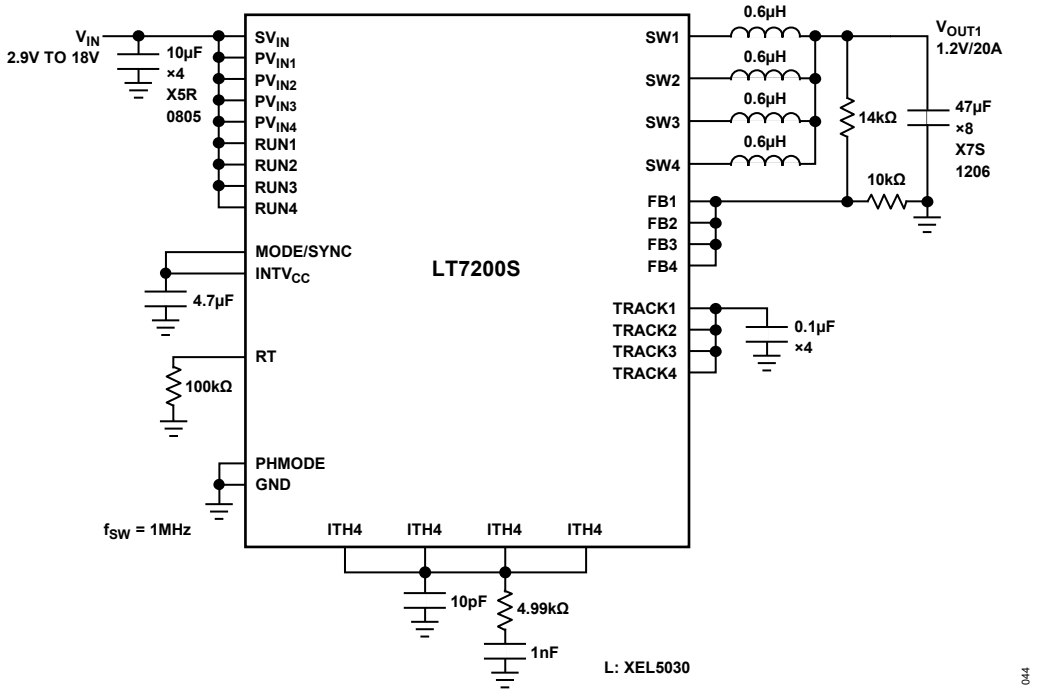


Figure 40. Single 1.2V/20A Output Buck Regulator

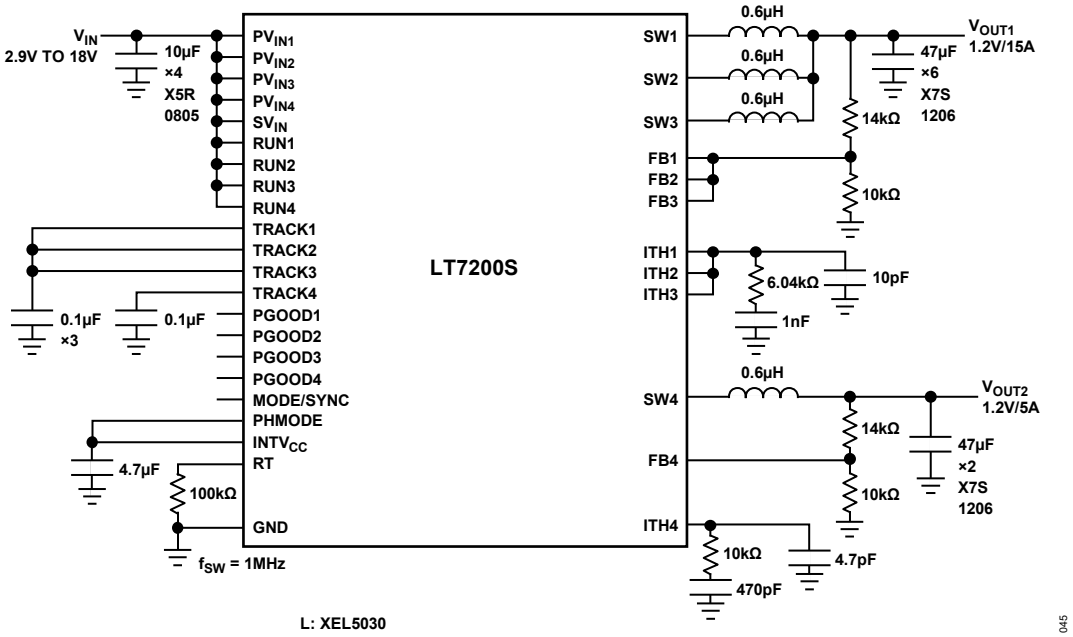


Figure 41. Dual 1.2V, 15A/5A Buck Regulator

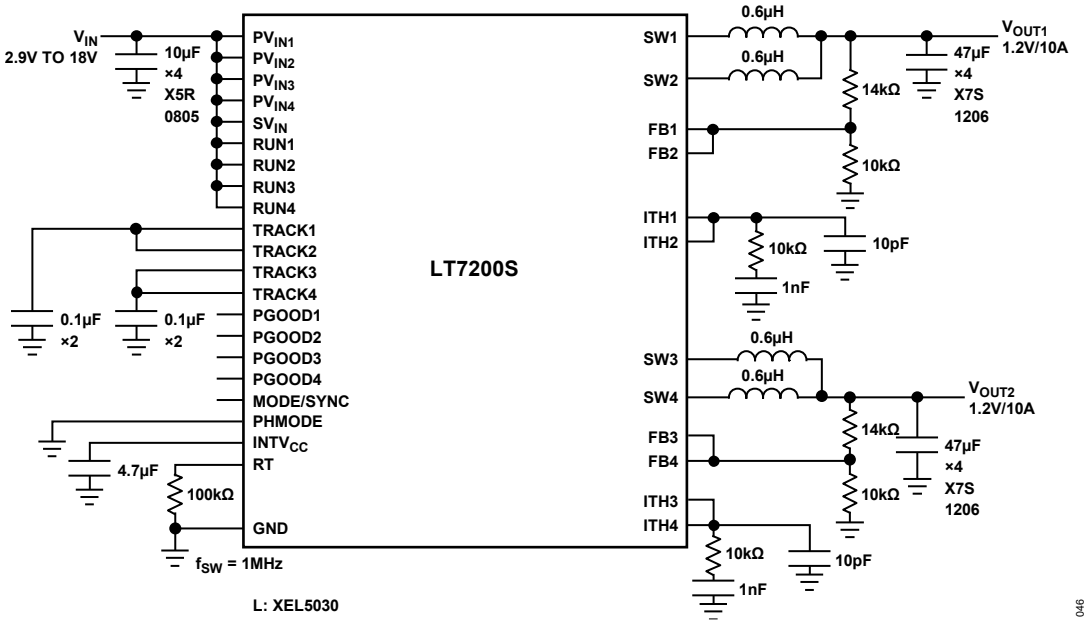


Figure 42. Dual 1.2V, 10A/10A Buck Regulator

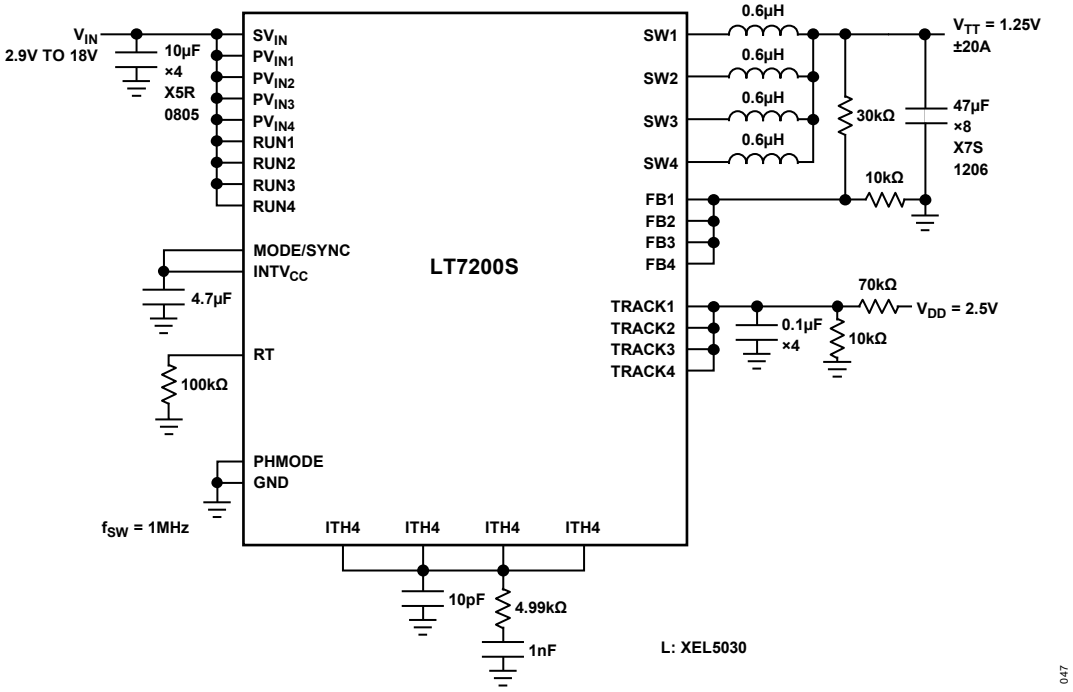


Figure 43. 4-Phase ±20A Single VTT DDR Power Supply

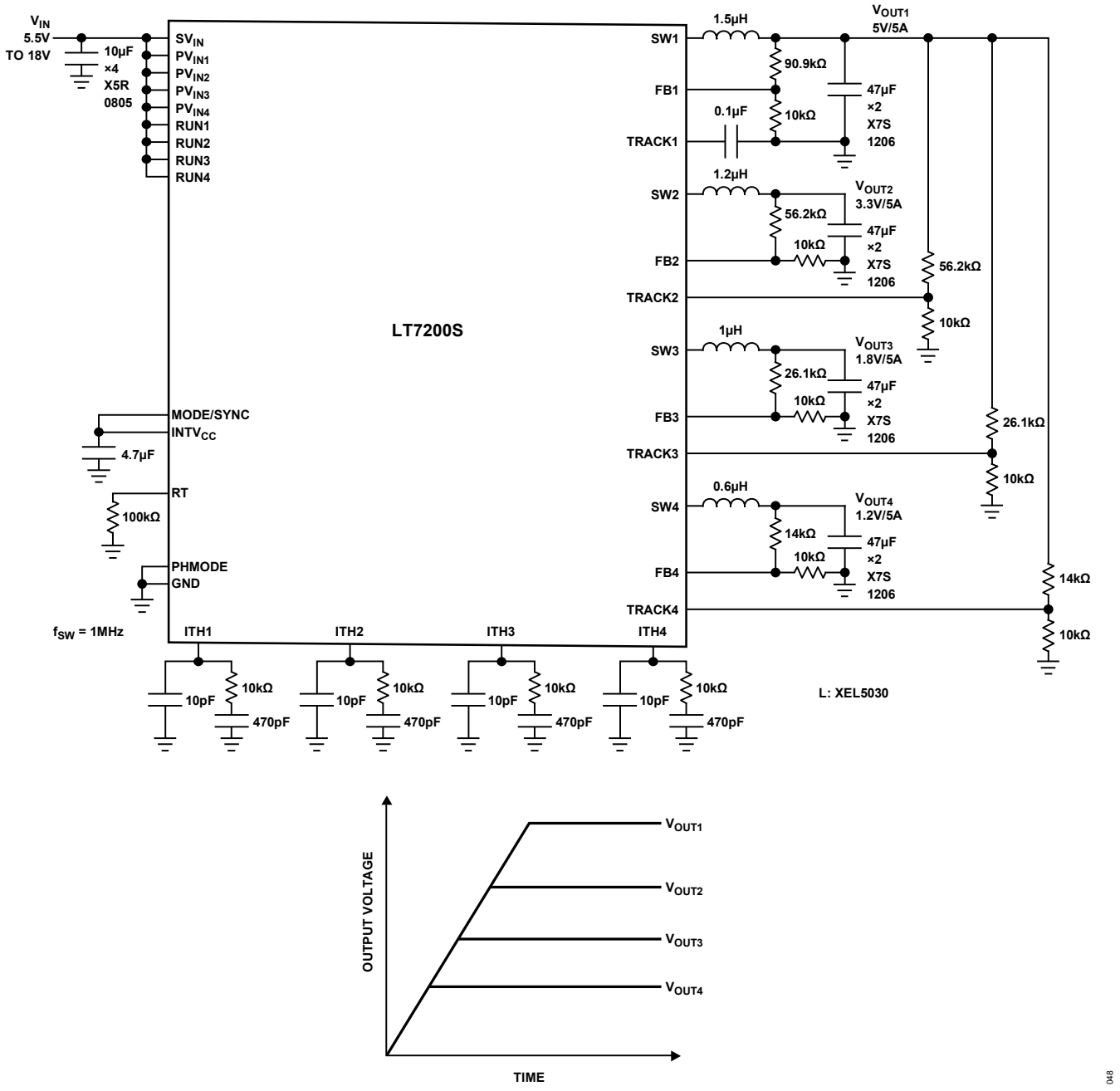


Figure 44. Quad 1.2V/5A, 1.8V/5A, 3.3V/5A, 5V/5A Buck Regulator with Coincident Tracking

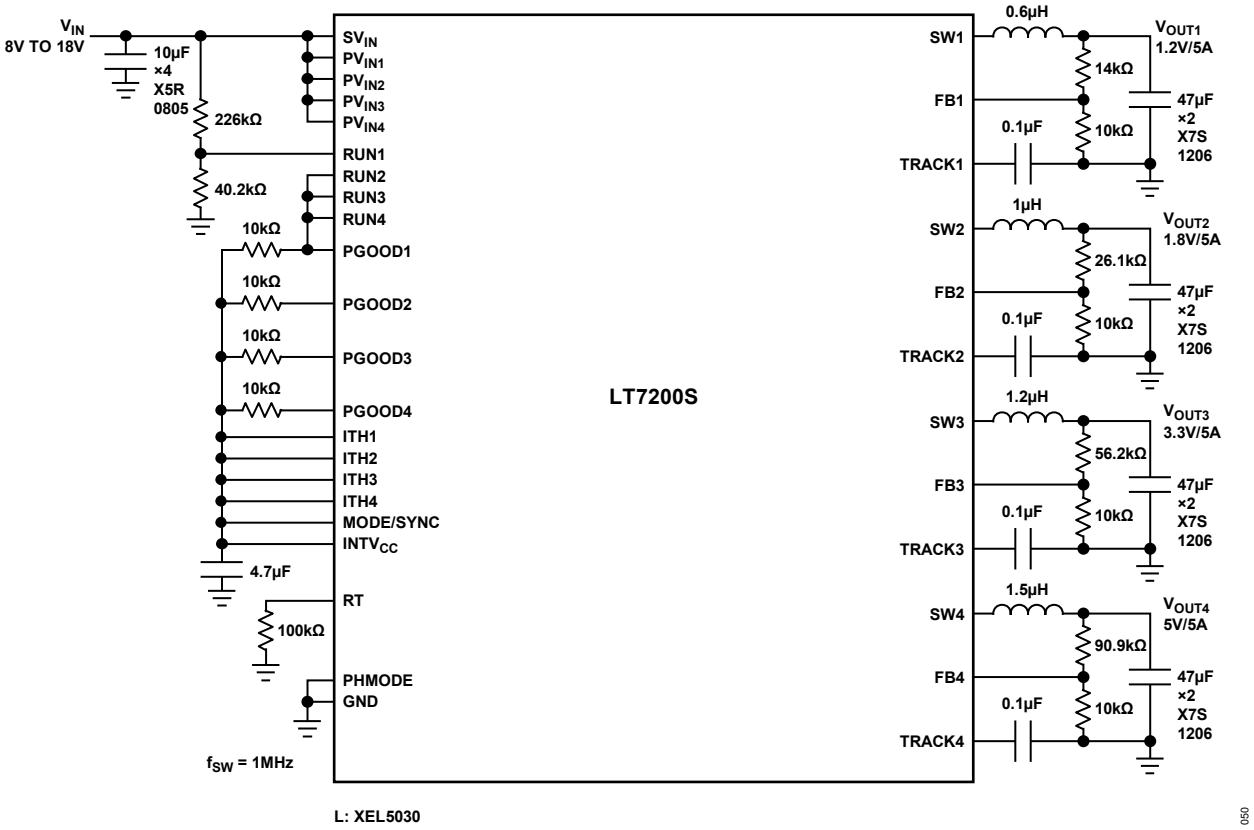
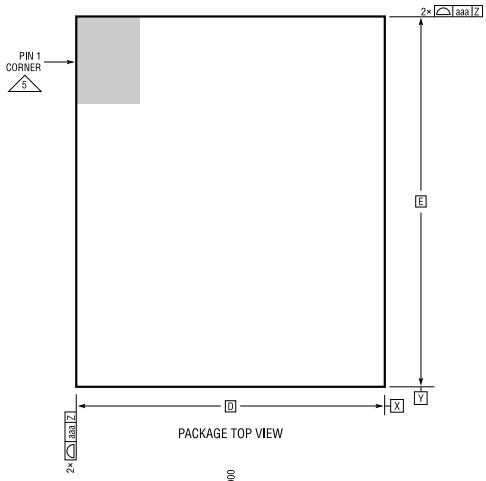
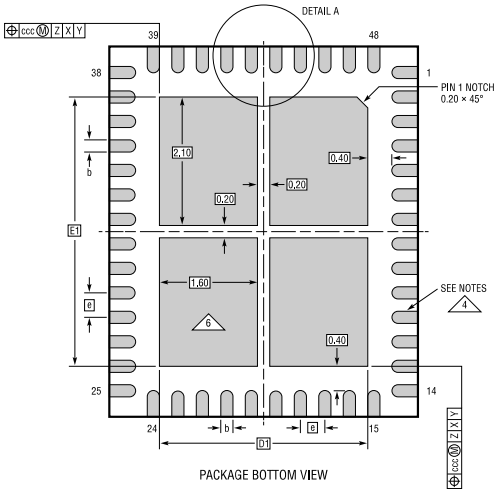


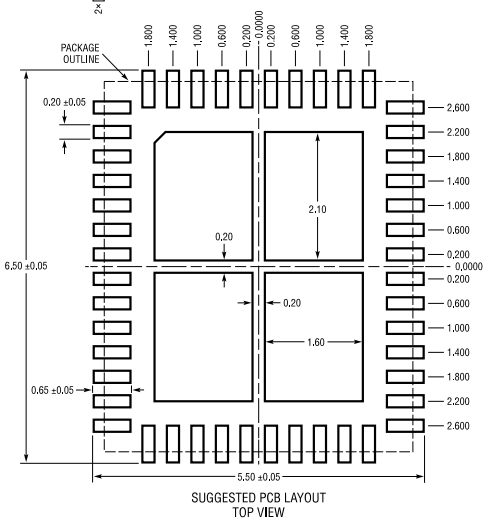
Figure 45. Quad 1.2V/5A, 1.8V/5A, 3.3V/5A, 5V/5A Sequenced Buck Regulator with 8V Input UVLO (VOUT2/3/4 Enabled by PGOOD1/2/3)

OUTLINE DIMENSIONS

LQFN Package
48-Lead (5mm × 6mm × 1.02mm)
(Reference LTC DWG # 05-08-1606 Rev B)

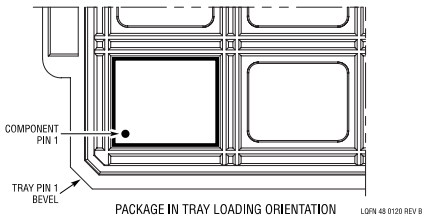






DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.93	1.02	1.11	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.17	0.20	0.23	
D		5.00		
E		6.00		
D1		3.40		
E1		4.40		
e		0.40		
H1		0.32 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT



ORDERING GUIDE

PART NUMBER	PART MARKING	FINISH CODE	PAD FINISH	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LT7200SAV#PBF	7200S	e4	Au(RoHS)	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C
LT7200SAV#TRPBF						

- Contact the factory for parts specified with wider operating temperature ranges.

  *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- *Recommended LGA and BGA PCB Assembly and Manufacturing Procedures*
- *LGA and BGA Package and Tray Drawings*

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3605/ LTC3605A	20V, 5A Synchronous Step-Down Regulator	4V < V_{IN} < 20V, 0.6V < V_{OUT} < 20V, 96% Maximum Efficiency, 4mm × 4mm QFN-24 Package
LTC3613	24V, 15A Monolithic Step-Down Regulator with Differential Output Sensing	4.5V < V_{IN} < 24V, 0.6V < V_{OUT} < 5.5V, 0.67% Output Voltage Accuracy, Valley Current Mode, Programmable from 200kHz to 1MHz, Current Sensing, 7mm × 9mm QFN-56 Package
LTC3622	17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current	2.7V < V_{IN} < 17V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 3mm × 4mm DFN-14 and MSOP-16 Package
LTC3623	15V, ±5A Rail-to-Rail Synchronous Buck Regulator	4V ≤ V_{IN} ≤ 15V, 0V < V_{OUT} < V_{IN} – 0.5V, Programmable Wire Drop Compensation, Current Sensing, 96% Maximum Efficiency, 3mm × 5mm QFN-24 Package
LTC3624	17V, 2A Synchronous Step-Down Regulator with 3.5µA Quiescent Current	2.7V < V_{IN} < 17V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 3.5µA IQ, Zero-Current Shutdown, 3mm × 3mm DFN-8 Package
LTC3633A/ LTC3633A-1	Dual Channel 3A, 20V Monolithic Synchronous Step-Down Regulator	3.6V < V_{IN} < 20V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 4mm × 5mm QFN-28 and TSSOP-28 Package
LTM4639	Low V_{IN} 20A DC/DC µModule® Step-Down Regulator	Complete 20A Switch Mode Power Supply, 2.375V < V_{IN} < 7V, 0.6V < V_{OUT} < 5.5V, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA Package
LTM4637	20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, 4.5V < V_{IN} < 20V, 0.6V < V_{OUT} < 5.5V, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA or LGA Package
LTC7130	20V, 20A Monolithic Buck Converter with Ultralow DCR Sensing	4.5V < V_{IN} < 20V, 95% Maximum Efficiency, Optimized for Low Duty Cycle Applications, 6.25mm × 7.5mm BGA Package