Buffered 8-Channel Simultaneous Sampling 20-Bit 1 MSPS Data Acquisition System

FEATURES

- Complete 20-bit Data Acquisition System (DAS)
  - Simultaneous sampling of 8 internally buffered channels
  - 1 MSPS per channel throughput
  - Differential, wide common mode range inputs
  - 75 pA / 40 nA input leakage at 25°C / 125°C
  - Full-scale input step settling < 1 µS
  - Integrated reference and reference buffer (4.096 V)
  - Integrated supply bypass capacitors
  - 45 mW / channel at 1 MSPS, power scales with throughput
- Minimal external signal conditioning
  - Seamless High Dynamic Range (SHDR)
    - Per-sample, per-channel automatic gain ranging
    - Maintains ppm-level INL
  - Per-channel SoftSpan™ input ranges
    - Bipolar: ±40 / 25 / 20 / 12.5 / 10 / 6.25 / 5 / 2.5 V
    - Unipolar: 0 V to 40 / 25 / 20 / 12.5 / 10 / 6.25 / 5 / 2.5 V
  - Rail-to-rail input overdrive tolerance
- High performance
  - INL: ±12 ppm maximum, from −40°C to +125°C
  - SNR: 97 dB single-conversion typical (±40 V range)
  - DR: 110 dB single-conversion typical (±40 V range)
  - THD: −115 dB typical
  - CMRR: 125 dB typical
- Digital flexibility
  - SPI CMOS (0.9 V to 5.25 V) and LVDS Serial I/O
  - Optional 24-bit oversampling with digital averaging
- 7 mm x 7 mm 64-Ball CSP_BGA full solution footprint

APPLICATIONS

- Automatic test equipment
- Avionics and aerospace
- Instrumentation and control systems
- Semiconductor manufacturing
- Test and measurement

FUNCTIONAL BLOCK DIAGRAM

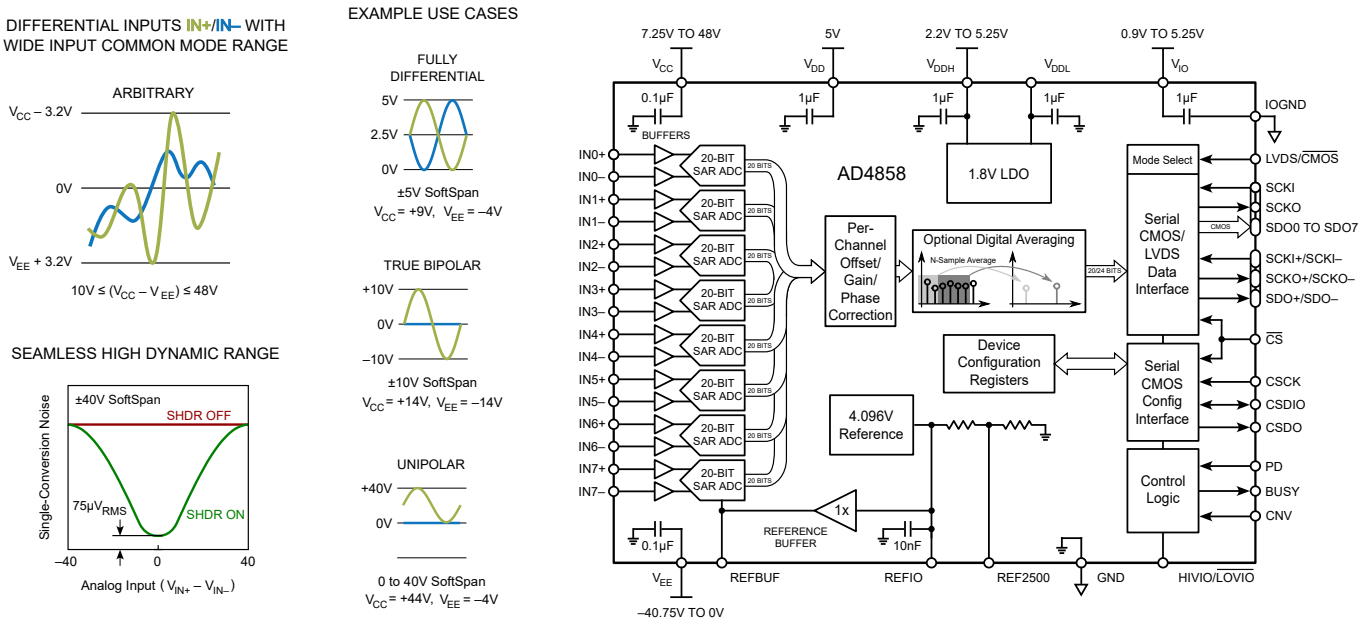

Figure 1. Functional Block Diagram. Some example analog input signal use cases shown

For more information about the AD4858, contact your local Analog Devices, Inc., sales office at www.analog.com/sales.

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GENERAL DESCRIPTION

The AD4858 is a fully buffered, 8-channel simultaneous sampling, 20-bit 1 MSPS data acquisition system (DAS) with differential, wide common mode range inputs. Its functional architecture is shown in Figure 1. Operating from a 5V low voltage supply, flexible high voltage supplies, and using the precision low drift internal reference and reference buffer, each channel's SoftSpan™ range can be independently configured to match the native application signal swing, minimizing additional external signal conditioning. To further maximize single-conversion dynamic range, the AD4858 incorporates seamless high dynamic range (SHDR) technology. When enabled, a channel's input signal path gain is automatically optimized on a sample-by-sample basis, minimizing converter noise on each sample without impacting linearity.

The 10 MHz bandwidth picoamp-input analog buffers, wide input common mode range and 125 dB CMRR of the AD4858 allow the DAS to directly digitize input signals with arbitrary swings on IN+ and IN−. This input signal flexibility, combined with ±12 ppm maximum INL, no missing codes at 20 bits, 97 dB SNR and 110 dB DR makes the AD4858 an ideal choice for applications requiring high accuracy, throughput and precision in a compact solution footprint. 24-bit oversampling offers further SNR and dynamic range improvements, while optional per-channel offset, gain and phase adjustment provide the ability to calibrate and remove system-level errors upstream to the DAS.

The AD4858 features a dedicated serial peripheral interface (SPI) Register Configuration Bus (0.9 V to 5.25 V) and pin selectable serial LVDS and CMOS Conversion Data Output buses. Between one and eight lines of data output may be employed in CMOS mode, allowing the user to optimize bus width and throughput.

The 7 mm x 7 mm 64-ball chip scale package ball grid array (CSP_BGA) of the AD4858 includes all critical power supply and reference bypass capacitors, minimizing full solution footprint and component count, and reducing sensitivity to application printed circuit board (PCB) layout. It operates over an extended industrial temperature range of −40°C to +125°C.

COMPANION PRODUCTS

- Voltage references: LTC6655 or ADR4540
- Power solutions: LT1761 or LT8330

SPECIFICATIONS

V_{EE} = −40.75 V to 0 V, V_{CC} = 7.25 V to 48 V, V_{CC} − V_{EE} = 10 V to 48 V, V_{DD} = 5 V, V_{DDH} = 2.5 V, 1.8 V LDO enabled, V_{IO} = 0.9 V to 5.25 V, all channels converting at sampling frequency (f_S) = 1 MSPS, internal reference and reference buffer enabled, all SoftSpan ranges, fully-differential input signal drive in SoftSpan 15, true bipolar/unipolar signal drive in other bipolar/unipolar SoftSpan ranges, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		20			Bits
ANALOG INPUTS					
Absolute Input Voltage	V_{INx+}, V_{INx-} to V_{CC} and V_{EE}	V_{EE} + 3.2		V_{CC} − 3.2	V
Differential Input Range	(V_{INx+} − V_{INx-}), V_{REF} = V_{REFBUF}/1.024				
	SoftSpan 15: ±10 × V_{REF} range	−10 × V_{REF}		10 × V_{REF}	V
	SoftSpan 14: 0 to 10 × V_{REF} range	0		10 × V_{REF}	V
	SoftSpan 13: ±6.25 × V_{REF} range	−6.25 × V_{REF}		6.25 × V_{REF}	V
	SoftSpan 12: 0 to 6.25 × V_{REF} range	0		6.25 × V_{REF}	V
	SoftSpan 11: ±5 × V_{REF} range	−5 × V_{REF}		5 × V_{REF}	V
	SoftSpan 10: 0 to 5 × V_{REF} range	0		5 × V_{REF}	V
	SoftSpan 9: ±3.125 × V_{REF} range	−3.125 × V_{REF}		3.125 × V_{REF}	V
	SoftSpan 8: 0 to 3.125 × V_{REF} range	0		3.125 × V_{REF}	V
	SoftSpan 7: ±2.5 × V_{REF} range	−2.5 × V_{REF}		2.5 × V_{REF}	V
	SoftSpan 6: 0 to 2.5 × V_{REF} range	0		2.5 × V_{REF}	V
	SoftSpan 5: ±1.5625 × V_{REF} range	−1.5625 × V_{REF}		1.5625 × V_{REF}	V
	SoftSpan 4: 0 to 1.5625 × V_{REF} range	0		1.5625 × V_{REF}	V
	SoftSpan 3: ±1.25 × V_{REF} range	−1.25 × V_{REF}		1.25 × V_{REF}	V
	SoftSpan 2: 0 to 1.25 × V_{REF} range	0		1.25 × V_{REF}	V
	SoftSpan 1: ±0.625 × V_{REF} range	−0.625 × V_{REF}		0.625 × V_{REF}	V
	SoftSpan 0: 0 to 0.625 × V_{REF} range	0		0.625 × V_{REF}	V
Common-Mode Input Range	V_{CM} = (V_{INx+} + V_{INx-})/2	V_{EE} + 3.2		V_{CC} − 3.2	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 36 V_{p_p} 200 Hz Sine	TBD	128		dB
Differential Input Overdrive Tolerance[1]	(V_{INx+} − V_{INx-})	−(V_{CC} − V_{EE})		(V_{CC} − V_{EE})	V
Input Overdrive Current Tolerance[1]	V_{INx+}, V_{INx-} > V_{CC}			10	mA
	V_{INx+}, V_{INx-} < V_{EE}	0			mA
Analog Input Leakage Current	V_{INx+}, V_{INx-} = V_{CC} to V_{EE}		0.075	40	nA
Analog Input Resistance	R_{INx+}, R_{INx-} for each pin		1000		GΩ
Analog Input Capacitance	C_{INx+}, C_{INx-} for each pin		3		pF
DC ACCURACY					
No Missing Codes		20			Bits
Integral Nonlinearity (INL) Error	SHDR ON	−12	±2	12	ppm
Differential Nonlinearity (DNL) Error		−0.9	±0.2		LSB
Transition Noise[2]	SHDR ON, near zero-scale		73		μV_{RMS}
	SHDR OFF				
	SoftSpans 15 and 14 : ±40 V and 0 to 40 V ranges		444		μV_{RMS}
	SoftSpans 13 and 12: ±25 V and 0 to 25 V ranges		276		μV_{RMS}
	SoftSpans 11 and 10: ±20 V and 0 to 20 V ranges		234		μV_{RMS}
	SoftSpans 9 and 8: ±12.5 V and 0 to 12.5 V ranges		150		μV_{RMS}
	SoftSpans 7 and 6: ±10 V and 0 to 10 V ranges		122		μV_{RMS}
	SoftSpans 5 and 4: ±6.25 V and 0 to 6.25 V ranges		92		μV_{RMS}
	SoftSpans 3 and 2: ±5 V and 0 to 5 V ranges		79		μV_{RMS}
	SoftSpans 1 and 0: ±2.5 V and 0 to 2.5 V ranges		73		μV_{RMS}
Zero-Scale Error		−350	±50	350	µV
Zero-Scale Error Drift			±1		µV/°C

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Full-Scale Error	V_{REFIO} = 4.096 V, REFIO overdriven[3]	−0.03	±0.005	0.03	%FS
Full-Scale Error Drift	V_{REFIO} = 4.096 V, REFIO overdriven[3]		±1		ppm/°C
AC ACCURACY[4]					
Dynamic Range (DR)	SHDR ON / OFF				
	SoftSpan 15: ±40 V range		111.5 / 96.1		dB
	SoftSpan 14: 0 to 40 V range		105.7 / 90.1		dB
	SoftSpan 13: ±25 V range		107.6 / 96.1		dB
	SoftSpan 12: 0 to 25 V range		101.7 / 90.1		dB
	SoftSpan 11: ±20 V range		105.7 / 95.6		dB
	SoftSpan 10: 0 to 20 V range		99.8 / 89.6		dB
	SoftSpan 9: ±12.5 V range		101.7 / 95.4		dB
	SoftSpan 8: 0 to 12.5 V range		95.7 / 89.4		dB
	SoftSpan 7: ±10 V range		99.8 / 95.2		dB
	SoftSpan 6: 0 to 10 V range		93.8 / 89.2		dB
	SoftSpan 5: ±6.25 V range		95.7 / 93.6		dB
	SoftSpan 4: 0 to 6.25 V range		89.7 / 87.6		dB
	SoftSpan 3: ±5 V range		93.8 / 93		dB
	SoftSpan 2: 0 to 5 V range		87.8 / 87		dB
	SoftSpan 1: ±2.5 V range		87.8 / 87.8		dB
	SoftSpan 0: 0 to 2.5 V range		81.8 / 81.8		dB
Oversampled Dynamic Range (ODR)	V_{REFIO} = 4.096 V, REFIO overdriven[3]				
	OSR = 2		DR + 3		dB
	OSR = 32		DR + 15		dB
	OSR = 1024		DR + TBD		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio	SHDR ON, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	TBD	97		dB
	SoftSpan 14: 0 to 40 V range	TBD	TBD		dB
	SoftSpan 13: ±25 V range	TBD	TBD		dB
	SoftSpan 12: 0 to 25 V range	TBD	TBD		dB
	SoftSpan 11: ±20 V range	TBD	TBD		dB
	SoftSpan 10: 0 to 20 V range	TBD	TBD		dB
	SoftSpan 9: ±12.5 V range	TBD	TBD		dB
	SoftSpan 8: 0 to 12.5 V range	TBD	TBD		dB
	SoftSpan 7: ±10 V range	TBD	TBD		dB
	SoftSpan 6: 0 to 10 V range	TBD	TBD		dB
	SoftSpan 5: ±6.25 V range	TBD	TBD		dB
	SoftSpan 4: 0 to 6.25 V range	TBD	TBD		dB
	SoftSpan 3: ±5 V range	TBD	TBD		dB
	SoftSpan 2: 0 to 5 V range	TBD	TBD		dB
	SoftSpan 1: ±2.5 V range	TBD	TBD		dB
	SoftSpan 0: 0 to 2.5 V range	TBD	TBD		dB
	SHDR OFF, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	TBD	96		dB
	SoftSpan 14: 0 to 40 V range	TBD	TBD		dB
	SoftSpan 13: ±25 V range	TBD	TBD		dB
	SoftSpan 12: 0 to 25 V range	TBD	TBD		dB
	SoftSpan 11: ±20 V range	TBD	TBD		dB
	SoftSpan 10: 0 to 20 V range	TBD	TBD		dB
	SoftSpan 9: ±12.5 V range	TBD	TBD		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	SoftSpan 8: 0 to 12.5 V range	TBD	TBD		dB
	SoftSpan 7: ±10 V range	TBD	TBD		dB
	SoftSpan 6: 0 to 10 V range	TBD	TBD		dB
	SoftSpan 5: ±6.25 V range	TBD	TBD		dB
	SoftSpan 4: 0 to 6.25 V range	TBD	TBD		dB
	SoftSpan 3: ±5 V range	TBD	TBD		dB
	SoftSpan 2: 0 to 5 V range	TBD	TBD		dB
	SoftSpan 1: ±2.5 V range	TBD	TBD		dB
	SoftSpan 0: 0 to 2.5 V range	TBD	TBD		dB
Signal-to-Noise Ratio (SNR)	SHDR ON, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	TBD	97		dB
	SoftSpan 14: 0 to 40 V range	TBD	TBD		dB
	SoftSpan 13: ±25 V range	TBD	TBD		dB
	SoftSpan 12: 0 to 25 V range	TBD	TBD		dB
	SoftSpan 11: ±20 V range	TBD	TBD		dB
	SoftSpan 10: 0 to 20 V range	TBD	TBD		dB
	SoftSpan 9: ±12.5 V range	TBD	TBD		dB
	SoftSpan 8: 0 to 12.5 V range	TBD	TBD		dB
	SoftSpan 7: ±10 V range	TBD	TBD		dB
	SoftSpan 6: 0 to 10 V range	TBD	TBD		dB
	SoftSpan 5: ±6.25 V range	TBD	TBD		dB
	SoftSpan 4: 0 to 6.25 V range	TBD	TBD		dB
	SoftSpan 3: ±5 V range	TBD	TBD		dB
	SoftSpan 2: 0 to 5 V range	TBD	TBD		dB
	SoftSpan 1: ±2.5 V range	TBD	TBD		dB
	SoftSpan 0: 0 to 2.5V range	TBD	TBD		dB
	SHDR OFF, f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	TBD	96		dB
	SoftSpan 14: 0 to 40 V range	TBD	TBD		dB
	SoftSpan 13: ±25 V range	TBD	TBD		dB
	SoftSpan 12: 0 to 25 V range	TBD	TBD		dB
	SoftSpan 11: ±20 V range	TBD	TBD		dB
	SoftSpan 10: 0 to 20 V range	TBD	TBD		dB
	SoftSpan 9: ±12.5 V range	TBD	TBD		dB
	SoftSpan 8: 0 to 12.5 V range	TBD	TBD		dB
	SoftSpan 7: ±10 V range	TBD	TBD		dB
	SoftSpan 6: 0 to 10 V range	TBD	TBD		dB
	SoftSpan 5: ±6.25 V range	TBD	TBD		dB
	SoftSpan 4: 0 to 6.25 V range	TBD	TBD		dB
	SoftSpan 3: ±5 V range	TBD	TBD		dB
	SoftSpan 2: 0 to 5 V range	TBD	TBD		dB
	SoftSpan 1: ±2.5 V range	TBD	TBD		dB
	SoftSpan 0: 0 to 2.5 V range	TBD	TBD		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range		−TBD	−TBD	dB
	SoftSpan 14: 0 to 40 V range		−TBD	−TBD	dB
	SoftSpan 13: ±25 V range		−TBD	−TBD	dB
	SoftSpan 12: 0 to 25 V range		−TBD	−TBD	dB
	SoftSpan 11: ±20 V range		−TBD	−TBD	dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	SoftSpan 10: 0 to 20 V range		−TBD	−TBD	dB
	SoftSpan 9: ±12.5 V range		−TBD	−TBD	dB
	SoftSpan 8: 0 to 12.5 V range		−TBD	−TBD	dB
	SoftSpan 7: ±10 V range		−TBD	−TBD	dB
	SoftSpan 6: 0 to 10 V range		−TBD	−TBD	dB
	SoftSpan 5: ±6.25 V range		−TBD	−TBD	dB
	SoftSpan 4: 0 to 6.25 V range		−TBD	−TBD	dB
	SoftSpan 3: ±5 V range		−TBD	−TBD	dB
	SoftSpan 2: 0 to 5 V range		−TBD	−TBD	dB
	SoftSpan 1: ±2.5 V range		−TBD	−TBD	dB
	SoftSpan 0: 0 to 2.5 V range		−TBD	−TBD	dB
Spurious Free Dynamic Range (SFDR)	f_{IN} = 1 kHz, −1 dBFS				
	SoftSpan 15: ±40 V range	TBD	TBD		dB
	SoftSpan 14: 0 to 40 V range	TBD	TBD		dB
	SoftSpan 13: ±25 V range	TBD	TBD		dB
	SoftSpan 12: 0 to 25 V range	TBD	TBD		dB
	SoftSpan 11: ±20 V range	TBD	TBD		dB
	SoftSpan 10: 0 to 20 V range	TBD	TBD		dB
	SoftSpan 9: ±12.5 V range	TBD	TBD		dB
	SoftSpan 8: 0 to 12.5 V range	TBD	TBD		dB
	SoftSpan 7: ±10 V range	TBD	TBD		dB
	SoftSpan 6: 0 to 10 V range	TBD	TBD		dB
	SoftSpan 5: ±6.25 V range	TBD	TBD		dB
	SoftSpan 4: 0 to 6.25 V range	TBD	TBD		dB
	SoftSpan 3: ±5 V range	TBD	TBD		dB
	SoftSpan 2: 0 to 5 V range	TBD	TBD		dB
	SoftSpan 1: ±2.5 V range	TBD	TBD		dB
	SoftSpan 0: 0 to 2.5 V range	TBD	TBD		dB
Channel-to-Channel Crosstalk	f_{inj} = 100 kHz, f_{rcv} = 1 kHz, all channels converting		−135		dB
−3dB Input Bandwidth			10		MHz
Aperture Delay			1		ns
Aperture Delay Matching			TBD		ps
Aperture Jitter			TBD		ps_{RMS}
Transient Response	Full-scale step, 0.005% settling, T_A = 25°C		420		ns
INTERNAL REFERENCE ENABLED					
Internal Reference Output Voltage (V_{REFIO})	T_A = 25°C	4.094	4.096	4.098	V
Internal Reference Temperature Coefficient[5]		−10	±2	10	ppm/°C
Internal Reference Line Regulation	V_{DD} = 4.75 V to 5.25 V		0.1		mV/V
REFIO Output Resistance			58		Ω
REFIO Output Capacitance			10		nF
INTERNAL REFERENCE DISABLED	REFIO overdriven[6]				
REFIO Input Voltage (V_{REFIO})		4.071	4.096	4.121	V
REFIO Input Resistance			38		kΩ
REFIO Input Capacitance			10		nF
REFERENCE BUFFER ENABLED					
Reference Buffer Offset Voltage (V_{os})	V_{os} = (V_{REFBUF} − V_{REFIO}), T_A = 25°C	−100	±20	100	µV
Reference Buffer Offset Voltage Drift			±0.2		µV/°C
REFERENCE BUFFER DISABLED	REFBUF overdriven[7]				

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFBUF Input Voltage (V_{REFBUF})		4.071	4.096	4.121	V
REFBUF Input Current (I_{REFBUF})[8]	V_{REFBUF} = 4.096 V, f_s = 1 MSPS		3.3	4.5	mA
	V_{REFBUF} = 4.096 V, not converting		2.2		mA
SCALED REFERENCE OUTPUT					
REF2500 Output Voltage ($V_{REF2500}$)	V_{REFIO} = 4.096 V, REFIO overdriven[3], T_A = 25°C	2.498	2.5	2.502	V
REF2500 Temperature Coefficient[5]	V_{REFIO} = 4.096 V, REFIO overdriven[3]	TBD	±1	TBD	ppm/°C
REF2500 Output Resistance			26		kΩ
CMOS DIGITAL INPUTS					
Input Voltage High (V_{IH})					
CNV		0.7			V
HIVIO/$\overline{\text{LOVIO}}$		4			V
All other pins		0.85 × V_{IO}			V
Input Voltage Low (V_{IL})					
CNV				0.4	V
HIVIO/$\overline{\text{LOVIO}}$				1	V
All other pins				0.15 × V_{IO}	V
Digital Input Current (I_{IN})					
CNV		−100		100	µA
HIVIO/$\overline{\text{LOVIO}}$		−10		10	µA
All other pins		−10		10	µA
Digital Input Capacitance (C_{IN})			2		pF
CMOS DIGITAL OUTPUTS					
Output Voltage High (V_{OH})	Source current (I_{SOURCE}) = 500 µA	V_{IO} − 0.2			V
Output Voltage Low (V_{OL})	Sink current (I_{SINK}) = 500 µA			0.2	V
Hi-Z Output Leakage Current (I_{OZ})		−10		10	µA
LVDS DIGITAL INPUTS					
Differential Input Voltage (V_{ID})		±200	±350	±600	mV
Differential Termination Resistance (R_{ID})	$\overline{CS}$ = 0 V, V_{ICM} = 1.2 V, termination enabled[9]	90	106	125	Ω
	$\overline{CS}$ = V_{IO} or termination disabled[9]		10		MΩ
Common Mode Input Voltage (V_{ICM})	1.71 V ≤ V_{IO} < 2.5 V	0.3	1.2	V_{IO} − 0.3	V
	2.5 V ≤ V_{IO} ≤ 5.25V	0.3	1.2	2.2	V
Common Mode Input Current (I_{ICM})		−10		10	µA
LVDS DIGITAL OUTPUTS					
Differential Output Voltage (V_{OD})	R_L = 100 Ω differential termination, full-bias mode[9]	±250	±350	±450	mV
	R_L = 100 Ω differential termination, half-bias mode[9]	±120	±185	±250	mV
Common-Mode Output Voltage (V_{OCM})	R_L = 100 Ω differential termination	1.1	1.25	1.4	V
Hi-Z Output Leakage Current (I_{OZ})		−10		10	µA
POWER SUPPLY VOLTAGES					
V_{CC}		7.25		48	V
V_{EE}		−40.75		0	V
V_{CC} − V_{EE}		10		48	V
V_{DD}		4.75	5.0	5.25	V
V_{DDH}	Disables 1.8 V LDO		0		V
	Enables 1.8 V LDO	2.2		5.25	V
V_{DDL}	Supplied externally, 1.8 V LDO disabled	1.71	1.8	1.89	V
	Supplied by 1.8 V LDO, no external connection		1.8		V
V_{IO}					
CMOS Conversion Data Output	HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	1.71		5.25	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	HIVIO/$\overline{\text{LOVIO}}$ = GND	0.9		1.89	V
LVDS Conversion Data Output	HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	1.71		5.25	V
	HIVIO/$\overline{\text{LOVIO}}$ = GND	1.71		1.89	V
POWER SUPPLY CURRENTS					
CMOS Conversion Data Output	C_L = 25 pF on CMOS outputs				
Operating Mode[10]	f_S = 1 MSPS, all channels converting				
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		15.2	18.3	mA
	V_{CC} = 15 V, V_{EE} = –15 V		13		mA
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		10.7		mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–14.4	–12		mA
	V_{CC} = 15 V, V_{EE} = –15 V		–10.2		mA
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		–8		mA
I_{VDD}	Reference and reference buffer enabled		15.7	23.7	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		13.9		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		3.7		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		60	85	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		58	83	mA
I_{VIO}	V_{IO} = 2.5 V		6	7.5	mA
Acquisition Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		9.7	11.7	mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–9	–7.5		mA
I_{VDD}	Reference and reference buffer enabled		10.8	17.9	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		8.9		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		1.2		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		0.08	1	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		0.02	1	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
Nap Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		4.6	5.6	mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–4	–3.3		mA
I_{VDD}	Reference and reference buffer enabled		10.8	17.9	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		8.2		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		1.2		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		0.08	1	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		0.02	1	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
Power Down Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		18	200	µA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V		–4	–40	µA
I_{VDD}			0.13	1.3	mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		0.02	1	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		0.01	1	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
LVDS Conversion Data Output	R_L = 100 Ω differential on LVDS outputs				
Operating Mode	f_S = 1 MSPS, all channels converting				
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		15.2	18.3	mA
	V_{CC} = 15 V, V_{EE} = –15 V		13		mA
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		10.7		mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–14.4	–12		mA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{CC} = 15 V, V_{EE} = –15 V		–10.2		mA
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		–8		mA
I_{VDD}	Reference and reference buffer enabled		19.2	28	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		TBD		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		7.7		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		69	97	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		68	96	mA
I_{VIO}	V_{IO} = 2.5 V		82	165	µA
Acquisition Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		9.7	11.7	mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–9	–7.5		mA
I_{VDD}	Reference and reference buffer enabled		12.3	19.7	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		TBD		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		TBD		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		9	11.9	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		9	11.9	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
Nap Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		4.6	5.6	mA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V	–4	–3.3		mA
I_{VDD}	Reference and reference buffer enabled		11.5	18.7	mA
	V_{REFIO} = 4.096 V, REFIO overdriven[6]		TBD		mA
	V_{REFBUF} = 4.096 V, REFBUF overdriven[7]		TBD		mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		9	11.9	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		9	11.9	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
Power Down Mode					
I_{VCC}	V_{CC} = 24 V, V_{EE} = –24 V		18	200	µA
I_{VEE}	V_{CC} = 24 V, V_{EE} = –24 V		–4	–40	µA
I_{VDD}			0.13	1.3	mA
I_{VDDH}	V_{DDH} = 2.5 V, 1.8 V LDO enabled		0.02	1	mA
I_{VDDL}	V_{DDH} = GND, 1.8 V LDO disabled, V_{DDL} = 1.8 V		0.01	1	mA
I_{VIO}	V_{IO} = 2.5 V		1	10	µA
POWER DISSIPATION	Reference and reference buffer enabled, V_{DDH} = 2.5 V, 1.8 V LDO enabled, V_{IO} = 2.5 V				
CMOS Conversion Data Output	C_L = 25 pF on CMOS outputs				
Operation Mode	f_S = 1 MSPS, all channels converting				
	V_{CC} = 24 V, V_{EE} = –24 V		897	1135	mW
	V_{CC} = 15 V, V_{EE} = –15 V		592		mW
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		357		mW
Acquisition Mode	V_{CC} = 24 V, V_{EE} = –24 V		468	589	mW
Nap Mode	V_{CC} = 24 V, V_{EE} = –24 V		244	323	mW
Power Down Mode	V_{CC} = 24 V, V_{EE} = –24 V		1.3	15	mW
LVDS Conversion Data Output	R_L = 100 Ω differential on LVDS outputs				
Operation Mode	f_S = 1 MSPS, all channels converting				
	V_{CC} = 24 V, V_{EE} = –24 V		922	1168	mW
	V_{CC} = 15 V, V_{EE} = –15 V		617		mW
	V_{CC} = 8.2 V, V_{EE} = –3.2 V		383		mW
Acquisition Mode	V_{CC} = 24 V, V_{EE} = –24 V		497	626	mW

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Nap Mode	V_{CC} = 24 V, V_{EE} = –24 V		270	354	mW
Power Down Mode	V_{CC} = 24 V, V_{EE} = –24 V		1.3	15	mW
OPERATING TEMPERATURE RANGE					
T_{MIN}		–40			°C
T_{MAX}				125	°C

[1] Exceeding these limits on any channel may corrupt conversion results on other channels. Driving an analog input above V_{CC} on any channel up to 10mA will not affect conversion results on other channels. Driving an analog input below V_{EE} may corrupt conversion results on other channels. Refer to Applications Information section for further details. Refer to Absolute Maximum Ratings section for pin voltage and current limits related to device reliability.

[2] A plot of transition noise versus input signal amplitude with SHDR ON and OFF is shown in Figure 24.

[3] These specifications are measured while externally supplying V_{REFIO} = 4.096 V with the internal bandgap reference powered down. They do not include nominal value, temperature drift or noise terms associated with the internal bandgap.

[4] All specifications in dB are referred to a full-scale input in the relevant SoftSpan input range, except for crosstalk, which is referred to the crosstalk injection signal amplitude.

[5] Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range (T_{MAX} – T_{MIN}).

[6] When REFIO is overdriven, the internal bandgap reference must be disabled though the Device Control Register.

[7] When REFBUF is overdriven, the internal bandgap reference and reference buffer must be disabled though the Device Control Register.

[8] I_{REFBUF} varies proportionally with the sample rate and the number of active channels.

[9] Enable or disable the LVDS termination resistance and half-bias mode through the Device Control Register.

[10] A plot of operating operating mode power dissipation versus number of active channels and sample rate is shown in Typical Performance Characteristics.

TIMING SPECIFICATIONS

V_{EE} = −40.75 V to 0 V, V_{CC} = 7.25 V to 48 V, V_{CC} − V_{EE} = 10 V to 48 V, V_{DD} = 5 V, V_{DDH} = 2.5 V, 1.8 V LDO enabled, V_{IO} = 0.9 V to 5.25 V, all channels converting at sampling frequency (f_S) = 1 MSPS, internal reference and reference buffer enabled, all SoftSpan ranges, fully-differential input signal drive in SoftSpan 15, true bipolar/unipolar signal drive in other bipolar/unipolar SoftSpan ranges, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C. Interface timing tested using a load capacitance C_L = 25pF on CMOS outputs, a differential termination resistance R_L = 100 Ω between LVDS output differential pairs, internal termination resistance enabled on LVDS input differential pairs, LVDS full-bias mode enabled, and common-mode input voltage V_{ICM} = 1.2 V and differential input voltage V_{ID} = ±350 mV on LVDS input differential pairs.

Table 2. Universal Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_S	0		1	MSPS
Time Between Conversions	t_{CYC}	1			µs
Conversion Time	t_{CONV}	635	675	715	ns
Acquisition Phase[1]	t_{ACQ}	465			ns
CNV High Time	t_{CNVH}	40			ns
CNV Low Time	t_{CNVL}	750			ns
CNV Rising Edge to BUSY Rising Edge Delay	$t_{DCNVBUSY}$			20	ns
Data Valid to BUSY Falling Edge Delay	$t_{DSDOBUSY}$	3			ns
Last SCKI Edge to CNV Rising Edge	$t_{SCKICNV}$	20			ns
PD High Time	t_{PDH}	40			ns
PD Low Time	t_{PDL}	40			ns
Device Wake Time to Start of Valid Conversion	t_{WAKE}			1	ms
Device Power-on-Reset Time	t_{POR}			1	ms

[1] The acquisition phase is the time available for the ADCs acquire a new input with the DAS running at a throughput rate of 1 MSPS

SPECIFICATIONS

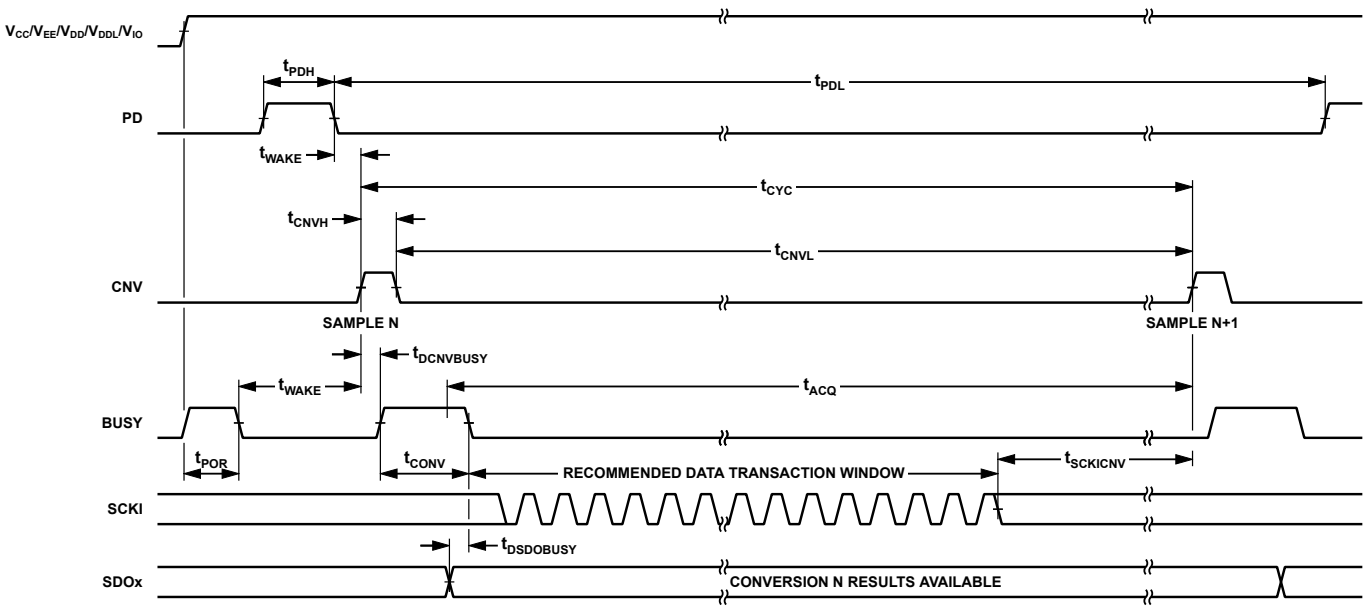


Figure 2. Universal Timing

Table 3. SPI Register Configuration Bus Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Low Time	t_{CSL}	15			ns
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Falling Edge to First CSCK Rising Edge	t_{CSCSCK}	15			ns
CSCK Period	t_{CSCK}	40			ns
CSCK Low Time	t_{CSCKL}	16			ns
CSCK High Time	t_{CSCKH}	16			ns
Last CSCK Edge to $\overline{CS}$ Rising Edge	t_{CSCKCS}	15			ns
CSDIO Valid Setup Time to CSCK Rising Edge	$t_{SCSDIOI}$	4			ns
CSDIO Valid Hold Time from CSCK Rising Edge	$t_{HCSDIOI}$	1			ns
CSCK 16th Rising Edge to CSDIO 3-Wire Output State Delay	t_{DIO}	2		10	ns
CSCK Falling Edge to CSDIO Data Valid Delay	$t_{DCSDIOO}$			10	ns
CSCK Falling Edge to CSDIO Data Remains Valid	$t_{HCSDIOO}$	2			ns
CSCK Falling Edge to CSDO Data Valid Delay	t_{DCSDO}			10	ns
CSCK Falling Edge to CSDO Data Remains Valid	t_{HCSDO}	2			ns
$\overline{CS}$ Falling Edge to 4-wire Bus Low Impedance Delay	t_{DCSEN}			15	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns

SPECIFICATIONS

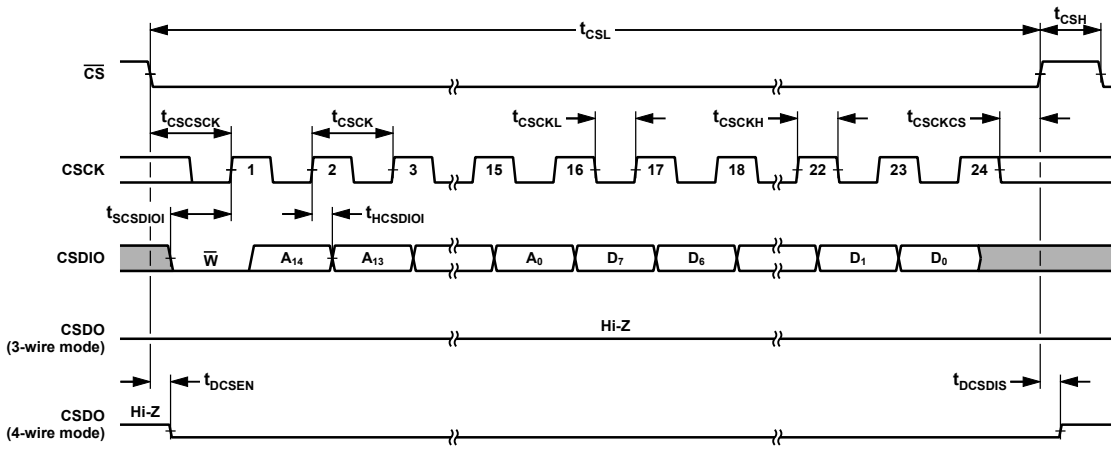


Figure 3. SPI Register Configuration Bus Write Timing

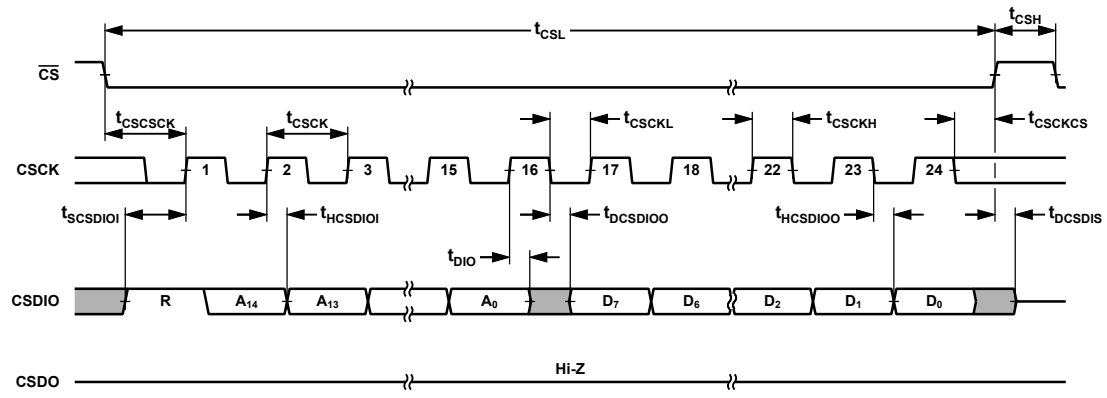


Figure 4. SPI Register Configuration Bus 3-Wire Read Timing

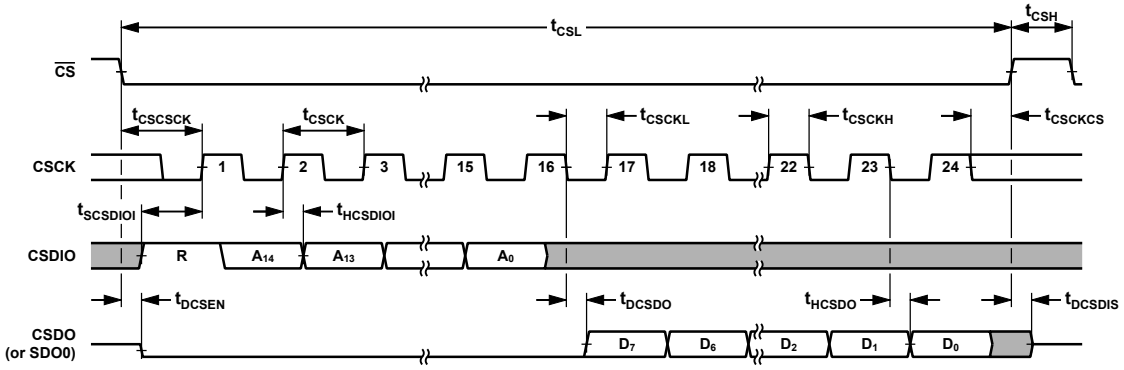


Figure 5. SPI Register Configuration Bus 4-Wire Read Timing

SPECIFICATIONS

Table 4. CMOS Conversion Data Output Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCKI Period	t_{SCKI}	10			ns
SCKI High Time	t_{SCKIH}	4			ns
SCKI Low Time	t_{SCKIL}	4			ns
SCKI Rising Edge to SDOx Data Valid Delay	t_{DSDO}			7.5	ns
SCKI Rising Edge to SDOx Remains Valid	t_{HSDO}	1.5			ns
Skew Between SDOx Data and SCKO	t_{SKEW}	−1	0	1	ns
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Low Time	t_{CSL}	15			ns
$\overline{CS}$ Falling Edge to Bus Low Impedance Delay	t_{DCSEN}			15	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns
$\overline{CS}$ Falling Edge to First SCKI Rising Edge	t_{CSSCKI}	15			ns
Last SCKI Edge to $\overline{CS}$ Rising Edge	t_{SCKICS}	15			ns

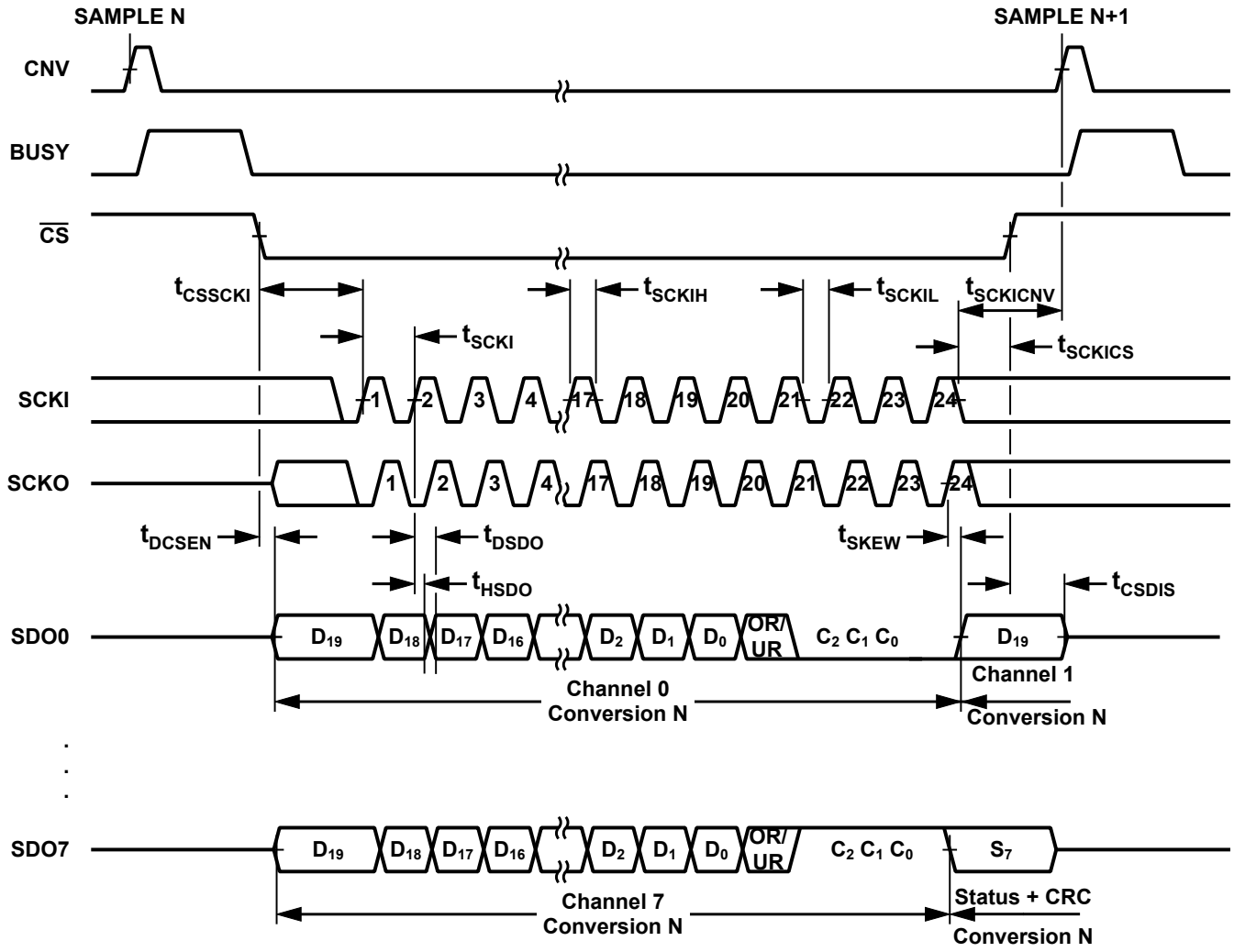


Figure 6. CMOS Conversion Data Bus Timing

SPECIFICATIONS

Table 5. LVDS Conversion Data Output Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCKI Period	t_{SCKI}	2.5			ns
SCKI High Time	t_{SCKIH}	0.75			ns
SCKI Low Time	t_{SCKIL}	0.75			ns
SCKI Edge to SDO Data Valid Delay	t_{DSDO}			7.5	ns
SCKI Edge to SDO Data Remains Valid	t_{HSDO}	1.5			
SDO to SCKO Skew	t_{SKEW}	−0.25	0	0.25	ns
$\overline{CS}$ High Time	t_{CSH}	75			ns
$\overline{CS}$ Low Time	t_{CSL}	15			ns
$\overline{CS}$ Falling Edge to Bus Low Impedance Delay	t_{DCSEN}			75	ns
$\overline{CS}$ Rising Edge to Bus High Impedance Delay	t_{DCSDIS}			15	ns
$\overline{CS}$ Falling Edge to First SCKI Rising Edge	t_{CSSCKI}	75			
Last SCKI Falling Edge to $\overline{CS}$ Rising Edge	t_{SCKICS}	15			

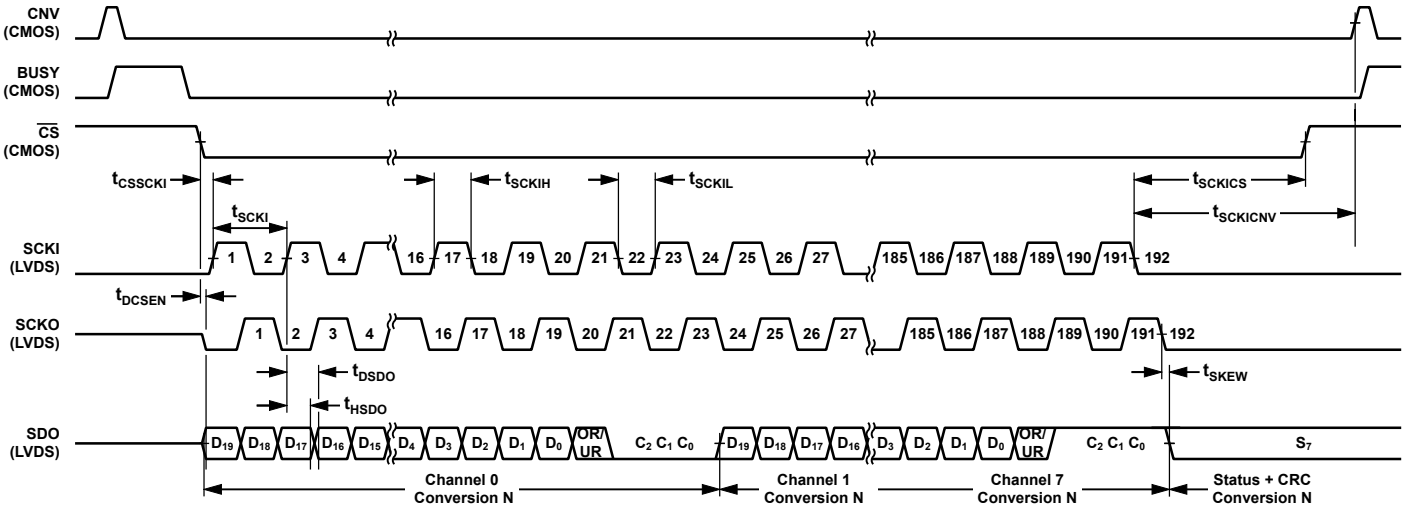


Figure 7. LVDS Conversion Data Bus Timing

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
Analog Input and Output Voltages	
IN0+ to IN7+, IN0− to IN7−	(V_{EE} − 0.3 V) to (V_{CC} + 0.3 V)
REFIO, REFBUF, REF2500 to GND	−0.3 V to (V_{DD} + 0.3 V)
Supply Voltages	
V_{CC} to GND	−0.3 V to (V_{EE} + 50.4 V)
V_{EE} to GND	(V_{CC} − 50.4 V) to 0.3 V
V_{CC} to V_{EE}	50.4V
V_{DD} , V_{DDH} to GND	−0.3V to 6V
V_{DDL} to GND	−0.3V to 2.1V
V_{IO} to GND[1]	
HIVIO/$\overline{\text{LOVIO}}$ = GND	−0.3V to 2.1V
HIVIO/$\overline{\text{LOVIO}}$ = V_{DD}	−0.3V to 6 V
IOGND to GND	−0.3V to 0.3V
Digital Input Voltages	
CNV, HIVIO/$\overline{\text{LOVIO}}$ to GND	−0.3 V to (V_{DD} + 0.3 V)
All other inputs to GND	−0.3 V to (V_{IO} + 0.3 V)
Digital Output Voltages	−0.3 V to (V_{IO} + 0.3 V)
Transient Latch-up Currents[2]	
IN0+ to IN7+, IN0− to IN7−	
V_{CC} − V_{EE} ≤ 44 V	±100 mA
V_{CC} − V_{EE} > 44 V	±10 mA
All other inputs and outputs	±100 mA
Temperature	
Storage Range	−65°C to +150°C
Operating Junction Range	−40°C to +125°C
Maximum Reflow (Package)	260°C

[1] The Absolute Maximum Ratings of V_{IO} depends on the selected state of HIVIO/$\overline{\text{LOVIO}}$

[2] Adding an external resistor in series with each INx+ and INx– pin is recommended in applications where V_{CC} − V_{EE} > 44 to limit latch-up current to these levels during fault conditions. See section TBD for further information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JCtop}	θ_{JCbot}	Unit
05-08-7086	26.4	13.0	4.9	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD RATINGS FOR AD4858

Table 8. AD4858, 64-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
FICDM	750	C4

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

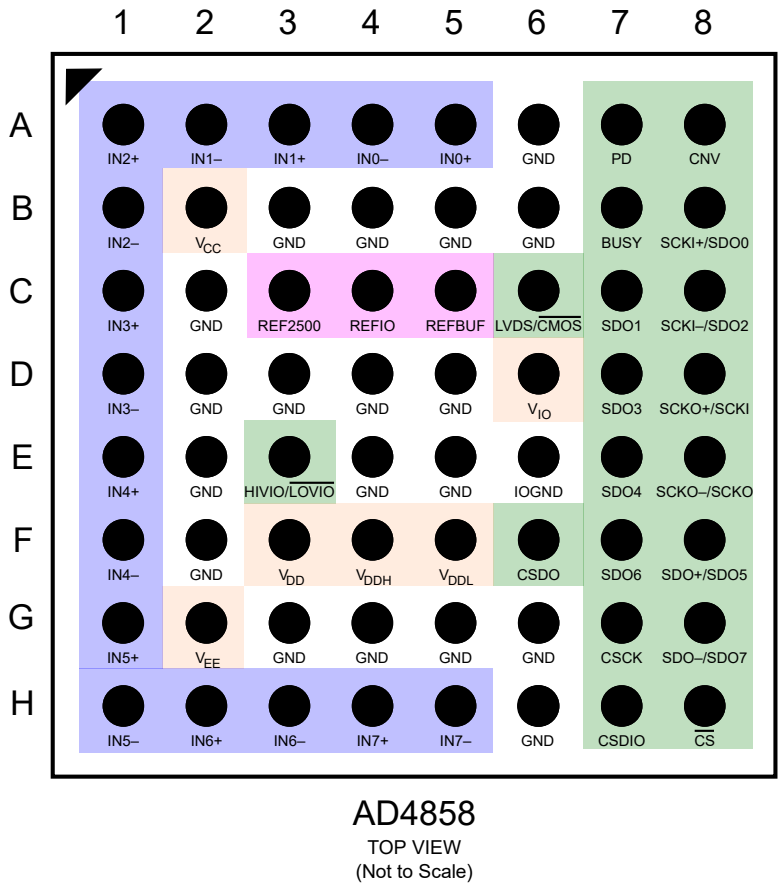


Figure 8. Pin Configuration

Table 9. Universal Pin Function Descriptions

Pin No.	Mnemonic	Type [1]	Description
A5/A4, A3/A2, A1/B1, C1/D1, E1/F1, G1/H1, H2/H3, H4/H5	IN0+/IN0– to IN7+/IN7–	AI	Channels 0 to 7 Positive and Negative Analog Inputs. The converter simultaneously samples and digitizes (V_{INx+} – $V_{INx–}$) for all channels. Wide input common-mode range and high common-mode rejection allow the inputs to accept arbitrary signal swings. Full-scale differential input range is determined by each channel's SoftSpan configuration.
A6, B3, B4, B5, B6, C2, D2, D3, D4, D5, E2, E4, E5, F2, G3, G4, G5, G6, H6	GND	P	Power Supply Ground. Solder all GND pins to a solid ground plane.
A7	PD	DI	Power Down Input. Bring this pin high to power down the device. If PD is brought high while BUSY is high, power down begins once BUSY goes low. Bringing PD high twice without an intervening conversion initiates a global device reset, equivalent to a power-on-reset event. Logic levels are determined by V_{IO}.
A8	CNV	DI	Convert Input. A rising edge on this pin initiates a new conversion. This signal must have low jitter to achieve specified device performance levels. The CNV high and low threshold voltages are 0.7 V and 0.4 V, respectively.
B2	V_{CC}	P	Analog Input Buffers Positive Power Supply. The range of V_{CC} is 7.25 V to 48 V with respect to GND and 10 V to 48 V with respect to V_{EE}. V_{CC} is internally bypassed to GND with a 0.1 µF ceramic capacitor.
B7	BUSY	DO	Busy Output. This pin goes high at the start of each conversion / oversampling window and returns low once the the conversion / oversampling window is complete. This pin also goes high during the start of power-on-reset and goes low once power-on-reset completes. Logic levels are determined by V_{IO}.
C3	REF2500	AO	2.5 V Scaled Reference Output. This pin outputs a precision scaled version of the REFIO pin voltage, nominally V_{REFIO} × (2.500/4.096). If connecting REF2500 externally, see TBD section for recommended use cases and precautions.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Universal Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type [1]	Description
C4	REFIO	AI/AO	Bandgap Reference Output / Reference Buffer Input. An internal bandgap reference nominally outputs 4.096 V on this pin. REFIO is internally bypassed to GND with a 10 nF ceramic capacitor to filter the bandgap output noise. If REFIO is overdriven with an external 4.096 V reference, disable the internal reference through the Device Control Register. If connecting REFIO externally, see the TBD section for recommended uses cases and precautions.
C5	REFBUF	AI/AO	Reference Buffer Output. An internal reference buffer amplifies V_{REFIO} to create the converter master reference voltage V_{REFBUF} = V_{REFIO} on this pin, nominally 4.096 V when using the internal bandgap reference. If REFBUF is overdriven with an external 4.096 V reference, disable the internal reference buffer and bandgap reference through the Device Control Register and bypass REFBUF to GND (pin B4) close to the pin with an external 47 µF ceramic capacitor. If connecting REFBUF externally, see the TBD section for recommended uses cases and precautions.
C6	LVDS/$\overline{\text{CMOS}}$	DI	Conversion Data Bus Mode Select. Tie this pin to V_{IO} to select LVDS Conversion Data bus mode, or to GND to select CMOS Conversion Data bus mode. The state of this pin does not affect the behavior of the SPI Register Configuration bus. Logic levels are determined by V_{IO}.
D6[2]	V_{IO}	P	Digital I/O Power Supply. The range of V_{IO} is 0.9 V to 5.25 V. HIVIO/$\overline{\text{LOVIO}}$ must be tied appropriately based on application V_{IO} level. Tie HIVIO/$\overline{\text{LOVIO}}$ to V_{DD} for applications where 1.71 V ≤ V_{IO} ≤ 5.25 V or to GND for applications where 0.9 V ≤ V_{IO} ≤ 1.89 V. Either tie option may be used when 1.71 V ≤ V_{IO} ≤ 1.89 V. V_{IO} is internally bypassed to IOGND with a 1 µF ceramic capacitor.
E3[2]	HIVIO/$\overline{\text{LOVIO}}$	DI	V_{IO} Voltage Mode Select. Tie this pin to V_{DD} for applications where 1.71 V ≤ V_{IO} ≤ 5.25 V or to GND for applications where 0.9 V ≤ V_{IO} ≤ 1.89 V. Either tie option may be used when 1.71 V ≤ V_{IO} ≤ 1.89 V. Logic levels are determined by V_{DD}.
E6	IOGND	P	Digital I/O Power Supply Ground. Solder IOGND to the same ground plase as GND.
F3	V_{DD}	P	5 V Power Supply. The range of V_{DD} is 4.75 V to 5.25 V. V_{DD} is internally bypassed to GND with a 1 µF ceramic capacitor.
F4	V_{DDH}	P	1.8 V LDO Power Supply. To supply V_{DDL} using the internal 1.8 V LDO, tie V_{DDH} to V_{DD} or to another external power supply between 2.2 V and 5.25 V. To disable the internal LDO, tie V_{DDH} to GND. V_{DDH} is internally bypassed to GND with a 1 µF ceramic capacitor.
F5	V_{DDL}	P	1.8 V Power Supply. To supply V_{DDL} using the internal 1.8 V LDO, tie V_{DDH} to V_{DD} or to another external power supply between 2.2 V and 5.25 V. Do not externally connect V_{DDL} in this case. To externally supply V_{DDL}, disable the internal LDO by tying V_{DDH} to GND and connect V_{DDL} to an external supply in the range of 1.71 V to 1.89 V. V_{DDL} is internally bypassed to GND with a 1 µF ceramic capacitor.
F6	CSDO	DO	SPI Register Configuration Bus Data Output. During 3-wire SPI Register Configuration bus operation this pin remains Hi-Z. During 4-wire bus operation this pin outputs serial data during read transactions. Logic levels are determined by V_{IO}.
G2	V_{EE}	P	Analog Input Buffers Negative Power Supply. The range of V_{EE} is 0 V to –40.75 V with respect to GND and –10 V to –48 V with respect to V_{CC}. V_{EE} is internally bypassed to GND with a 0.1 µF ceramic capacitor.
G7	CSCK	DI	SPI Register Configuration Bus Clock Input. Drive CSCK with the SPI Register Configuration bus clock. CSCK is allowed to idle either high or low. Logic levels are determined by V_{IO}.
H7	CSDIO	DI/DO	SPI Register Configuration Bus Data Input/Output. During both 3- and 4-wire SPI Register Configuration bus operation this pin accepts serial input data. During 3-wire bus operation this pin also outputs serial data during read transactions. Logic levels are determined by V_{IO}.
H8	$\overline{\text{CS}}$	DI	Chip Select Input. The SPI Register Configuration and Conversion Data busses are enabled when $\overline{\text{CS}}$ is low and disabled and Hi-Z when $\overline{\text{CS}}$ is high. Logic levels are determined by V_{IO}.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, DO is digital output, DNC is do not connect

[2] The maximum operating and absolute maximum ratings of V_{IO} and associated digital inputs and outputs are defined by the HIVIO/$\overline{\text{LOVIO}}$ pin state.

Table 10. CMOS Conversion Data Bus Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
B8, C7, C8, D7, E7, F8, F7, G8	SDO0 to SDO7	DO	Channels 0 to 7 CMOS Conversion Data Outputs. Conversion results and optional channel status information are output on these pins synchronized to SCKI. SDO0 may also be configured through Entry/Exit ADC Read Mode Control Register Address to output SPI Register Configuration bus serial data during 4-wire read operations. Logic levels are determined by V_{IO}.
D8	SCKI	DI	CMOS Conversion Data Clock Input. Drive SCKI with the CMOS Conversion Data bus clock. SCKI is allowed to idle either high or low. Logic levels are determined by V_{IO}.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. CMOS Conversion Data Bus Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
E8	SCKO	DO	CMOS Conversion Data Clock Output. SCKO outputs a copy of SCKI skew-matched to the serial output data on SDO0 to SDO7. If clock echoing is disabled through the Device Control Register, this pin is Hi-Z. Logic levels are determined by V_{IO}.

Table 11. LVDS Conversion Data Bus Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
B8/C8	SCKI+/SCKI–	DI	LVDS Conversion Data Clock Input. Differentially drive SCKI+/SCKI– with the LVDS Conversion Data bus clock. Idle SCKI+/SCKI– low, including when transitioning $\overline{CS}$. By default SCKI+/SCKI– is internally terminated with a 100 Ω differential resistor when $\overline{CS}$ is low. This termination may be disabled through the Device Control Register.
C7, D7, E7, F7	SDO1, SDO3, SDO4, SD06	DO	CMOS Conversion Data Outputs. In LVDS Conversion Data bus mode these pins are Hi-Z.
D8/E8	SCKO+/SCKO–	DO	LVDS Conversion Data Clock Output. SCKO+/SCKO– outputs a copy of SCKI+/SCKI–, skew-matched with the serial output data on SDO+/SDO–. The SCKO+/SCKO– output pair must be differentially terminated with a 100 Ω resistor at the receiver (FPGA). If clock echoing is disabled through the Device Control Register, these pins are Hi-Z.
F8/G8	SDO+/SDO–	DO	LVDS Conversion Data Output. Conversion results and optional channel status information are output on these pins synchronized to SCKI+/SCKI–. The SDO+/SDO–output pair must be differentially terminated with a 100 Ω resistor at the receiver (FPGA).

TYPICAL PERFORMANCE CHARACTERISTICS

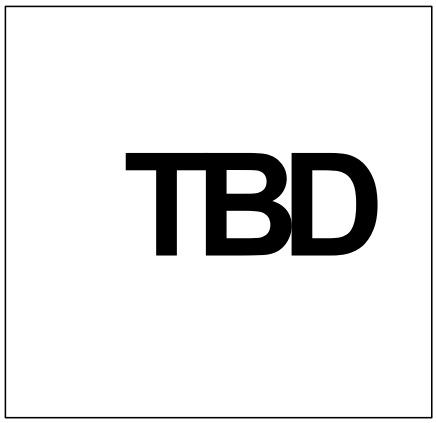


Figure 9. Fast Fourier Transform (FFT) , ±10V range, 1MSPS, fully differential

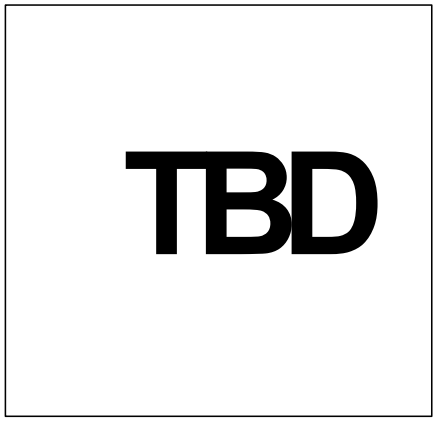


Figure 10. FFT, ±10V range, 1MSPS, fully differential, sHDR ON

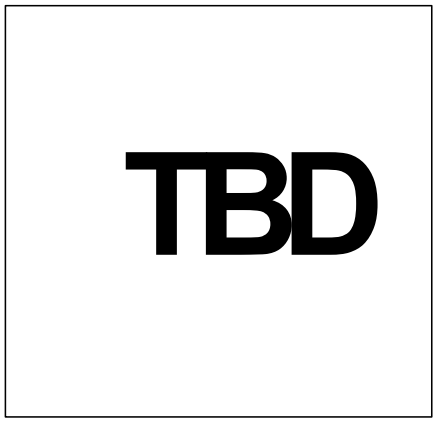


Figure 11. FFT,0 to 10V range, 1MSPS,single-ended

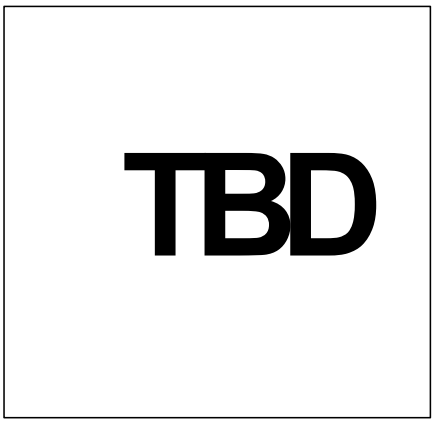


Figure 12. FFT, ±10V range, 1MSPS, single-ended

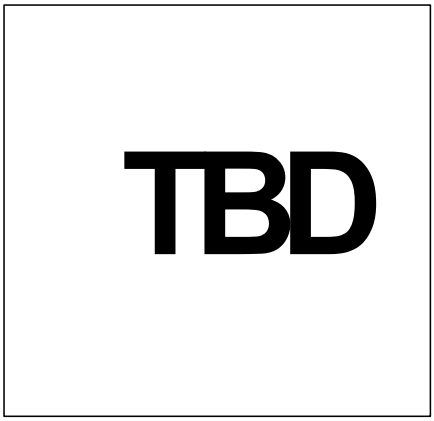


Figure 13. FFT, ±10V range, 1MSPS, single-ended, sHDR ON

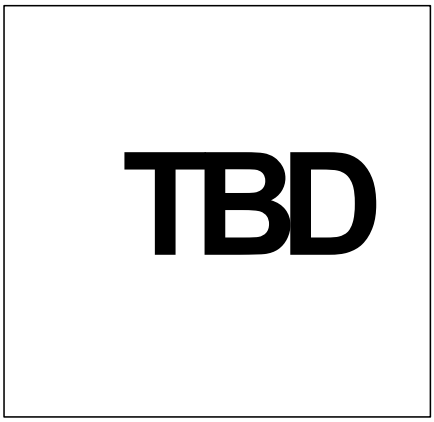


Figure 14. FFT, 0 to 10V range, 1MSPS, single-ended, sHDR ON

TYPICAL PERFORMANCE CHARACTERISTICS

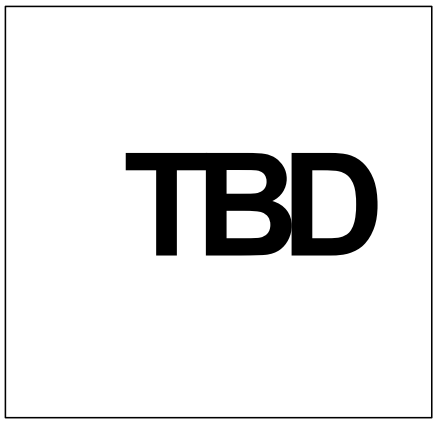


Figure 15. SNR vs V_{REFBUF}, ±10V range

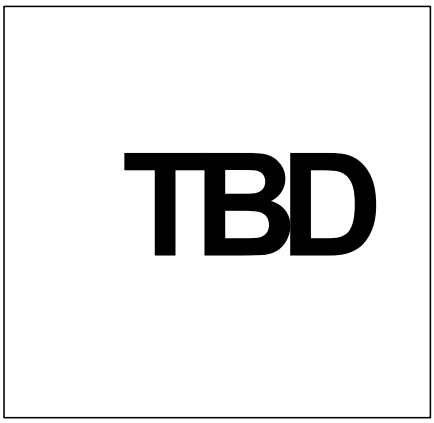


Figure 18. SNR vs Input Level, sHDR ON

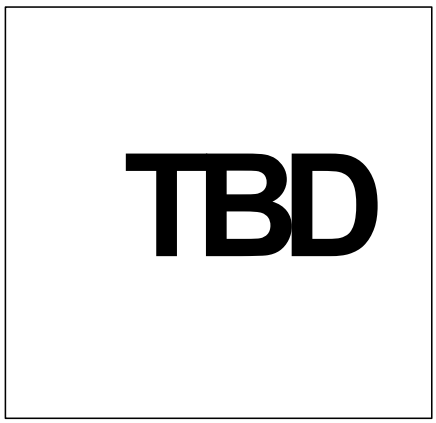


Figure 16. SNR vs Input frequency for different OSR, ±10V range

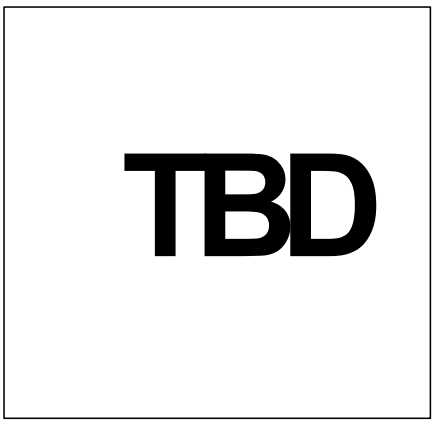


Figure 19. SNR vs freq for different OSR, ±20V range

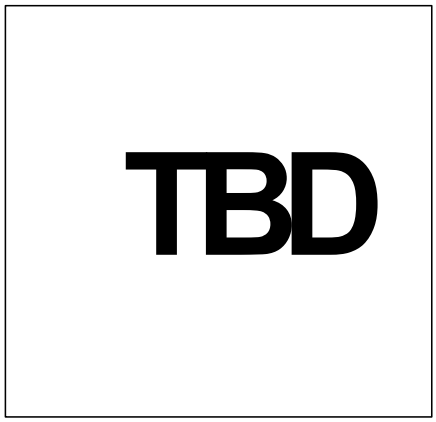


Figure 17. SNR vs freq for different OSR, 0 to 10V range

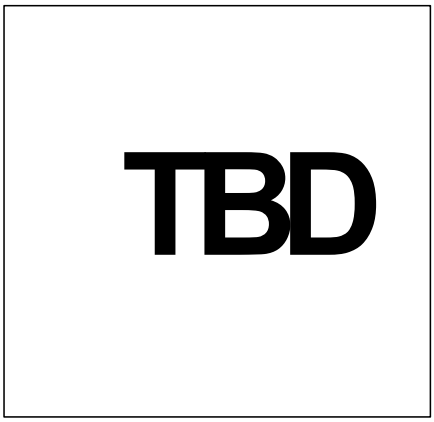


Figure 20. SNR, SINAD vs Input Level

TYPICAL PERFORMANCE CHARACTERISTICS

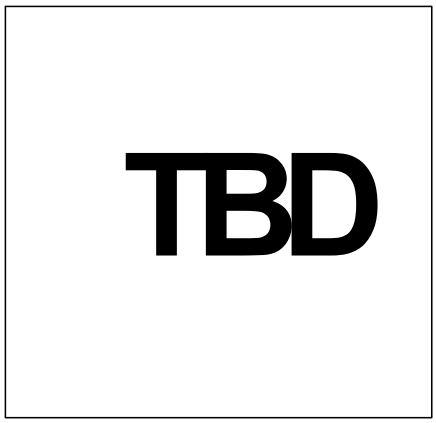


Figure 21. SNR vs Temperature for different softspans

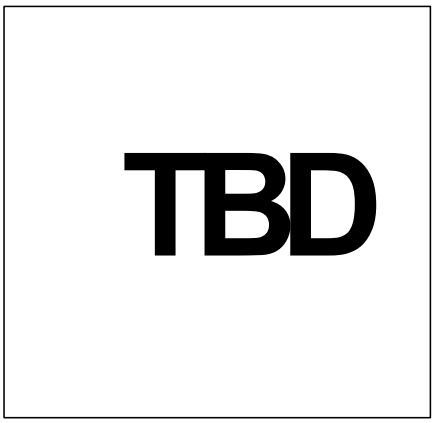


Figure 24. RMS noise vs DC input voltage, sHDR ON

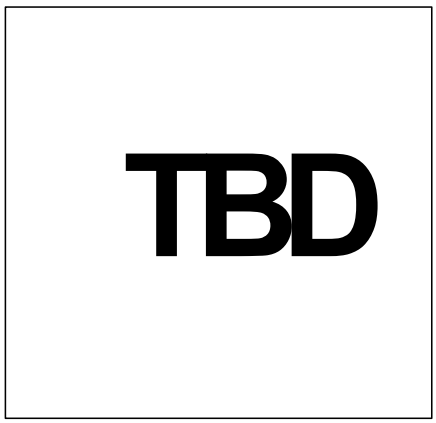


Figure 22. THD vs Input frequency for different R_{source}

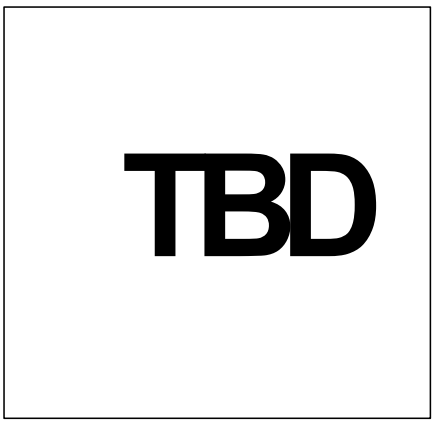


Figure 25. THD vs Input common mode

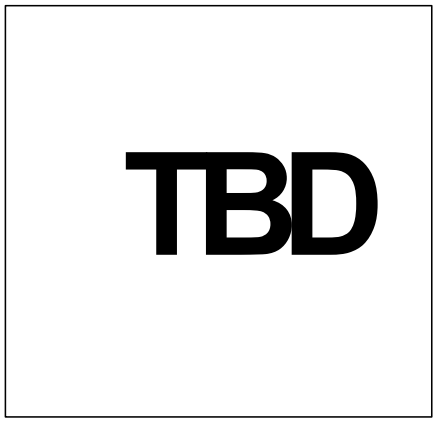


Figure 23. THD vs Input Level for different input tones (1, 10, 50, 100 kHz)

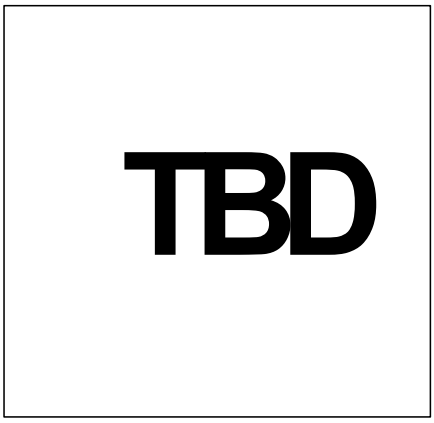


Figure 26. THD vs V_{REFBUF}

TYPICAL PERFORMANCE CHARACTERISTICS

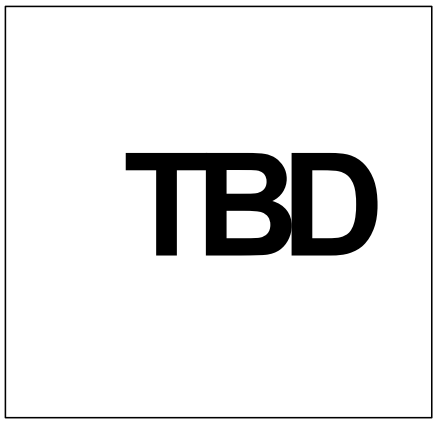


Figure 27. INL, DNL, vs Temperature

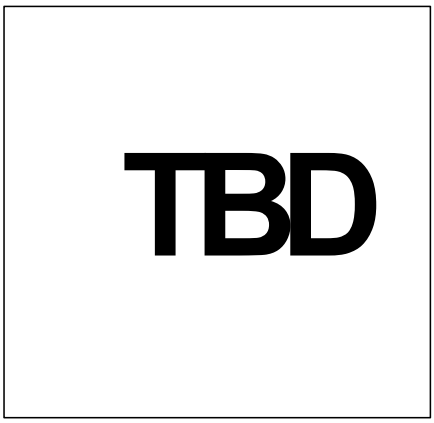


Figure 30. THD vs Temperature, for various softspan ranges

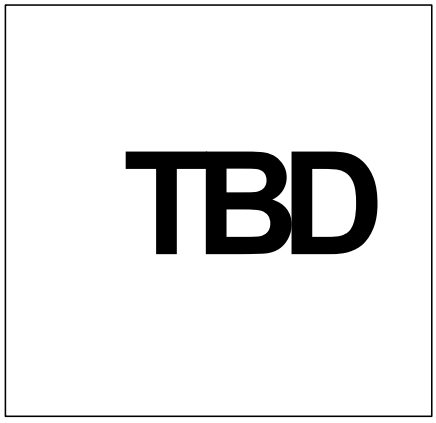


Figure 28. Typical DNL vs code, for various softspan ranges

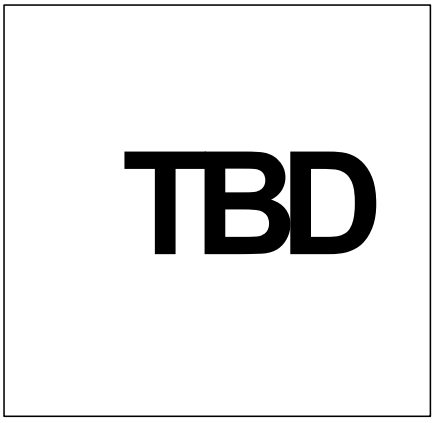


Figure 31. Typical INL vs code, for various softspan ranges

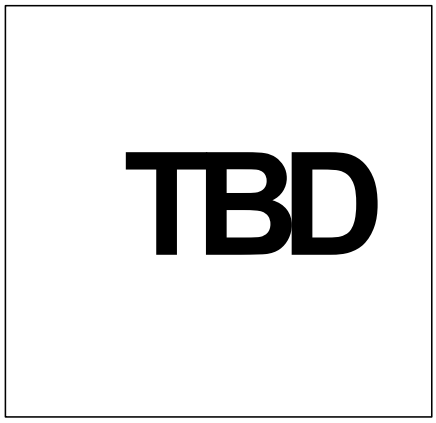


Figure 29. Analog Input Leakage current vs Temperature

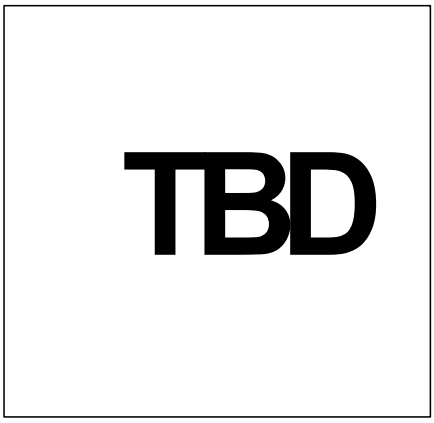


Figure 32. Analog Input current vs Input Voltage, for various softspan ranges

TYPICAL PERFORMANCE CHARACTERISTICS

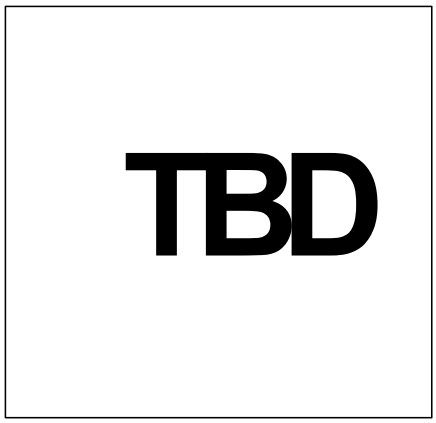


Figure 33. Histogram of codes, for various softspan ranges

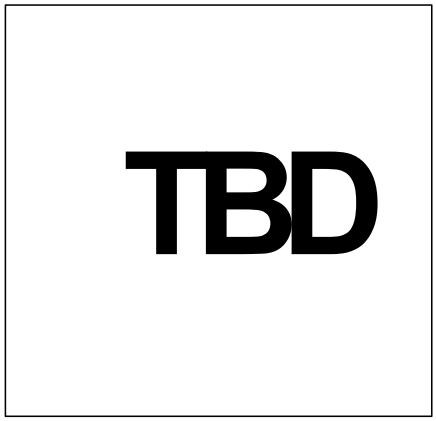


Figure 34. PFS/NFS error vs temperature, all channels

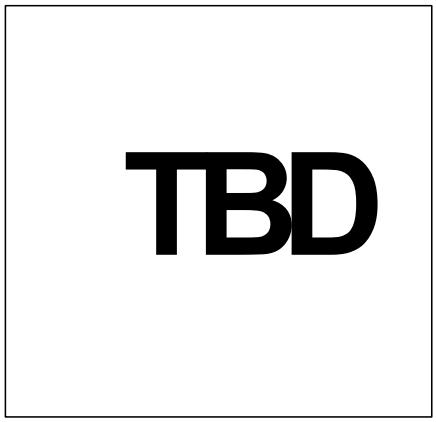


Figure 35. PFS/NFS drift histogram

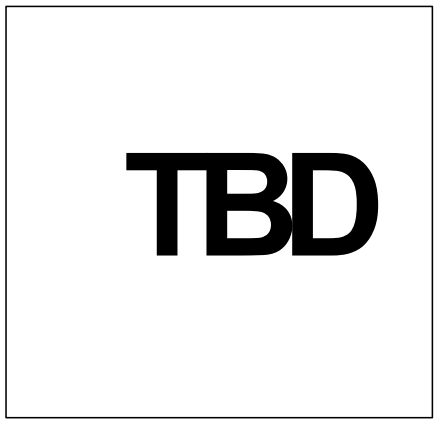


Figure 36. Zero-Scale error vs Temperature, all channels

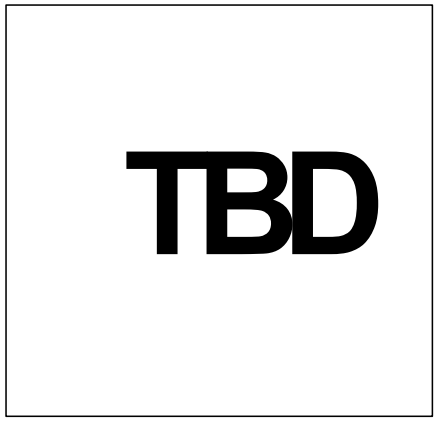


Figure 37. Zero-Scale drift Histogram

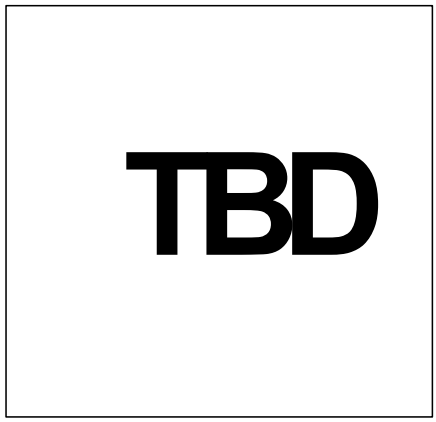


Figure 38. Offset error vs Input Common mode

TYPICAL PERFORMANCE CHARACTERISTICS

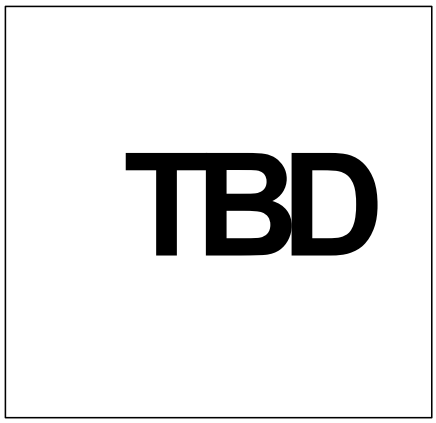


Figure 39. Supply Current vs Temperature, all supply pins

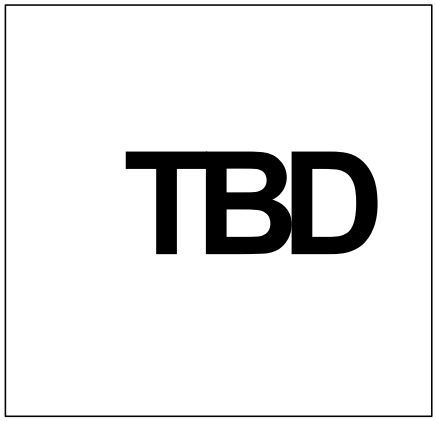


Figure 40. Power Dissipation vs Sampling Rate, N-channels enabled

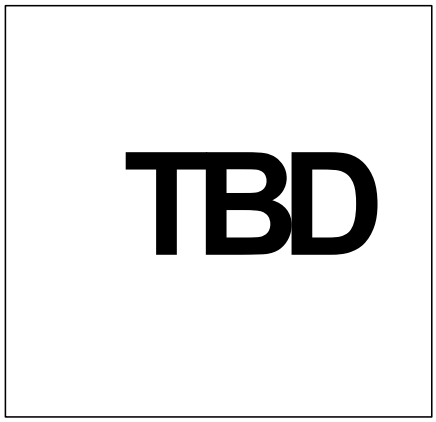


Figure 41. PSRR vs frequency, all supply pins

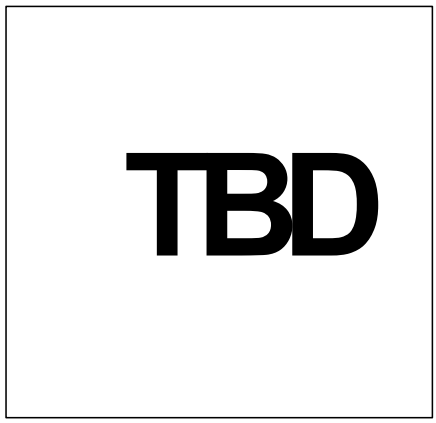


Figure 42. Supply current vs Sampling Rate

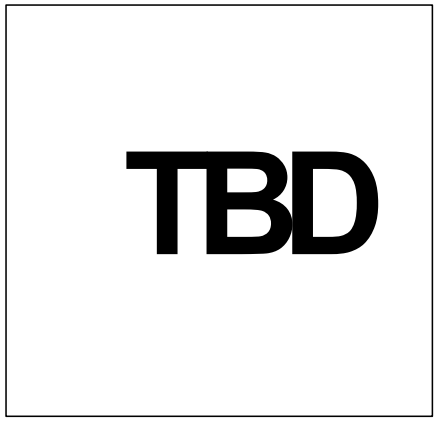


Figure 43. PowerDown current vs Temperature, all supply pins

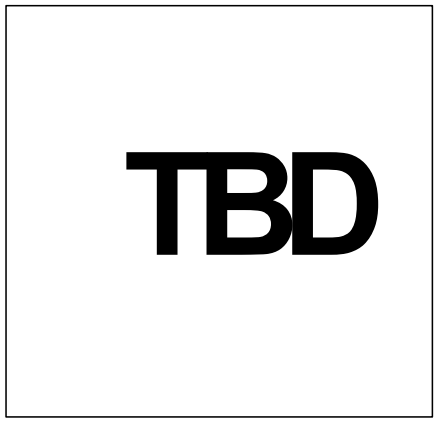


Figure 44. Internal Reference Output vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

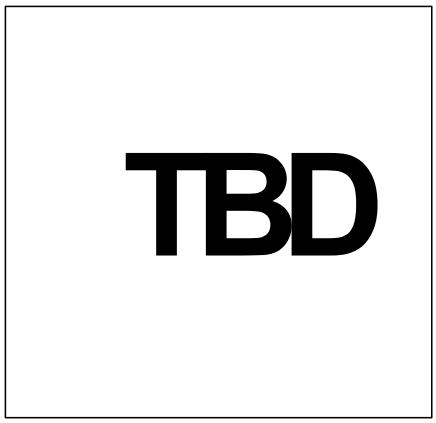


Figure 45. Step Response (Large-signal settling)

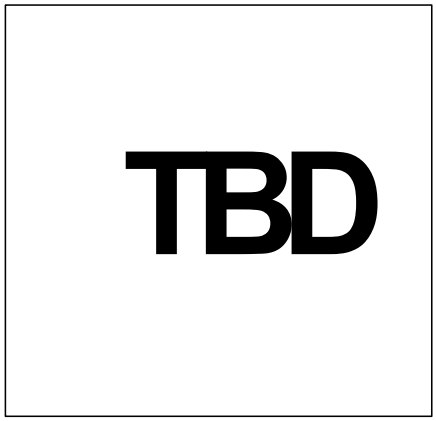


Figure 46. Step Respone (fine settling)

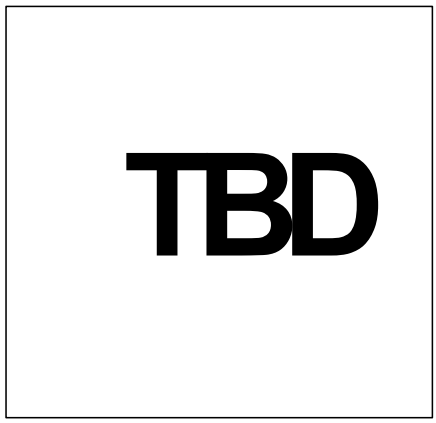


Figure 47. CMRR vs input frequency, all channels

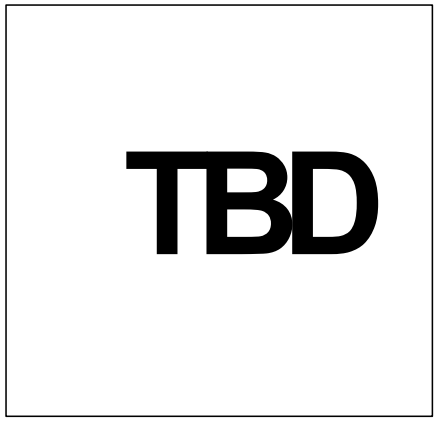


Figure 48. Crosstalk vs input frequency

TERMINOLOGY

Integral Nonlinearity (INL) Error

INL is the deviation of each individual code from a line drawn through the two endpoints of the ADC transfer function. The two endpoints of the transfer function are ½ LSB before the first code transition and 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 31).

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Zero-Scale Error

For bipolar SoftSpan ranges, zero-scale error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 0000 0000 and 1111 1111 1111 1111 1111.

For unipolar SoftSpan ranges, zero-scale error is the offset voltage measured from 0.5 LSB when the output code flickers between 0000 0000 0000 0000 0000 and 0000 00000000 0000 0001.

Full-Scale Error

For bipolar SoftSpan ranges, full-scale error is the worst-case deviation of the first and last code transitions from ideal. It includes the effect of zero-scale error and any contributions from the reference buffer.

For unipolar SoftSpan ranges, full-scale error is the worst-case deviation of the last code transition from ideal. It includes the effect of zero-scale error and any contributions from the reference buffer.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$ENOB = (SINAD_{dB} - 1.76)/6.02$

ENOB is expressed in bits.

Dynamic Range (DR)

Dynamic range is the ratio of the rms amplitude of a full-scale sine wave to the total rms noise, and is expressed in decibels (dB). It is measured with a −60 dBFS input signal to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms amplitude of a full-scale sine wave to the rms sum of all other spectral components below the Nyquist frequency, excluding the first five harmonics and dc. The value for SNR is expressed in decibels (dB).

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms amplitude of a full-scale sine wave to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels (dB).

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms amplitude of the fundamental input signal and is expressed in decibels (dB).

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of a full-scale input signal and the peak spurious signal.

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is measured by applying a −1 dBFS sine wave at frequency (f_{inj}) on seven crosstalk injector channels and a second −1 dBFS sine wave at a different frequency (f_{rcv}) on a single crosstalk receiver channel. Crosstalk is the ratio of the rms sum of the spectral tones at f_{inj} and its first two harmonics on the receiver and injector channels, and is expressed in decibels (dB). All channels are converting at f_S = 1 MSPS with the internal reference and reference buffer enabled during the measurement.

Aperture Delay

Aperture delay is a measure of acquisition performance. It is the time between the rising edge of the CNV input and when the input signals are held for a conversion.

Transient Response

Transient response is the time required for the ADC to acquire a full-scale input step to 0.005% settling accuracy.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the rms amplitude of a sine wave of frequency f applied to the analog input common-mode voltage to the rms amplitude of the ADC output data at frequency f. The value for CMRR is expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the rms amplitude of a sine wave of frequency f applied to the power supply voltage to the rms amplitude of the ADC output data at frequency f. The value for PSRR is expressed in decibels (dB).

THEORY OF OPERATION

OVERVIEW

The AD4858 is a 20-bit, low noise 8-channel simultaneous sampling successive approximation register (SAR) ADC with buffered differential, wide common mode range picoamp inputs. The ADC operates from a 5 V low voltage supply and flexible high voltage supplies, nominally ±24 V. Using the integrated low-drift reference and buffer (V_{REFBUF} = 4.096 V nominal), each channel of this SoftSpan ADC can be independently configured to accept bipolar signals (±40 / 25 / 20 / 12.5 / 10 / 6.25 / 5 / 2.5 V) or unipolar signals (0 V to 40 / 25 / 20 / 12.5 / 10 / 6.25 / 5 / 2.5 V). Individual channels may also be disabled to reduce power consumption.

The integrated picoamp input analog buffers, wide input common mode range, and 125dB CMRR of the AD4858 allow the ADC to directly digitize a variety of signals using minimal board space and power. This input signal flexibility, combined with ±12 ppm INL, no missing codes at 20 bits, 97 dB SNR and 110 dB dynamic range makes the AD4858 an ideal choice for many high voltage applications requiring wide dynamic range. The absolute common mode input range (V_{EE} + 3.2 V to V_{CC} – 3.2 V) is determined by the choice of high voltage supplies. These supplies may be biased asymmetrically around ground and include the ability for V_{EE} to be tied directly to ground.

The AD4858 supports pin-selectable SPI CMOS (0.9 V to 5.25 V) and LVDS serial interfaces enabling it to communicate equally well with legacy microcontrollers and modern FPGAs. In CMOS mode, applications may employ between one and eight lanes of serial output data, allowing the user to optimize bus width and data throughput. In LVDS mode, pins SDO^+/SDO^-, $SCKI^+/SCKI^-$ and $SCKO^+/SCKO^-$ function as differential serial data output, clock input and clock output pins respectively.

The AD4858 typically dissipates 45 mW per channel, when converting eight channels simultaneously at 1 MSPS. Optional nap and power down modes may be employed to further reduce power consumption during inactive periods.

Per-channel offset, gain and phase calibration registers can be used for optional system performance improvement.

APPLICATIONS INFORMATION

NAP MODE

The AD4858 can be placed into nap mode after a conversion has been completed to reduce power consumption between conversions. In this mode, a portion of the device circuitry is turned off, including circuits associated with sampling the analog input signals. Nap mode is enabled by keeping CNV high between conversions, as shown in Figure 49. To initiate a new conversion after entering nap mode, bring CNV low and hold for at least 700ns before bringing it high again. The converter acquisition time (t_{ACQ}) is set by the CNV low time (t_{CNVL}) when using nap mode.

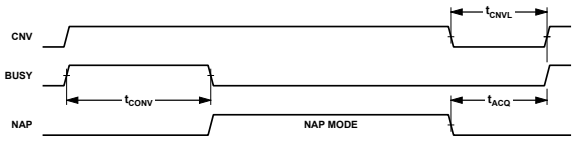


Figure 49. Nap Mode Timing for the AD4858

POWER DOWN MODE

When the PD line is brought high or the POWER_MODE field in the Device Configuration Register is set to 2b'11, the AD4858 is powered down and subsequent conversion requests are ignored. If this occurs during a conversion, the device powers down once the conversion completes. In this mode, the device draws only a small regulator standby current resulting in a typical power dissipation of 1.3 mW. To exit power down mode, bring the PD pin low and wait at least 1 ms before initiating a conversion. Any conversion initiated before these times will produce invalid results.

RESET TIMING

A global reset of the AD4858, equivalent to a power-on-reset event, may be executed without needing to cycle the supplies. This feature is useful when recovering from system-level events that require the state of the entire system to be reset to a known synchronized value. To initiate a global reset, bring PD high twice without an intervening conversion as shown in Figure 50 . Alternatively, an equivalent global reset may be triggered by entering, exiting, and then re-entering power down mode using the POWER_MODE field in the Device Configuration Register without an intervening conversion.

The reset event is triggered on the second rising edge of PD, and asynchronously ends based on an internal timer. Reset clears all serial data output registers and restores the internal SoftSpan configuration register to the default SoftSpan15 for all channels. If reset is triggered during conversion, the conversion is immediately halted. The normal power down behavior associated with PD going high is not affected by reset. Once PD is brought low, wait at least 1ms before initiating a conversion. Any conversion initiated before the time will produce invalid results.

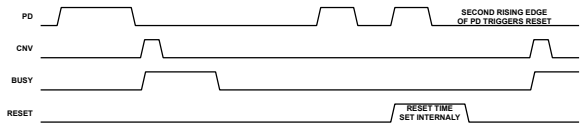


Figure 50. Reset Timing for AD4858

REGISTER INFORMATION

The AD4858 register map contains the fields required to monitor and configure the device. All read and write communication is performed using the AD4858 SPI CMOS Register Configuration Bus.

The AD4858 register map is organized into three regions: SPI_CORE_CONFIG (address 0x000 to 0x01F), AD4858 USER_MAP registers (address 0x020 to 0x29) and Channel configuration registers (address 0x2A to 0xB9). Table 12 through Table 21 show the complete register map address assignments for the AD4858.

Though some configuration information spans multiple bytes, the register space is addressed byte-wise for both read and write operations. For example, the device ID spans two registers for [DEVICE_ID_H, DEVICE_ID_L] with its least significant byte address at 0x04 and its most significant byte at address 0x05.

Fields in the AD4858 configuration registers are defined as read-only, read/write or write-1-to-clear. Read-only bits cannot be reconfigured by SPI writes. Read/write bits can be read from or written to. Write-1-to-clear (W1C) bits can be read from and are reset to 0 when the digital host writes a 1 to their associated memory location.

Note per-channel configuration register address and descriptions are shown for channel 0. Per-channel configuration registers for channels[1:7] may be accessed starting at address 0x3C. There are 0x12 (or decimal 18) registers per channel, so the address spacing between the same named register for adjacent channels is 0x12. For example, addressing register 0x2A will read or write from the channel 0 SoftSpan register while addressing from 0x2A + 0x12= 0x3C will write to the SoftSpan register for channel 1.

The reset value for register CH[N]_TESTPAT_H for all channels is determined as follows: 0x{N,A} where N is the channel number and 0x0A is a fixed hexadecimal value. For example, the reset register for channel[0]s is 0x0A, where the reset value for channel 5 is 0x5A.

REGISTER BUS CRC

The AD4858 register bus data includes optional error checking based on an 8-bit CRC. When the CRC is enabled, an 8-bit checksum code is appended to the data phase of each register's read or write transaction. The value of the checksum is calculated from the data read or written, allowing the AD4858 and the digital host to detect if data corruption has occurred. If the checksum does not match the corresponding register data, the register read or write is considered invalid.

The following CRC polynomial is used to calculate the checksums:
$x^8 + x^2 + x + 1$
The initial value for the CRC calculation is 0xA5 in all transactions.

REGISTER SUMMARY

Table 12. SPI_CORE_CONFIG(DEVICE BASE) Register Summary

Address	Name	Description	Reset	Access
0x00	INTERFACE_CONFIG_A	Interface Configuration A.	0x00	R/W
0x01	INTERFACE_CONFIG_B	Interface Configuration B.	0x00	R/W
0x02	DEVICE_CONFIG	Device Configuration.	0xF0	R/W
0x03	CHIP_TYPE	Chip Type.	0x07	R
0x04	PRODUCT_ID_L	Product ID Low.	0x60	R
0x05	PRODUCT_ID_H	Product ID High.	0x00	R
0x06	CHIP_GRADE	Chip Grade.	0x00	R
0x0A	SCRATCH_PAD	Scratch Pad.	0x00	R/W
0x0B	SPI_REVISION	SPI Revision.	0x83	R
0x0C	VENDOR_L	Vendor ID Low.	0x56	R
0x0D	VENDOR_H	Vendor ID High.	0x04	R
0x0E	STREAM_MODE	Stream Mode.	0x00	R/W
0x0F	TRANSFER_CONFIG	Transfer Config.	0x00	R/W
0x10	INTERFACE_CONFIG_C	Interface Configuration C.	0x03	R/W
0x11	INTERFACE_STATUS_A	Interface Status A.	0x00	R/W

Table 13. USER_MAP(USER_MAP) Register Summary

Address	Name	Description	Reset	Access
0x14	SPI_CONFIG_D	Entry/Exit ADC Read mode control register address.	0x00	R/W
0x20	DEVICE_STATUS	Device Status.	0x40	R/W
0x21	CH_OR_STATUS	OR Status.	0x00	R/W
0x22	CH_UR_STATUS	UR Status.	0x00	R/W
0x23	REGMAP_CRC	Register map CRC.	0x0000	R/W
0x25	DEVICE_CTRL	Device Control.	0x11	R/W
0x26	PACKET	Packet format.	0x01	R/W
0x27	OVERSAMPLE	Oversample control.	0x00	R/W
0x28	SEAMLESS_HDR	SEAMLESS_HDR.	0xFF	R/W
0x29	CH_SLEEP	Channel sleep.	0x00	R/W

Table 14. CH0_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x2A	CH0_SOFTSPAN	Softspan.	0x0F	R/W
0x2B	CH0_OFFSET	Offset.	0x000000	R/W
0x2E	CH0_GAIN	Gain.	0x8000	R/W
0x30	CH0_PHASE	Phase.	0x0000	R/W
0x32	CH0_OR	Overrange limit.	0x7FFFF0	R/W
0x35	CH0_UR	Underrange limit.	0x800000	R/W
0x38	CH0_TESTPAT	Test Pattern.	0x0ACE3C2A	R/W

Table 15. CH1_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x3C	CH1_SOFTSPAN	Softspan.	0x0F	R/W
0x3D	CH1_OFFSET	Offset.	0x000000	R/W
0x40	CH1_GAIN	Gain.	0x8000	R/W
0x42	CH1_PHASE	Phase.	0x0000	R/W
0x44	CH1_OR	Overrange limit.	0x7FFFF0	R/W
0x47	CH1_UR	Underrange limit.	0x800000	R/W

REGISTER SUMMARY

Table 15. CH1_CONFIG(CH_CONFIG) Register Summary (Continued)

Address	Name	Description	Reset	Access
0x4A	CH1_TESTPAT	Test Pattern.	0x1ACE3C2A	R/W

Table 16. CH2_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x4E	CH2_SOFTSPAN	Softspan.	0x0F	R/W
0x4F	CH2_OFFSET	Offset.	0x000000	R/W
0x52	CH2_GAIN	Gain.	0x8000	R/W
0x54	CH2_PHASE	Phase.	0x0000	R/W
0x56	CH2_OR	Overrange limit.	0x7FFFF0	R/W
0x59	CH2_UR	Underrange limit.	0x800000	R/W
0x5C	CH2_TESTPAT	Test Pattern.	0x2ACE3C2A	R/W

Table 17. CH3_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x60	CH3_SOFTSPAN	Softspan.	0x0F	R/W
0x61	CH3_OFFSET	Offset.	0x000000	R/W
0x64	CH3_GAIN	Gain.	0x8000	R/W
0x66	CH3_PHASE	Phase.	0x0000	R/W
0x68	CH3_OR	Overrange limit.	0x7FFFF0	R/W
0x6B	CH3_UR	Underrange limit.	0x800000	R/W
0x6E	CH3_TESTPAT	Test Pattern.	0x3ACE3C2A	R/W

Table 18. CH4_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x72	CH4_SOFTSPAN	Softspan.	0x0F	R/W
0x73	CH4_OFFSET	Offset.	0x000000	R/W
0x76	CH4_GAIN	Gain.	0x8000	R/W
0x78	CH4_PHASE	Phase.	0x0000	R/W
0x7A	CH4_OR	Overrange limit.	0x7FFFF0	R/W
0x7D	CH4_UR	Underrange limit.	0x800000	R/W
0x80	CH4_TESTPAT	Test Pattern.	0x4ACE3C2A	R/W

Table 19. CH5_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x84	CH5_SOFTSPAN	Softspan.	0x0F	R/W
0x85	CH5_OFFSET	Offset.	0x000000	R/W
0x88	CH5_GAIN	Gain.	0x8000	R/W
0x8A	CH5_PHASE	Phase.	0x0000	R/W
0x8C	CH5_OR	Overrange limit.	0x7FFFF0	R/W
0x8F	CH5_UR	Underrange limit.	0x800000	R/W
0x92	CH5_TESTPAT	Test Pattern.	0x5ACE3C2A	R/W

Table 20. CH6_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0x96	CH6_SOFTSPAN	Softspan.	0x0F	R/W
0x97	CH6_OFFSET	Offset.	0x000000	R/W
0x9A	CH6_GAIN	Gain.	0x8000	R/W

REGISTER SUMMARY

Table 20. CH6_CONFIG(CH_CONFIG) Register Summary (Continued)

Address	Name	Description	Reset	Access
0x9C	CH6_PHASE	Phase.	0x0000	R/W
0x9E	CH6_OR	Overrange limit.	0x7FFFF0	R/W
0xA1	CH6_UR	Underrange limit.	0x800000	R/W
0xA4	CH6_TESTPAT	Test Pattern.	0x6ACE3C2A	R/W

Table 21. CH7_CONFIG(CH_CONFIG) Register Summary

Address	Name	Description	Reset	Access
0xA8	CH7_SOFTSPAN	Softspan.	0x0F	R/W
0xA9	CH7_OFFSET	Offset.	0x000000	R/W
0xAC	CH7_GAIN	Gain.	0x8000	R/W
0xAE	CH7_PHASE	Phase.	0x0000	R/W
0xB0	CH7_OR	Overrange limit.	0x7FFFF0	R/W
0xB3	CH7_UR	Underrange limit.	0x800000	R/W
0xB6	CH7_TESTPAT	Test Pattern.	0x7ACE3C2A	R/W

REGISTER SUMMARY: BASE DEVICE & INTERFACE AND CONFIGURATION (DEVICE BASE)

Table 22. DEVICE BASE Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			RESET_SW	0x00	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED							0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	STATUS_BIT_3	STATUS_BIT_2	STATUS_BIT_1	STATUS_BIT_0	RESERVED		OPERATING_MODES		0xF0	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x60	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x83	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x0F	TRANSFER_CONFIG	[7:0]	RESERVED					KEEP_STREAM_LENGTH_VAL	RESERVED		0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		RESERVED		ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x03	R/W
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	RESERVED	ADDRESS_INVALID_ERR	0x00	R/W

REGISTER SUMMARY: USER_MAP

Table 23. USER_MAP Register Summary

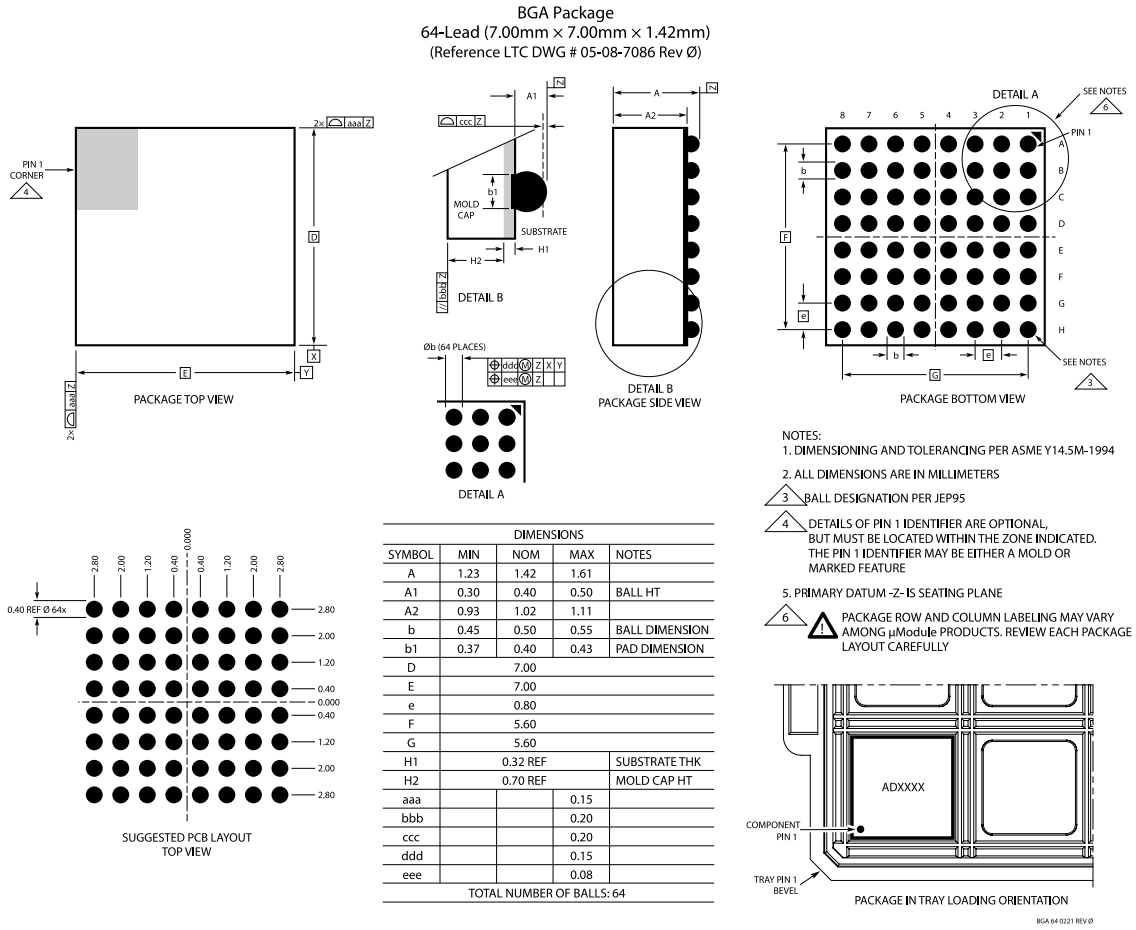
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x14	SPI_CONFIG_D	[7:0]	RESERVED							CSDO_ON_SDO0	0x00	R/W
0x20	DEVICE_STATUS	[7:0]	DEVICE_READY	RESET_FLAG	FUSE_CRC_FLAG	REGMAP_CRC_FLAG	SPI_FLAG	CH_ORUR_FLAG	PD_FLAG	SLEEP_FLAG	0x40	R/W
0x21	CH_OR_STATUS	[7:0]	CH7_OR_FLAG	CH6_OR_FLAG	CH5_OR_FLAG	CH4_OR_FLAG	CH3_OR_FLAG	CH2_OR_FLAG	CH1_OR_FLAG	CH0_OR_FLAG	0x00	R/W
0x22	CH_UR_STATUS	[7:0]	CH7_UR_FLAG	CH6_UR_FLAG	CH5_UR_FLAG	CH4_UR_FLAG	CH3_UR_FLAG	CH2_UR_FLAG	CH1_UR_FLAG	CH0_UR_FLAG	0x00	R/W
0x23	REGMAP_CRC	[15:8]	REGMAP_CRC[15:8]								0x0000	R/W
		[7:0]	REGMAP_CRC[7:0]									
0x25	DEVICE_CTRL	[7:0]	TEST_CRCS	RESERVED		LVDS_TERM	LVDS_HALF_BIAS	RB_SLEEP	BG_SLEEP	SCKO_ECHO	0x11	R/W
0x26	PACKET	[7:0]	RESERVED					TEST_PAT	PACKET_FORMAT		0x01	R/W
0x27	OVERSAMPLE	[7:0]	OS_EN	RESERVED			OS_RATIO				0x00	R/W
0x28	SEAMLESS_HDR	[7:0]	CH7_SHDR_EN	CH6_SHDR_EN	CH5_SHDR_EN	CH4_SHDR_EN	CH3_SHDR_EN	CH2_SHDR_EN	CH1_SHDR_EN	CH0_SHDR_EN	0xFF	R/W
0x29	CH_SLEEP	[7:0]	CH7_SLEEP	CH6_SLEEP	CH5_SLEEP	CH4_SLEEP	CH3_SLEEP	CH2_SLEEP	CH1_SLEEP	CH0_SLEEP	0x00	R/W

REGISTER SUMMARY: (CH_CONFIG)

Table 24. CH_CONFIG Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0	CH0_SOFTSPAN	[7:0]	RESERVED				CH0_SOFTSPAN				0x0F	R/W
0x1	CH0_OFFSET	[23:16]	CH0_OFFSET[19:12]								0x000000	R/W
		[15:8]	CH0_OFFSET[11:4]									
		[7:0]	CH0_OFFSET[3:0]				RESERVED					
0x4	CH0_GAIN	[15:8]	CH0_GAIN[15:8]								0x8000	R/W
		[7:0]	CH0_GAIN[7:0]									
0x6	CH0_PHASE	[15:8]	CH0_PHASE[15:8]								0x0000	R/W
		[7:0]	CH0_PHASE[7:0]									
0x8	CH0_OR	[23:16]	CH0_OR[19:12]								0x7FFFF0	R/W
		[15:8]	CH0_OR[11:4]									
		[7:0]	CH0_OR[3:0]				RESERVED					
0xB	CH0_UR	[23:16]	CH0_UR[19:12]								0x800000	R/W
		[15:8]	CH0_UR[11:4]									
		[7:0]	CH0_UR[3:0]				RESERVED					
0xE	CH0_TESTPAT	[31:24]	CH0_TESTPAT[31:24]								0x0ACE3C2A	R/W
		[23:16]	CH0_TESTPAT[23:16]									
		[15:8]	CH0_TESTPAT[15:8]									
		[7:0]	CH0_TESTPAT[7:0]									

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.23	1.42	1.61	
A1	0.30	0.40	0.50	BALL HT
A2	0.93	1.02	1.11	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.00		
E		7.00		
e		0.80		
F		5.60		
G		5.60		
H1		0.32 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 64				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

Figure 51. 64 ball BGA, dimensions shown in millimeters