ADMFM2000

0.5 GHz to 32 GHz Microwave Downconverter

FEATURES

- Dual-channel, 0.5 GHz to 32 GHz receiver
- Integrated LNA
- Integrated downconversion mixer
- Integrated switch for mixer bypass
- Integrated IF LPF: 8 GHz bandwidth
- Integrated DSA
- Attenuation range: 31 dB with 1 dB step
- Single common LO input
- 50 Ω matched input and output
- 20.00 mm × 14.00 mm, 179-ball CSP_BGA

APPLICATIONS

- Electronic warfare
- Satellite communication
- Phased-array radar receiver

GENERAL DESCRIPTION

The ADMFM2000 is a dual-microwave downconverter, system-in-package (SiP) module, with input RF and local oscillator (LO) frequency ranges covering 5 GHz to 32 GHz, with an output intermediate frequency (IF) frequency range from 0.5 GHz to 8 GHz. A common LO input signal is split to feed two separate buffer amplifiers to drive the mixer in each channel. Each down conversion path consists of an LNA, a mixer, an IF filter, a digital step attenuator (DSA), and an IF amplifier.

Fabricated using a combination of surface mount and bare die components, the ADMFM2000 provides precise gain adjustment capabilities with low distortion performance. The ADMFM2000 comes in a compact, shielded 20.00 mm × 14.00 mm, 179-ball chip scale package ball grid array [CSP_BGA] and operates over a temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

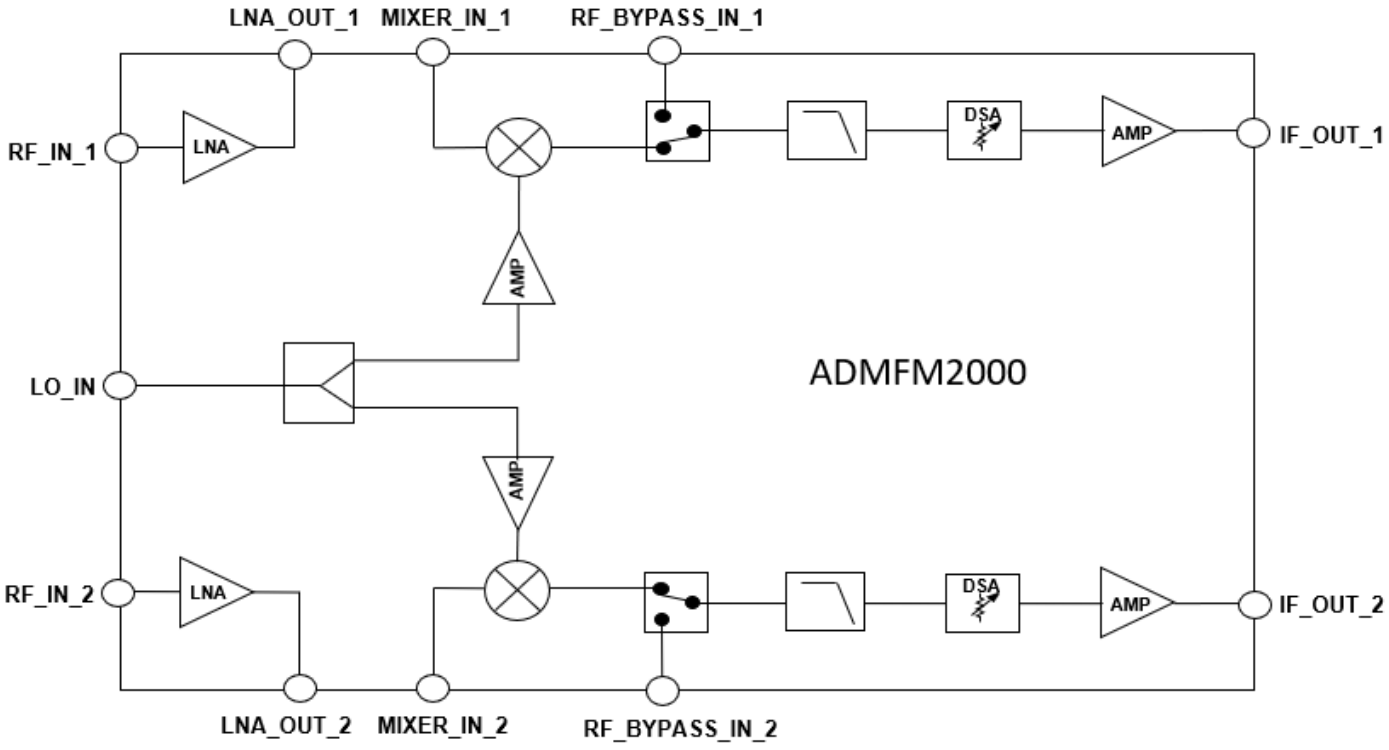

Figure 1. Functional Block Diagram

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SPECIFICATIONS

VDD_LNA_1 = VDD_LNA_2 = VDD_IF_1 = VDD_IF_2 = VDD_LO_DRIVER_1 = VDD_LO_DRIVER_2 = 5 V, VSS_DSAS = −5 V, VGG_RFAMP_1 = VGG_RFAMP_2 = VGG_LO_AMP_1 = VGG_LO_AMP_2 = open, LO_IN: P_{LO} = 6 dBm, and T_A = 25°C, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range					GHz
LNA Input		5		32	GHz
Mixer Input		5		32	GHz
Direct IF Input		0.5		8	GHz
LNA Output		5		32	GHz
IF Output		0.5		8	GHz
LO Input		7		30	GHz
LNA	Input: RF_IN_1 and RF_IN_2, output: LNA_OUT_1 and LNA_OUT_2				
Gain	18 GHz		13		dB
Gain Flatness	Over any 4 GHz of bandwidth		1		dB p-p
Gain Variation over Temperature	−40°C to +85°C		1.2		dB
Noise Figure	Single sideband, 18 GHz		3.3		dB
Input 1dB Compression Point (IP1dB)	18 GHz		0.3		dBm
Second Harmonic (HD2)	f_{RF_IN} = 9 GHz, P_{LNA_OUT} = −6 dBm		−37		dBc
Third Harmonic (HD3)	f_{RF_IN} = 9 GHz, P_{LNA_OUT} = −6 dBm		−69		dBc
Input Third-Order Intercept (IIP3)	18 GHz, 1 MHz tone spacing, output power (P_{OUT}) = −6 dBm per tone		11		dBm
Input Second-Order Intercept (IIP2)	9 GHz, 11 MHz tone spacing, P_{OUT} = −6 dBm per tone		30		dBm
Channel-to-Channel Isolation	$P_{LNA\_OUT\_1}$ to $P_{LNA\_OUT\_2}$, 18 GHz, $P_{RF\_IN\_1}$ = −20 dBm, RF_IN_2: 50 Ω termination		−60		dB
MIXER	Input: MIXER_IN_1 and MIXER_IN_2, LO: LO_IN = 6 dBm, SW1_CTRL_A = −5 V, SW1_CTRL_B = 0 V, SW2_CTRL_A = 0 V, SW2_CTRL_B = −5 V, output: IF_OUT_1 and IF_OUT_2 = 3 GHz				dB
Gain	18 GHz		−6.3		dB
Gain Flatness	Over any 4 GHz of bandwidth		1.25		dB p-p
Gain Variation over Temperature	−40°C to +85°C		1.4		dB p-p
DSA Range		0		31	dB
DSA Step Size			1		dB
Noise Figure	Single sideband		26.3		dB
IP1dB			16.5		dBm
IIP3	$f1_{MIXER\_IN}$ = 18 GHz, 1 MHz tone spacing, P_{OUT} = −15 dBm per tone		23.5		dBm
IIP2	$f1_{MIXER\_IN}$ = 9 GHz, 11 MHz tone spacing, P_{OUT} = −15 dBm per tone		39		dBm
Mixer Isolation					
RF to IF	(P_{MIXER_IN} = −10 dBm at f_{MIXER_IN}= 18 GHz) − (P_{IF_OUT} at f_{IF_OUT} = 18 GHz)		57		dB
LO to RF	(P_{LO_IN} = 8 dBm at f_{LO_IN}= 18 GHz) − (P_{MIXER_IN} at f_{MIXER_IN} = 18 GHz)		32		dB
LO to IF	(P_{LO_IN} = 8 dBm at f_{LO_IN}= 18 GHz) − (P_{IF_OUT} at f_{IF_OUT} = 18 GHz)		77		
Channel-to-Channel Isolation	MIXER_IN_2: 50 Ω termination, $P_{MIXER\_IN\_1}$ = −10 dBm at f_{MIXER_IN} = 18 GHz				

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IF to IF	$P_{IF\_OUT\_1}$ to $P_{IF\_OUT\_2}$, 3.0 GHz		-67		dB
DIRECT IF MODE	Input: RF_BYPASS_IN_1 and RF_BYPASS_IN_2, Output: IF_OUT_1 and IF_OUT_2, SW1_CTRL_A = 0 V SW1_CTRL_B = −5 V, SW2_CTRL_A = −5 V, SW2_CTRL_B = 0V				
Gain	3.0 GHz		5.0		dB
Gain Flatness	3 GHz ± 1.0 GHz		1.2		dBpp
Gain Variation over Temperature	−40°C to +85°C		0.5		dB
DSA Range		0		31	dB
DSA Step Size			1		dB
Noise Figure	Single sideband, 3.0 GHz		12.3		dB
IP1dB	3.0 GHz		15.5		dBm
HD2	P_{IF_OUT} − P(2 × f_{IF_OUT}), P_{OUT} = 5 dBm per tone		−39		dBc
HD3	P_{IF_OUT} − P(3 × f_{IF_OUT}), P_{OUT} = 5 dBm per tone		−64		dBc
IIP3	3.0 GHz, 1MHz tone spacing, P_{OUT} = 5 dBm per tone		27		dBm
IIP2	3.0 GHz, 11MHz tone spacing, P_{OUT} = 5 dBm per tone		33.5		dBm
Channel-to-Channel Isolation	$P_{IF\_OUT\_1}$ to $P_{IF\_OUT\_2}$, 3.0 GHz, $P_{RF\_BYPASS\_IN\_1}$ = −20 dBm, RF_BYPASS_IN_2: 50 Ω termination		−69		dB
LNA MIXER CASCADED	Input: RF_IN_1 and RF_IN_2, output: IF_OUT_1 and IF_OUT_2, 3 dB attenuation between LNA_OUT and MIXER_IN, SW1_CTRL_A = −5 V, SW1_CTRL_B = 0 V, SW2_CTRL_A = 0 V, SW2_CTRL_B = −5 V				
Gain	f_{RF_IN} = 18GHz, f_{IF_OUT} = 3.0 GHz		3.8		dB
DSA Range		0		31	dB
DSA Step Size			1		dB
Noise Figure	Single sideband, 3.0 GHz		12		dB
IP1dB			10.6		dBm
IIP3	18 GHz, 1 MHz tone spacing, P_{OUT} = −15 dBm per tone		6.1		dBm
IIP2	18 GHz, 1 MHz tone spacing, P_{OUT} = −15 dBm per tone		24.3		dBm
Channel-to-Channel Isolation	$P_{IF\_OUT\_1}$ to $P_{IF\_OUT\_2}$, 18 GHz, $P_{RF\_IN\_1}$ = −20 dBm, RF_IN_2: 50 Ω termination		60		dB
DSA SPECIFICATIONS					
Range		0		31	dB
Step Size	Between any successive attenuation states, 0.5 GHz to 8 GHz		1		dB
Step Error	Between any successive attenuation states, 0.5 GHz to 8 GHz		±0.5		dB
Settling Time	Minimum attenuation to maximum attenuation, t_{Fall} (90/10% RF)		38		ns
	Maximum attenuation to minimum attenuation, t_{Rise} (10/90% RF)		42		ns
	t_{ON} (50% CTL to 90% RF)		60		ns
	t_{ON}/t_{OFF}(50% CTL to 10% RF)		60		ns
LO CHARACTERISTICS					
LO Drive Level			8		dBm
Input Return Loss	LO_IN				dB
LOGIC INPUTS					
SW_CHx_CTRL_y	SW_CH1_CTRL_A, SW_CH1_CTRL_B, SW_CH2_CTRL_A, and SW_CH2_CTRL_B				
Input Low Voltage, V_{IL}		−0.2		0	V
Input High Voltage, V_{IH}		−5		−3	V
DSAx_Vy	DSA1_V0, DSA1_V1, DSA1_V2, DSA1_V3, DSA1_V4, DSA2_V0, DSA2_V1, DSA2_V2, DSA2_V3, DSA2_V4				
Input Low Voltage, V_{IL}		0		0.8	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input High Voltage, V_{IH}		2		5	V
POWER SUPPLIES					
VDD_LNA_1, VDD_LNA_2			5		V
VDD_IF_1, VDD_IF_2			5		V
VDD_LO_DRIVER_1, VDD_LO_DRIVER_2			5		V
VSS_DSAS			−5		V
VDD_LNA_x Current, $I_{VDD\_LNA\_x}$			66		mA
VDD_IF_x Current, $I_{VDD\_IF\_x}$			72		mA
VDD_LO_DRIVER_x Current, $I_{VDD\_LO\_DRIVER\_x}$			68		mA
VSS_DSAS Current, I_{VSS_DSAS}			12		mA
Total Power Consumption			2.18		W

OUTLINE DIMENSIONS

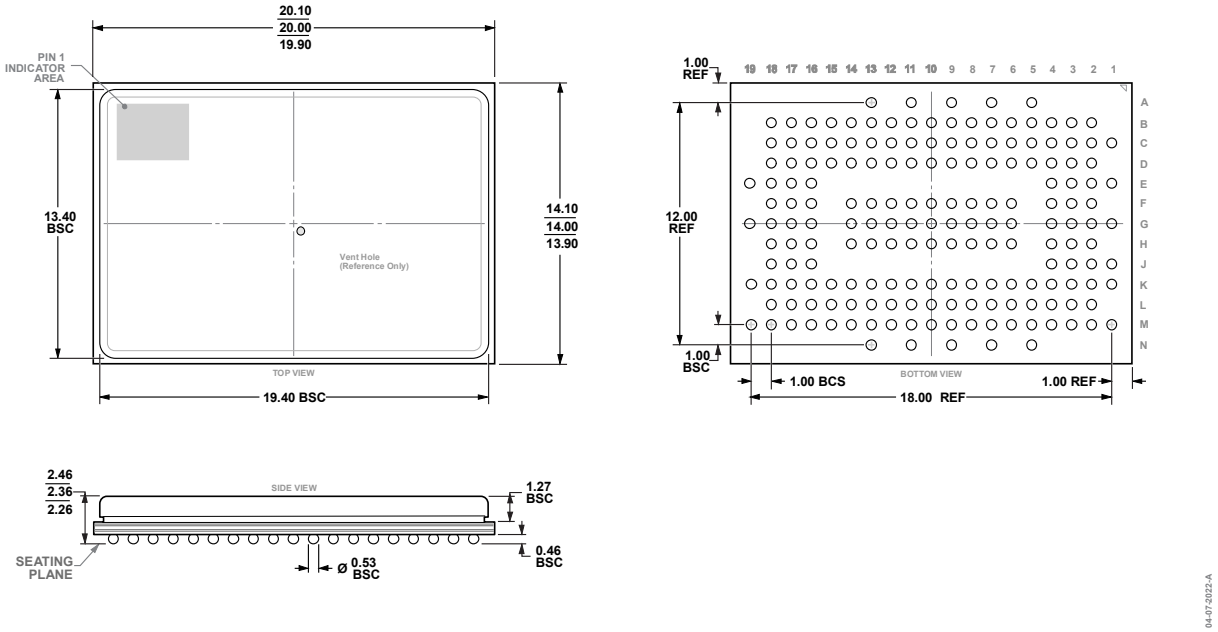

Figure 2. 179-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BV-179-1)
Dimensions shown in millimeters