SCOPE: Complete, 8-Channel, 12-Bit Data Acquisition Systems

Device Type	Generic Number	Circuit Function
01	MAX186AM(x)/883B	Low Power, 8-Channel, 12-Bit Serial
02	MAX186BM(x)/883B	ADC Track/Hold and Reference
03	MAX186CM(x)/883B	
04	MAX186DM(x)/883B	
05	MAX188AM(x)/883B	Low Power, 8-Channel, 12-Bit Serial
06	MAX188BM(x)/883B	ADC with Track/Hold
07	MAX188CM(x)/883B	
08	MAX188DM(x)/883B	

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JP	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
LP	CQCC1-N20	20-Pin LCC	L20

Absolute Maximum Ratings

V_{DD} to AGND ..... -0.3V to +6V
V_{SS} to AGND ..... +0.3V to -6V
V_{DD} to V_{SS} ..... -0.3V to +12V
AGND to DGND ..... -0.3V to +0.3V
CH0-CH7 to AGND, DGND ..... (V_{SS} -0.3V) to (V_{DD} +0.3V)
VREF to AGND ..... -0.3V to (V_{DD} +0.3V)
REFADJ to AGND ..... -0.3V to (V_{DD} +0.3V)
Digital Inputs to DGND..... -0.3V to (V_{DD} +0.3V)
Digital Outputs to DGND ..... -0.3V to (V_{DD} +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 pin CERDIP(derate 11.1mW/°C above +70°C) 889mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
20 pin CERDIP..... 40°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
20 pin CERDIP..... 90°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V_{DD}) ..... +4.75V to +5.25V
Negative Supply Voltage (V_{SS})..... -4.75V to -5.25V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, f_{CLK}=2.0MHz V_{SS}=0V or -5V, external clock (50% duty cycle). 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
ACCURACY 2/							
Resolution	N			All	12		Bits
Relative Accuracy 3/			1,2,3	01,02 05,06 03,04,08 07		±0.5 ±1.0 ±.75	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	1,2,3	All		±1.0	LSB
Offset Error	V_{OS}		1,2,3	01,05 02,03 04,06 07,08		±2.0 ±3.0	LSB
Gain Error NOTE 4		External Reference 4.096V	1,2,3	01,02 03,04 05 06,07 08		±3.0 ±1.5 ±2.0 ±3.0	LSB
DYNAMIC TESTS Bipolar Input Mode		10kHz sine wave input, 4.096Vp-p, 133ksps, 2.0MHz external clock					
Signal-to-Noise Plus Distortion	SINAD		1,2,3	All	70		dB
Total Harmonic Distortion	THD	Up to the 5th Harmonic	1,2,3	All		-80	dB
Spurious Free Dynamic Range	SFDR		1,2,3	All	80		dB
CONVERSION RATE							
Track-and-Hold Acquisition Time	tACQ		9,10,11	All		1.5	µs
Conversion Time NOTE 5	t_{CONV}	Internal clock External clock, 2mhz, 12 clocks/ conversion	9,10,11	All	5.5 6.0	10	µs
External Clock Frequency Range		Exteral compensation, 4.7µF Internal compensation, NOTE 6	4,5,6	All	0.1 0.1	2.0 0.4	MHz
ANALOG INPUT							
Input Voltage Range Single Ended and Differential NOTE 8		Unipolar, V_{SS}=0V Bipolar, V_{SS}=-5V	1,2,3	All		0 to V_{REF} ±V_{REF}/2	V
Multiplexer Leakage Current		On/Off Leakage Current, VIN=±5V	1,2,3	All	0	±1.0	µA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, f_{CLK}=2.0MHz V_{SS}=0V or -5V, external clock (50% duty cycle). 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
REFERENCE INPUT		Reference Buffer Enabled					
V_{REF} Output Voltage			1	01-04	4.076	4.116	V
V_{REF} Short Circuit Current			1,2,3	01-04		30	mA
V_{REF} Tempco			1,2,3	01-03		±80	ppm/°C
Capacitive Bypass at V_{REF}		Interenal Compensation External Compensation	test condition only	01-04	.0.0 4.7		µF
Capacitive Bypass at REF_{ADJ}		Interenal Compensation External Compensation	test condition only	01-04	.01 .01		µF
EXTERNAL REFERENCE AT V_{REF}		Buffer disabled, V_{REF}=4.096V					
Input Voltage Range			1,2,3	All	2.50	V_{DD}+ 50mV	V
Input Current			1,2,3	All		350	µA
Input Resistance			1,2,3	All	12		kΩ
Shutdown V_{REF} Input Current			1,2,3	All		10	µA
Buffer Disable Threshold REF_{ADJ}			1,2,3	All	V_{DD}- 50mV		V
EXTERNAL REFERENCE AT REF_{ADJ}							
Capacitive Bypass at V_{REF}		Internal Compensation External Compensation	1,2,3	All	0.0 4.7		µF
REF_{ADJ} Input Current			1,2,3	01-04 05-08		±50 ±5	µA
DIGITAL INPUTS		__ _____ DIN, SCLK, CS, SHDN					
__ DIN, SCLK, CS Input Voltage High	V_{INH}		1,2,3	All	2.4		V
__ DIN, SCLK, CS Input Voltage Low	V_{INL}		1,2,3	All		0.8	V
__ DIN, SCLK, CS Input Leakage	I_{IN}	V_{IN}=0V or V_{DD}	1,2,3	All		±1.0	µA
__ DIN, SCLK, CS Input Capacitance	C_{IN}	NOTE 6		All		15	pF
_____ SHDN Input High Voltage	V_{INH}		1,2,3	All	V_{DD}- 0.5		V
_____ SHDN Input Low Voltage	V_{INL}		1,2,3	All		0.5	V
_____ SHDN Input High Current	I_{INH}	_____ SHDN=V_{DD}	1,2,3	All		4.0	µA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, f_{CLK}=2.0MHz V_{SS}=0V or -5V, external clock (50% duty cycle). 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
$\overline{\text{SHDN}}$ Input Low Curent	I_{INL}	$\overline{\text{SHDN}}$=0V	1,2,3	All	-4.0		µA
$\overline{\text{SHDN}}$ Input Mid Voltage	VIM		1,2,3	All	1.5	V_{DD}-1.5	V
$\overline{\text{SHDN}}$ Max Allowed Leakage, Mid Input		$\overline{\text{SHDN}}$=open	1,2,3	All	-100	100	nA
DIGITAL OUTPUTS		DOUT, SSTRB					
Output High Voltage	V_{OH}	I_{SOURCE}=1mA	1,2,3	All	4.0		V
Output Low Voltage	V_{OL}	I_{SINK}=5mA	1,2,3	All		0.4	V
Three-State Leakage Current	I_{LKG}	$\overline{\text{CS}}$=5V	1,2,3	All		±10	µA
Three-State Output Capacitance NOTE 5	C_{OUT}	NOTE 6		All		15	pF
POWER REQUIREMENTS							
Positive Supply Current	I_{DD}	Operating Mode	1,2,3	All		2.5	mA
		Fast power-down				70.0	µA
		Full power-down				10.0	
Negative Supply Current	I_{SS}	Operating mode and fast power-down	1,2,3	All		50.0	µA
		Full power-down				10.0	
Positive Supply Rejection NOTE 7	PSR	V_{DD}=+5V ±5%, external reference, 4.096V; full-scale input	1,2,3	All		±0.5	mV
Negative Supply Rejection NOTE 7	PSR	V_{DD}=-5V ±5%, external reference, 4.096V; full-scale input	1,2,3	All		±0.5	mV
TIMING		V_{DD}=+5V ±5%, VSS=0V or -5V Unless otherwise specified					
Acquisition Time	t_{AZ}		9,10,11	All	1.5		µs
DIN to SCLK Setup	t_{DS}		9,10,11	All	100		ns
DIN to SCLK Hold	t_{DH}		9,10,11	All		0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD}=100pF	9,10,11	All	20	200	ns
$\overline{\text{CS}}$ Fall to Output Enable	t_{DV}	C_{LOAD}=100pF	9,10,11	All		100	ns
$\overline{\text{CS}}$ Rise to Output Disable	t_{TR}	C_{LOAD}=100pF	9,10,11	All		100	ns
$\overline{\text{CS}}$ to SCLK Rise Setup	t_{CSS}		9,10,11	All	100		ns
$\overline{\text{CS}}$ to SCLK Rise Hold	t_{CSH}		9,10,11	All	0		ns
SCLK Pulse Width High	t_{CH}		9,10,11	All	200		ns
SCLK Pulse Width Low	t_{CL}		9,10,11	All	200		ns
SCLK Fall to SSTRB	tSSTRB	C_{LOAD}=100pF	9,10,11	All		200	ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V_{DD}=+5V±5%, V_{SS}=0V or -5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
$\overline{CS}$ Fall to SSTRB Output Enable NOTE 6	t_{SDV}	External clock mode only, C_{LOAD}=100pF	9,10,11	All		200	ns
$\overline{CS}$ Rise to SSTRB Output Disable NOTE 6	t_{STR}	External clock mode only, C_{LOAD}=100pF	9,10,11	All		200	ns
SSTRB Rise to SCLK Rise NOTE 6	t_{SCK}	Internal clock mode only	9,10,11	All	0		ns

NOTE 1: 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at V_{REF} pin; MAX188 - external refence, V_{REF}=4.096V applied to V_{REF} pin.
NOTE 2: Tested at V_{DD}=+5V, V_{SS}=0V, unipolar input mode.
NOTE 3: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
NOTE 4: MAX186-internal reference, offset nulled; MAX188-external reference (V_{REF} = +4.096V), offset nulled.
NOTE 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle
NOTE 6: Guaranteed by design. Not production tested.
NOTE 7: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only..
NOTE 8: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

Package	ORDERING	INFORMATION:		
20 pin CERDIP	MAX186AMJP/883B	MAX186BMJP/883B	MAX186CMJP/883B	MAX186DMJP/883B
20 pin CERDIP	MAX188AMJP/883B	MAX188BMJP/883B	MAX188CMJP/883B	MAX188DMJP/883B
20 pin LCC	MAX186AMLP/883B	MAX186BMLP/883B	MAX186CMLP/883B	MAX186DMLP/883B
20 pin LCC	MAX188AMLP/883B	MAX188BMLP/883B	MAX188CMLP/883B	MAX188DMLP/883B

TERMINAL CONNECTIONS:

MAX186	& MAX188
1	CH0
2	CH1
3	CH2
4	CH3
5	CH4
6	CH5
7	CH6
8	CH7
9	V_{SS}
10	$\overline{SHDN}$
11	V_{REF}
12	REF_{ADJ}
13	AGND
14	DGND
15	DOUT
16	SSTRB
17	DIN
18	$\overline{CS}$
19	SCLK
20	V_{DD}

MODE SELECTION TABLE:

		Channel Selection in Single-Ended Mode $\overline{\quad\quad}$ (SGL/DIFF=1)											
		SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
1	CH0	0	0	0	+								-
2	CH1	0	0	1		+							-
3	CH2	1	0	0			+						-
4	CH3	0	0	1				+					-
5	CH4	1	0	1					+				-
6	CH5	0	1	0						+			-
7	CH6	1	1	0							+		-
8	CH7	0	1	1								+	-
9	V_{SS}	1	1	1								+	-
10	$\overline{SHDN}$	Channel Selection in Differential Mode $\overline{\quad\quad}$ (SGL/DIFF =0)											
11	V_{REF}	SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
12	REF_{ADJ}	0	0	0	+	-							
13	AGND	0	0	1			+	-					
14	DGND	0	1	0					+	-			
15	DOUT	0	1	1							+	-	
16	SSTRB	1	0	0	-	+							
17	DIN	1	0	1			-	+					
18	$\overline{CS}$	1	1	0					-	+			
19	SCLK	1	1	1							-	+	
20	V_{DD}												

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4, 5, 6, 7, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 7, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.