DESCRIPTION

The RH108A is a precision operational amplifier particularly well-suited for high source impedance applicationsrequiring low offset and bias currents and low power-consumption.

The wafer lots are processed to Linear Technology's in-house Class S flow to yield circuits usable in stringent-military applications.

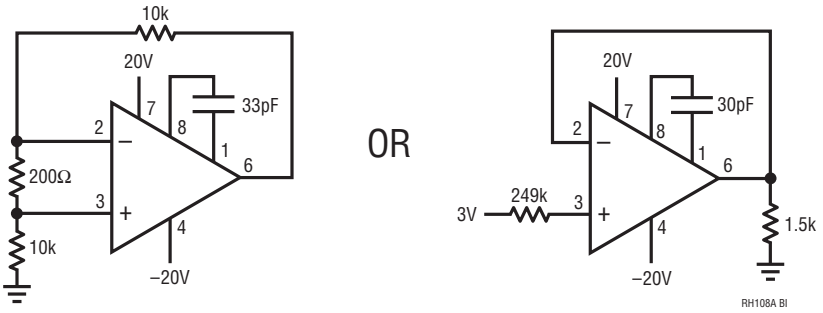
For complete electrical specifications, performance curves and applications information, see the LM108A/LM108 data sheet.

ABSOLUTE MAXIMUM RATINGS

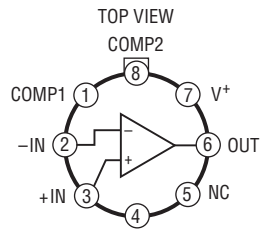
(Note 1)

Supply Voltage ..... ±20V
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

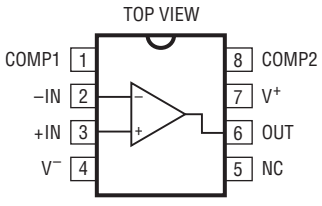
BURN-IN CIRCUIT



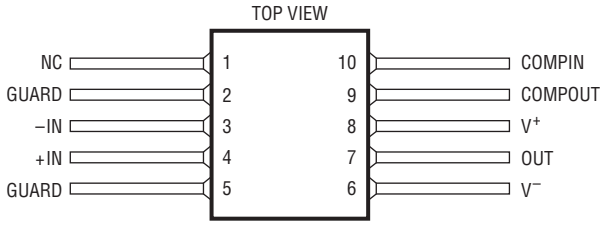
PACKAGE INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN



J8 PACKAGE
8-LEAD CERDIP



W PACKAGE
10-LEAD CERPAC

TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation, Note 4)

Device is characterized at the TID levels below. Device is production tested at 100kRad(si).

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	–55°C ≤ T_A ≤ 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage					0.5	1			1.0	2,3	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage		3							5.0		µV/°C
I_{OS}	Input Offset Current					0.2	1			0.4	2,3	nA
$\frac{\Delta I_S}{\Delta Temp}$	Average Tempco of Offset Current		3							2.5		pA/°C
I_B	Input Bias Current					2.0	1			3.0	2,3	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 10k		80			4	40			5,6	V/mV
CMRR	Common Mode Rejection Ratio			96			1	96			2,3	dB
PSRR	Power Supply Rejection Ratio			96			1	96			2,3	dB
	Input Voltage Range	V_S = ±15V	3	±13.5				±13.5				V
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10k		±13			4	±13			5,6	V
R_{IN}	Input Resistance		3	30								MΩ
I_S	Supply Current	(Note 6)				0.6	1			0.4	2	mA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Preirradiation, Note 4)

Device is characterized at the TID levels below. Device is production tested at 100kRad(si).

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si) MIN	MAX	20KRAD (Si) MIN	MAX	50KRAD (Si) MIN	MAX	80KRAD (Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage				0.5		0.5		0.5		1.0	mV
I_{OS}	Input Offset Current				0.3		0.3		0.3		0.3	nA
I_B	Input Bias Current				±2.0		±2.0		±2.0		±4.0	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 10k		98		98		90		86		dB
CMRR	Common Mode Rejection Ratio			96		96		84		70		dB
PSRR	Power Supply Rejection Ratio		4	96		96		84		70		dB
	Input Voltage Range		3	±13.5		±13.5		±13.5		±13.5		V
V_{OUT}	Output Voltage Swing			±13		±13		±13		±13		V
R_{IN}	Input Resistance		3	30		30		30		30		MΩ
I_S	Supply Current				0.6		0.6		0.6		0.6	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: For supply voltages less than ±15V, the maximum input voltage isequal to the supply voltage.

Note 3: Guaranteed by design, characterization or correlation to othertested parameters.

Note 4: ±5V ≤ V_S ≤ ±20V preirradiation, ±5V ≤ V_S ≤ ±15V postirradiation, unless otherwise noted.

Note 5: V_S = ±15V, V_{CM} = 0V, T_A = 25°C unless otherwise noted.

Note 6: 25°C ≤ T_A ≤ 125°C.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group C and D End Point Electrical Parameters (Method 5005)	1

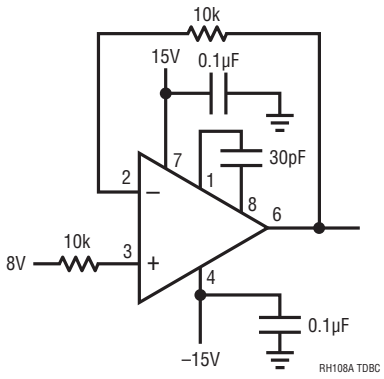
*PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

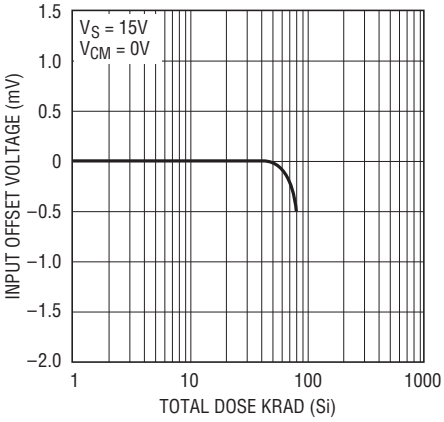


REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/10	Note 4 revised and added to Power Supply Rejection Ratio.	2
D	7/23	Updated art title in the Electrical Characteristics section and updated the document to ADI format	1–4

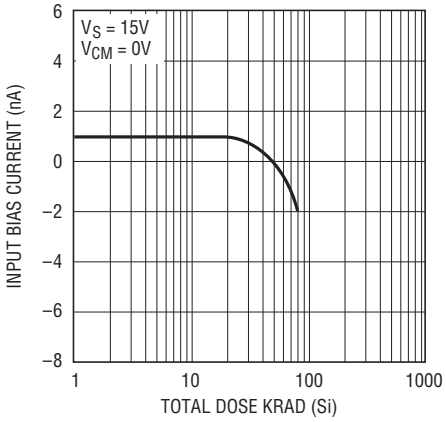
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



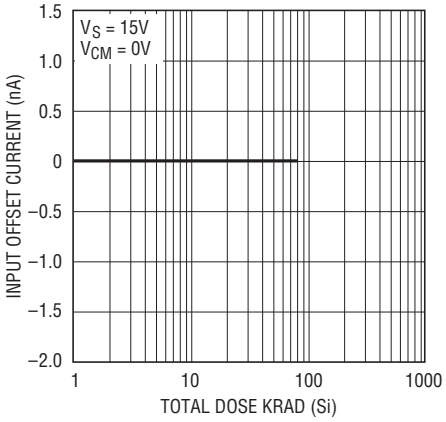
RH108A G01

Input Bias Current



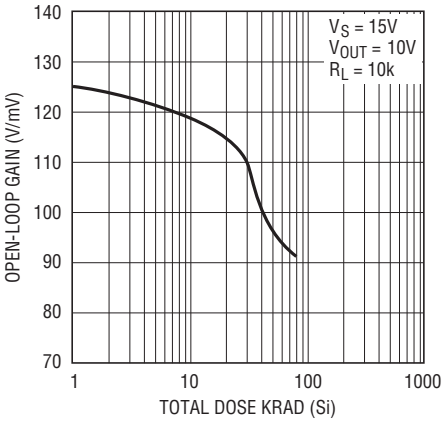
RH108A G02

Input Offset Current



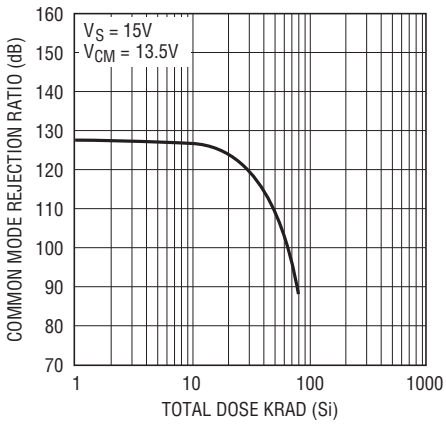
RH108A G03

Open-Loop Gain



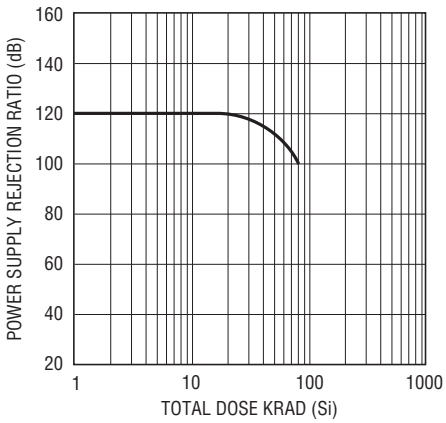
RH108A G04

Common Mode Rejection Ratio



RH108A G05

Power Supply Rejection Ratio



RH108A G06