Small, Dual-Channel, Precision, Programmable-Gain, Transimpedance Amplifiers (PGTIAs)

FEATURES

- Small, dual, precision TIAs with integrated switches/gains
  - ADA4351-2 integrated switches, 2 external gains per channel
  - ADA4352-2 integrated switches, 4 integrated gains per channel
- Wide Input Current Range
  - <100 pA to 15 mA
- Excellent DC Precision
  - Low offset voltage: 100 µV maximum
  - Low offset voltage drift: 0.6 µV/°C maximum, 0°C to 85°C
  - Low input bias current: 9 pA maximum
  - Low off leakage proprietary switches: 130 pA maximum(-40°C to 125°C)
  - New proprietary architecture eliminates Gain error due to switch R_{ON}
- Low noise: 7.8 nV/√Hz at 100 kHz
- Single supply operation: 3 V to 5.5 V
- Quiescent current: 3.3 mA per channel
- Operating Temperature Range: -40°C to +125°C
- Small size package: 16 lead LFCSP, 3 mm x 3 mm

APPLICATIONS

- Precision current to voltage (I to V) conversion
- Programmable-Gain TIAs (PGTIAs™)
- Photodetector interface and amplification
- Optical equipment and networks
- Optical power measurement
- Instrumentation—spectroscopy
- Precision data acquisition systems (DAQ)

TYPICAL APPLICATION DIAGRAM

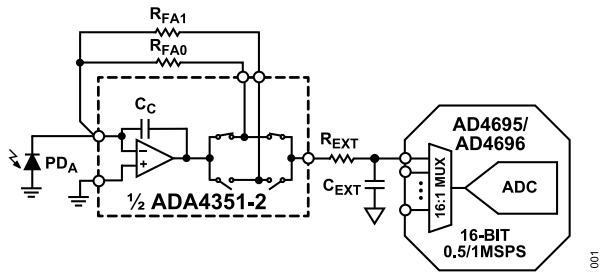

Figure 1. Optical Power Measurement Signal Chain

GENERAL DESCRIPTION

The ADA4351-2/ADA4352-2 are integrated dual-channel transimpedance amplifiers (TIAs) including a proprietary gain switching architecture in a small 3 mm x 3 mm 16 lead LFCSP. They feature excellent dc precision performance over temperature (−40°C to +125°C). Their precision can eliminate the need for calibration over temperature, therefore reducing equipment test time and cost. The ADA4351-2/ADA4352-2 exhibit low noise and can drive SAR (AD4696) or Σ-Δ (AD7xxx) ADCs directly, further reducing system complexity and cost.

The dual-channel ADA4351-2 provides the user flexibility to choose two gain states per channel via external resistors. The dual-channel ADA4352-2 reduces board space use by integrating four internal gain states per channel, using internal thin film resistors with excellent linearity, optimizing dynamic range, and performance over temperature. Additionally, the ADA4352-2 gains are internally compensated eliminating the need for external compensation capacitors, further reducing board space requirements. Both products utilize proprietary low leakage internal switch architectures to minimize off-leakage and errors due to on-resistance.

Both are offered in a 16 lead 3x3 mm LFCSP package with no EPAD on the backside of the package. This eliminates the need for vias and allows routing on all layers underneath the device for the smallest PGTIA™ solution.

For typical performance curves, contact ADA4351-2_ADA4352-2@analog.com.

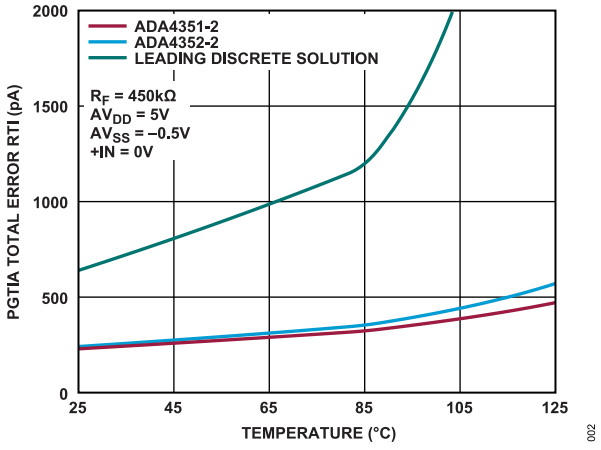

Figure 2. PGTIA Total Error RTI vs. Temperature (Total Error Includes I_{BIAS}, V_{OS}, and Switch Leakage)

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FUNCTIONAL BLOCK DIAGRAMS

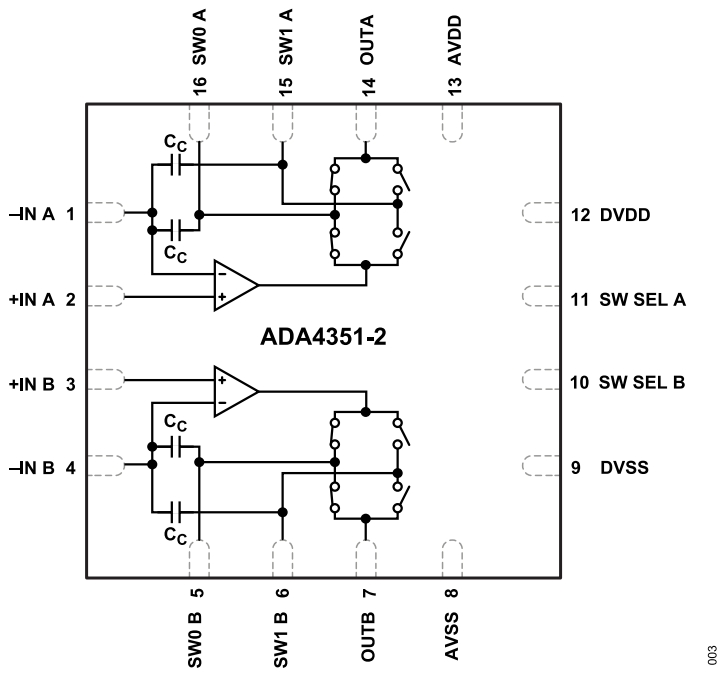

Figure 3. ADA4351-2 Functional Block Diagram

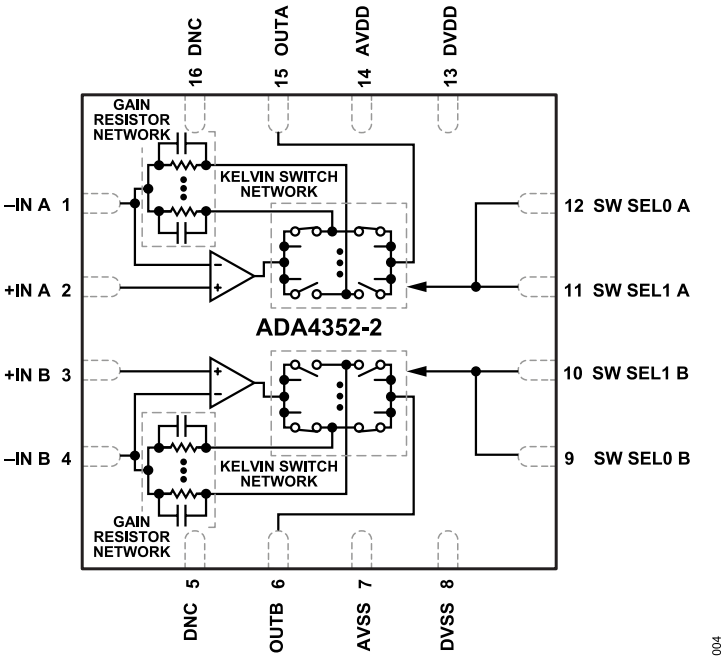

Figure 4. ADA4352-2 Functional Block Diagram

SPECIFICATIONS

T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3 V, DVSS = 0 V, R_L = open, +IN = 2.5 V, unless otherwise noted.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Open-Loop Gain	R_F = 10 kΩ, V_{OUT} = 0.5V to 4.5V	TBD	130		dB
	V_{OUT} = 0.1 V to 4.9 V	TBD	130		dB
Offset Voltage, RTI	R_F = 10 kΩ		20	100	µV
Offset Voltage Drift, RTI	R_F = 10 kΩ, T_A = 0°C to +85°C			±0.6	µV/°C
	T_A = −40°C to +125°C			±1	µV/°C
Input Bias Current	T_A = 25°C			9	pA
	T_A = −40°C to +85°C			TBD	pA
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			TBD	pA
INPUT CHARACTERISTICS					
Common Mode Input Impedance			1/2.5		GΩ/pF
Input Common-Mode Voltage Range (V_{CM})	T_A = −40°C to +125°C	AVSS + 0.1[1]		AVDD − 1.5	V
Common-Mode Rejection	V_{CM} = 0.1 V to 2.6 V	TBD	92		dB
	V_{CM} = 2.6 V to 3.5 V	TBD	102		dB
OUTPUT CHARACTERISTICS					
Output Voltage Range	R_F = 10 kΩ, R_L = open	AVSS + 0.1		AVDD – 0.1	V
Maximum Output Current				15	mA RMS
Short-Circuit Current	Sinking and sourcing		±60		mA
Settling Time	12 bit and 16 bit, +IN = TBD		TBD/TBD		µs
Overload Recovery			TBD		ns
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			8		MHz
Slew Rate, Peak			8		V/µs
HARMONIC DISTORTION					
Harmonic Distortion (HD2/HD3)	G = −1		TBD/TBD		dBc
ANALOG POWER SUPPLY (AVDD AND AVSS)					
Operating Range (V_S = AVDD − AVSS)		3		5.5	V
AVSS Range				DVSS	V
Quiescent Current	Per amplifier		3.3		mA
Power Supply Rejection Ratio	V_S = 3 V to 5.5 V, T_A = −40°C to +125°C		TBD		dB
	V_S = 3 V to 5.5 V	TBD	90		dB
	V_S = 4.75 V to 5.25 V	TBD	105		dB
THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS					
Input High Voltage		DVDD − 0.7			V
Input Low Voltage				DVSS + 0.5	V
DIGITAL POWER SUPPLY (DVDD AND DVSS)					
Operating Range (V_S = DVDD − DVSS)		1.8		5.5	V
Quiescent Current				1	µA
ANALOG SWITCH					
Switch On-Resistance	T_A = −40°C to +125°C		15	25	Ω
On-Resistance Drift	T_A = −40°C to +125°C		0.4		%/°C
Switch Off Input Capacitance	T_A = −40°C to +125°C		1.6		pF
Switch Off Leakage Current					
AVSS + 0.5 < +IN < AVDD − 1.5					
	T_A = 25°C			6	pA

SPECIFICATIONS

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	T_A = −40°C to +85°C			TBD	pA
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			130	pA
AVSS + 0.1 < +IN < AVDD − 1.5					
	T_A = 25°C			10	pA
	T_A = −40°C to +85°C			TBD	pA
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			170	pA
NOISE					
Input Voltage Noise	f = 100 kHz		7.8		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.4		µV RMS

[1] Device is operational at V_{CM} = AVSS; however, specifications listed are not guaranteed. Refer to applications section for further details.

T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 3 V, DVSS = 0 V, R_L = open, +IN = 1.5 V, unless otherwise noted.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Open-Loop Gain	V_{OUT} = 0.5 V to 2.5 V	TBD	120		dB
	V_{OUT} = 0.1 V to 2.9 V	TBD	123		dB
Offset Voltage, RTI			20	150	µV
Offset Voltage Drift, RTI	T_A = 0°C to +85°C			±0.6	µV/°C
	T_A = −40°C to +125°C			±1	µV/°C
Input Bias Current	T_A = 25°C			9	pA
	T_A = −40°C to +85°C			TBD	
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			TBD	pA
INPUT CHARACTERISTICS					
Common Mode Input Impedance			1/2.5		GΩ/pF
Input Common-Mode Voltage Range (V_{CM})	T_A = −40°C to +125°C	AVSS + 0.1[1]		AVDD − 1.5V	V
Common-Mode Rejection	V_{CM} = 0.1 V to 2.6 V	TBD	91		dB
	V_{CM} = 2.6 V to 3.5 V				
OUTPUT CHARACTERISTICS					
Output Voltage Range	R_F = 10 kΩ, R_L = open	AVSS + 0.1		AVDD – 0.1	V
Maximum Output Current				15	mA RMS
Short-Circuit Current	Sinking and sourcing		TBD		mA
Settling Time	12 bit and 16 bit, +IN = TBD		TBD/TBD		µs
Overload Recovery			TBD		ns
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			TBD		MHz
Slew Rate, Peak			TBD		V/µs
HARMONIC DISTORTION					
Harmonic Distortion (HD2/HD3)	G = −1		TBD/TBD		dBc
ANALOG POWER SUPPLY (AVDD ANDD AVSS)					
Operating Range (V_S = AVDD − AVSS)		3		5.5	V
AVSS Range				DVSS	V
Quiescent Current	Per amplifier		3		mA

SPECIFICATIONS

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply Rejection Ratio	V_S = 3 V to 3.75 V, T_A = −40°C to +125°C		TBD		dB
	V_S = 3 V to 3.75 V	TBD	98		dB
THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS					
Input High Voltage		DVDD − 0.7			V
Input Low Voltage				DVSS + 0.5	V
DIGITAL POWER SUPPLY (DVDD AND DVSS)					
Operating Range (DVDD − DVSS)		1.8		5.5	V
Quiescent Current				TBD	µA
ANALOG SWITCH					
Switch On-Resistance	T_A = −40°C to +125°C		21	TBD	Ω
On-Resistance Drift	T_A = −40°C to +125°C		0.4		%/°
Switch off Input Capacitance	T_A = −40°C to +125°C		1.6		pF
Switch Off Leakage Current					
AVSS + 0.5 < +IN < AVDD − 1.5					
	T_A = 25°C			6	pA
	T_A = −40°C to +85°C			TBD	pA
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			130	pA
AVSS + 0.1 < +IN < AVDD − 1.5					
	T_A = 25°C			10	pA
	T_A = −40°C to +85°C			TBD	pA
	T_A = −40°C to +105°C			TBD	pA
	T_A = −40°C to +125°C			170	pA
NOISE					
Input Voltage Noise	f = 100 kHz		TBD		nV/√Hz
	f = 0.1 Hz to 10 Hz		TBD		µV RMS

[1] Device is operational at V_{CM}= AVSS; however, specifications listed are not guaranteed. Refer to applications section for further details.

ADA4352-2 GAIN SPECIFICATIONS

T_A = 25°C, AVDD = 5 V and 3 V, AVSS = 0 V, DVDD = 1.8 V, DVSS = 0 V, R_L = open, +IN = 2.5 V, unless otherwise noted.

Table 1. ADA4352-2 Gain Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Internal Gain Resistor					
RG0	SW SEL1 = 0, SW SEL0 = 0	284	315	346	Ω
RG1	SW SEL1 = 0, SW SEL0 = 1	3.16	3.5	3.86	kΩ
RG2	SW SEL1 = 1, SW SEL0 = 0	36.2	40	44.2	kΩ
RG3	SW SEL1 = 1, SW SEL0 = 1	405	450	495	kΩ
TCR			−15		ppm/°C

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
Voltage Between Any Two Pins	6 V
DVDD, AVDD to DVSS	−0.3 V to +6 V
DVDD, AVDD, DVSS to AVSS	−0.3 V to +6 V
+IN A, −IN A, +IN B, −IN B Voltage	AVSS − 1 V to AVDD + 1 V
+IN A, −IN A, +IN B, −IN B Current	10 mA
SW0 A, SW0 B, SW1 A, SW1 B	AVSS − 0.3 V to AVDD + 0.3 V
SW SEL A, SW SEL B, SW SEL0 A, SW SEL1 A, SW SEL0 B, SW SEL1 B	DVSS − 0.3 V to DVDD + 0.3 V
SW SEL A, SW SEL B, SW SEL0 A, SW SEL1 A, SW SEL0 B, SW SEL1 B Current	10 mA
Op amp Output Continuous Current	20 mA[1]
Switch Continuous Current	20 mA[1]

[1] Specified at 100°C. See derating curve for temperatures beyond 100°C (See Figure 5).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 5 lists the θ_{JA} for the ADA4351-2 and ADA4352-2 in the 16-Lead LFCSP package.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	91	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4351-2 and ADA4352-2 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses the package exerts on the die, permanently shifting the parametric performance of the ADA4351-2 and ADA4352-2. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (PD) is the sum of the quiescent power dissipation and the power dissipated in the die due to the amplifier's output load drive.

CURRENT DERATING CURVE

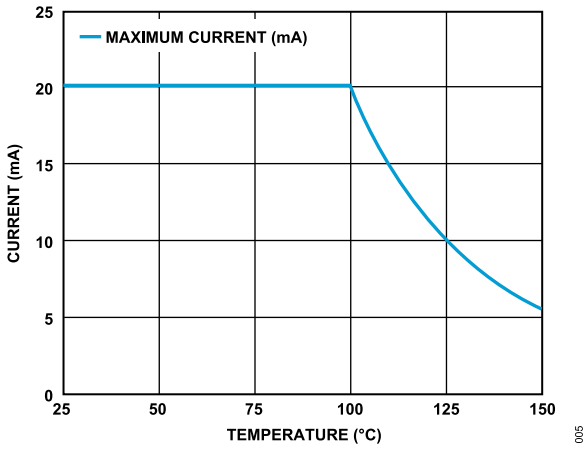

Figure 5. Maximum Derating Curve vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

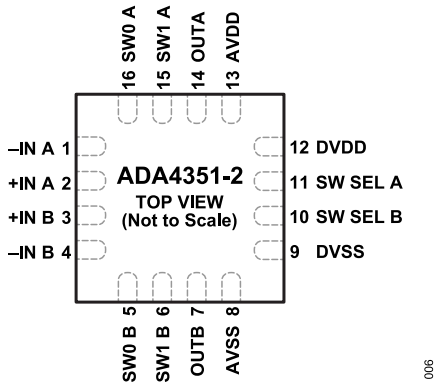

Figure 6. ADA4351-2 Pin Configuration

Table 4. ADA4351-2 Pin Function Description

Pin No.	Mnemonic	Description
1	−IN A	Inverting Input of Amplifier A
2	+IN A	Noninverting Input of Amplifier A
3	+IN B	Noninverting Input of Amplifier B
4	−IN B	Inverting Input of Amplifier B
5	SW0 B	Switch 0 Feedback Pin for Amplifier B
6	SW1 B	Switch 1 Feedback Pin for Amplifier B
7	OUTB	Output of Amplifier B
8	AVSS	Analog Negative Supply Voltage
9	DVSS	Digital Negative Supply Voltage
10	SW SEL B	Switch Control in Amplifier B
11	SW SEL A	Switch Control in Amplifier A
12	DVDD	Digital Positive Supply Voltage
13	AVDD	Analog Positive Supply Voltage
14	OUTA	Output of Amplifier A
15	SW1 A	Switch 1 Feedback Pin for Amplifier A
16	SW0 A	Switch 0 Feedback Pin for Amplifier A

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

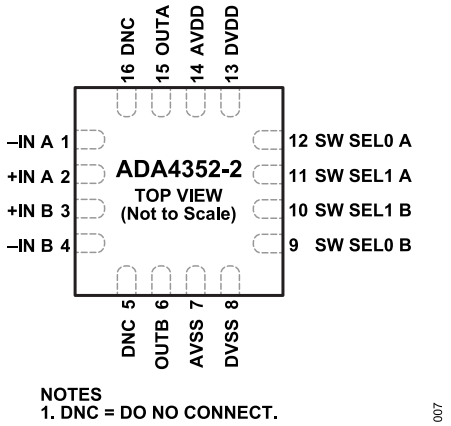

Figure 7. ADA4352-2 Pin Configuration

Table 5. ADA4352-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN A	Inverting Input of Amplifier A
2	+IN A	Noninverting Input of Amplifier A
3	+IN B	Noninverting Input of Amplifier B
4	−IN B	Inverting Input of Amplifier B
5	DNC	Do Not Connect
6	OUTB	Output of Amplifier B
7	AVSS	Analog Negative Supply Voltage
8	DVSS	Digital Negative Supply Voltage
9, 10	SW SEL1 B, SW SEL0 B	Switch Control in Amplifier B
11, 12	SW SEL1 A, SW SEL0 A	Switch Control in Amplifier A
13	DVDD	Digital Positive Supply Voltage
14	AVDD	Analog Positive Supply Voltage
15	OUTA	Output of Amplifier A
16	DNC	Do Not Connect

TRUTH TABLES

Table 6. ADA4351-2 Truth Table

SW_SELx	SW0x	SW1x
0	On	Off
1	Off	On

Table 7. ADA4352-2 Truth Table

SW_SELx1	SW_SELx0	Selected Gain Resistor
0	0	315 Ω
0	1	3.5 kΩ
1	0	40 kΩ
1	1	450 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

Contact ADA4351-2_ADA4352-2@analog.com for Typical Performance Characteristics.

APPLICATIONS INFORMATION

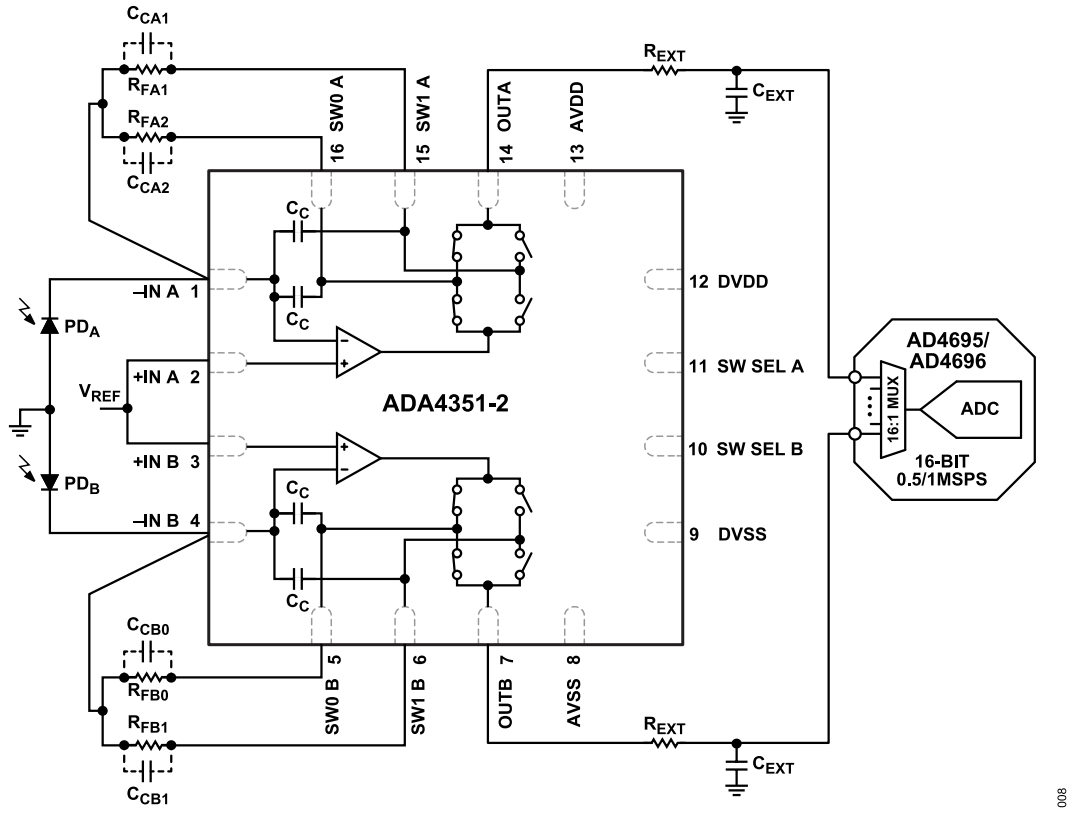

Figure 8. ADA4351-2 Applications Diagram, Two Customer Selectable External Gain Resistors per Channel

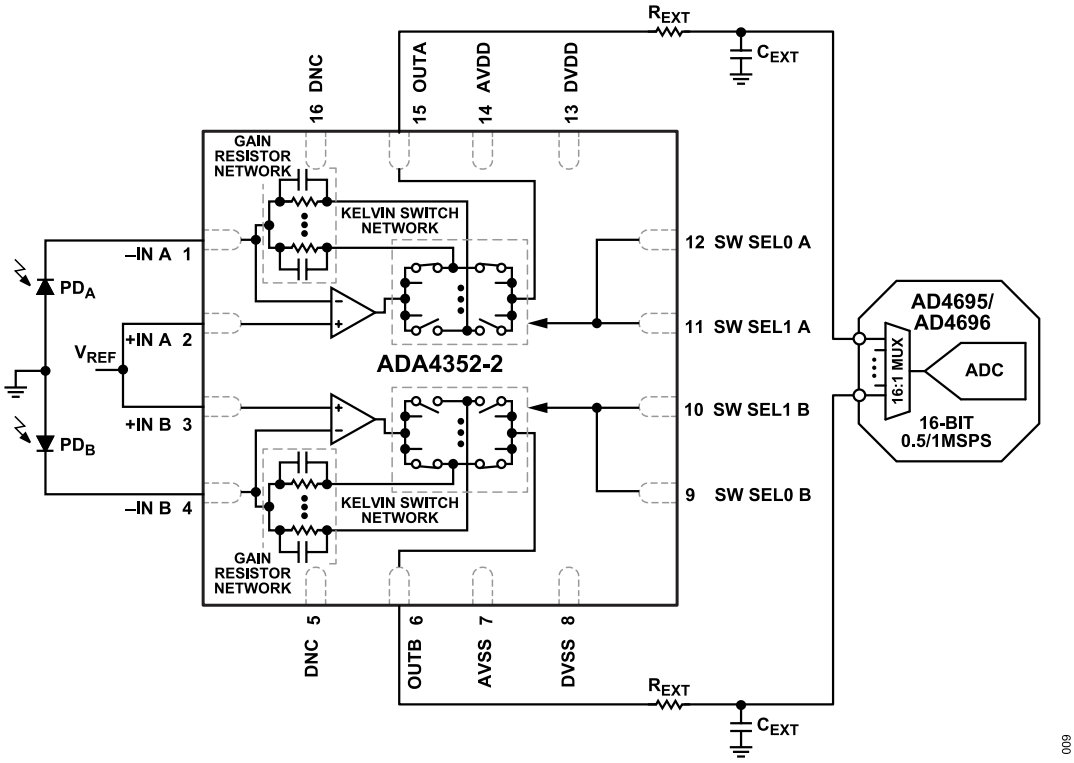

Figure 9. ADA4352-2 Applications Diagram, Four Internal Gain Resistors per Channel

OUTLINE DIMENSIONS

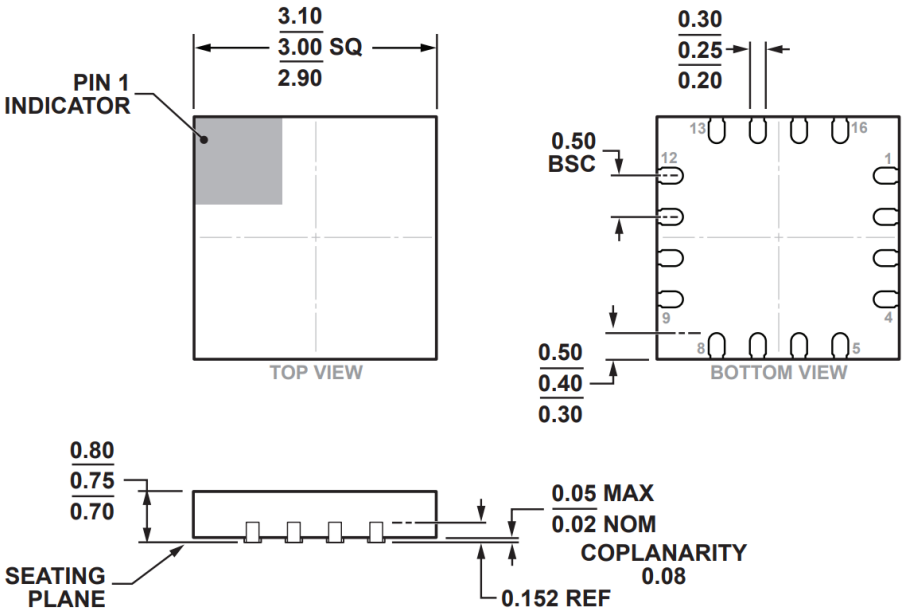

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP]