DEBUGGING MIX-UP?

The industry standard 8052 microcontroller today includes timers, counters, a UART, and on-chip RAM and ROM. Semiconductor manufacturers have integrated ultra-high precision analogue I/O peripherals like 12- to 24bit ADCs and precision DACs on chip, offering a fully integrated system-on-chip solution. This level of integration presents new challenges in terms of debugging the embedded software and hardware system.

Debugging issues

Embedded system designers can make extensive use of modern microcontroller-based code simulators, to prove functionality of a great portion of code before running on a real hardware platform.

These simulators can accept assembled microcontroller code and allow the user to single step through the code execution in a Windows-based environment.

A 'burn and learn' approach can be adopted on OTP or EPROM-based microcontrollers. PC-assembled code is programmed onto the ROM-based microcontroller via a device programmer. External port pins can be used to drive LEDs on/off when the code gets to certain points in its execution. External interrupt inputs can be used to trigger specific debug events dumping internal register contents via the UART to an PC or dumb serial port terminal to confirm microcontroller core status.

As manufacturers integrate more peripheral functions into microcontrollers, the resulting small, large pin-count package makes the socket based approach impractical.

These constraints have led to the development of an on-chip (software) debug monitor strategy. A debug-monitor is programmed onto the device with the user's run-time code. The on-chip debug monitor typically communicates with a host PC's, Windows-based debug monitor via a serial link.

Today, many different 8bit architectures proliferate, and predications of the demise of the 8bit microcontroller are greatly exaggerated

This strategy is called intrusive debug, because the on-chip debug monitor uses on-chip resources like the serial port for communication. The debug monitor sets break points in software by replacing the code instruction at a break point location by a jump instruction directly to the debug monitor code. Because the monitor must modify (or reprogram) the code memory to set a break point, it is not a strategy that can be used in EPROM or OTP devices. Some on-chip monitors will be interrupt-driven; this means that designers may not be able to set debug break points within interrupt service routines in their own code.

In-circuit emulators provide a debug option where an emulation pod electrically replicates the functionality of the microcontroller. The functionality of the real device can be emulated from a PC-based debug front-end.

Many modern emulators have additional RAM to trace real-time code execution. Given

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the developments in packages, it is often difficult to achieve a robust mechanical connection between the emulation pod and the target device PCB footprint.

With the emergence of the latest generation of mixed signal devices, system designers want to debug the functionality of the microcontroller and digital peripherals and also verify the performance of the precision ADC and DAC circuits on the microcontroller in-circuit during debug. Extended cabling or daughtercard pods in many emulation systems can make verification of precision analogue circuits in-circuit, an impossibility.

On-chip debugging

JTAG-based debugging systems are being used on 8bit microcontroller devices.

Here, a PC-hosted debug front-end has a serial port or parallel port connection to an external pod which translates the PC based communications protocol into the required JTAG interface signals. This type of on-chip debugging supports all of the standard non-intrusive debug features and lets the system engineer evaluate the true (in-circuit) analogue performance of a mixed signal solution while developing the final target embedded system.

The major components of the IEEE1149.1 JTAG architecture are the test access pins, the JTAG scan chain and the test access port (TAP) controller. To support debugging functionality some additional extensions are required, including break point registers, scan register and control logic.

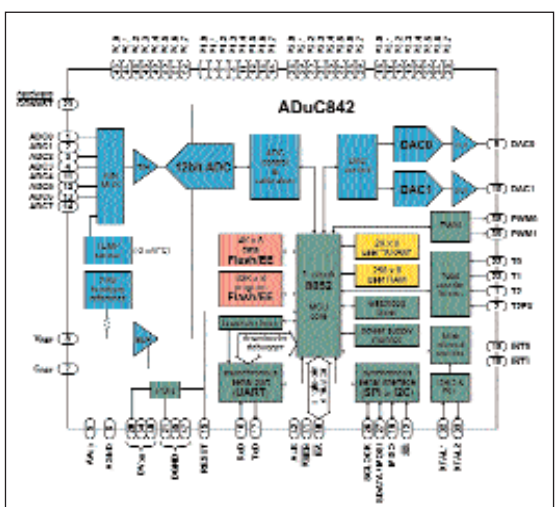

Figure 1: The ADuC842 block diagram

Break points are set in hardware, so most have a finite limit on the break points that can be set. This limit is set by the number of hardware break point registers that are supported in the specific microcontroller JTAG implementation.

As some 8bit microcontroller devices shrink in size, the standard physical external connector for JTAG connection on the PCB should be a 10-way box header type. In many small form factor embedded systems there may not be room to incorporate the standard JTAG external connector.

To meet debug challenges, Analog Devices has enhanced its QuickStart development environment for its MicroConverter family of mixed signal, 8052-based microcontrollers.

The latest addition is the ADuC842. This integrates a self calibrating multi-channel 12bit ADC, dual 12bit DAC and an optimised single cycle 16MHz, 8bit MCU (8051 instruction set-compatible) on a single chip.

The microcontroller offers up to 16MIPS peak performance. There is 62kByte of non-volatile Flash/EE program memory on-chip, with 4kBbyte of nonvolatile Flash/EE data memory, 256Byte RAM and 2kByte of extended RAM. Additional analogue functionality is provided with two 12bit DACs, power supply monitor, and a bandgap reference. On-chip digital peripherals include two 16bit sigma-delta DACs, dual output 16bit PWM, watchdog timer, time interval counter, three timers/counters, and three serial I/O ports.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the EA pin. The part is specified for 3 and 5V operation and is packaged in a 52-lead PQFP or 56-lead chip scale package.The company has worked with Accutron (**www.accutron.com**), to create a patented single pin, on-chip debug scheme. The debug path communicates with a non-intrusive on-chip debug monitor on a factory Flash memory space and does not take up any user code space. Because the emulation path involves a single pin, the debug environment can be incorporated in a very small form factor, embedded system development, with the external PCB connector comprising of the single pin referenced to a system ground.

The system does not use any of the on-chip resources. The debug path allows the designer to debug code and general system digital functionality as well as measuring the on-chip precision ADCs and DACs.

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