19-2928; Rev 1; 2/07

可提供评估板

四通道铜缆信号调理器

MAX3983

概述

MAX3983是工作于2.5Gbps至3.2Gbps的四通道铜缆信号调理器。它能够为4x铜质InfiniBand和10Gbase-CX4以太网链路提供补偿，允许跨距达20米的24AWG和15米的28AWG电缆连接。电缆驱动器单元提供四种可选的预加重级别。电缆驱动器的输入可补偿最长0.5米的FR4电路板。电缆接收器单元提供固定的输入均衡，同时，为驱动长达0.5米的FR4电路板提供可选的预加重。

MAX3983在所有八个输入通道上还具有信号检测功能和用于诊断测试的内部环回功能。该芯片采用10mm x 10mm、68引脚QFN封装，工作温度范围为0°C至+85°C。

应用

4x InfiniBand (4 x 2.5Gbps)

10Gbase-CX4以太网(4 x 3.125Gbps)

10G光纤信道XAUI (4 x 3.1875Gbps)

4x铜缆或背板传输(1Gbps至3.2Gbps)

引脚配置在数据资料的最后给出。

特性

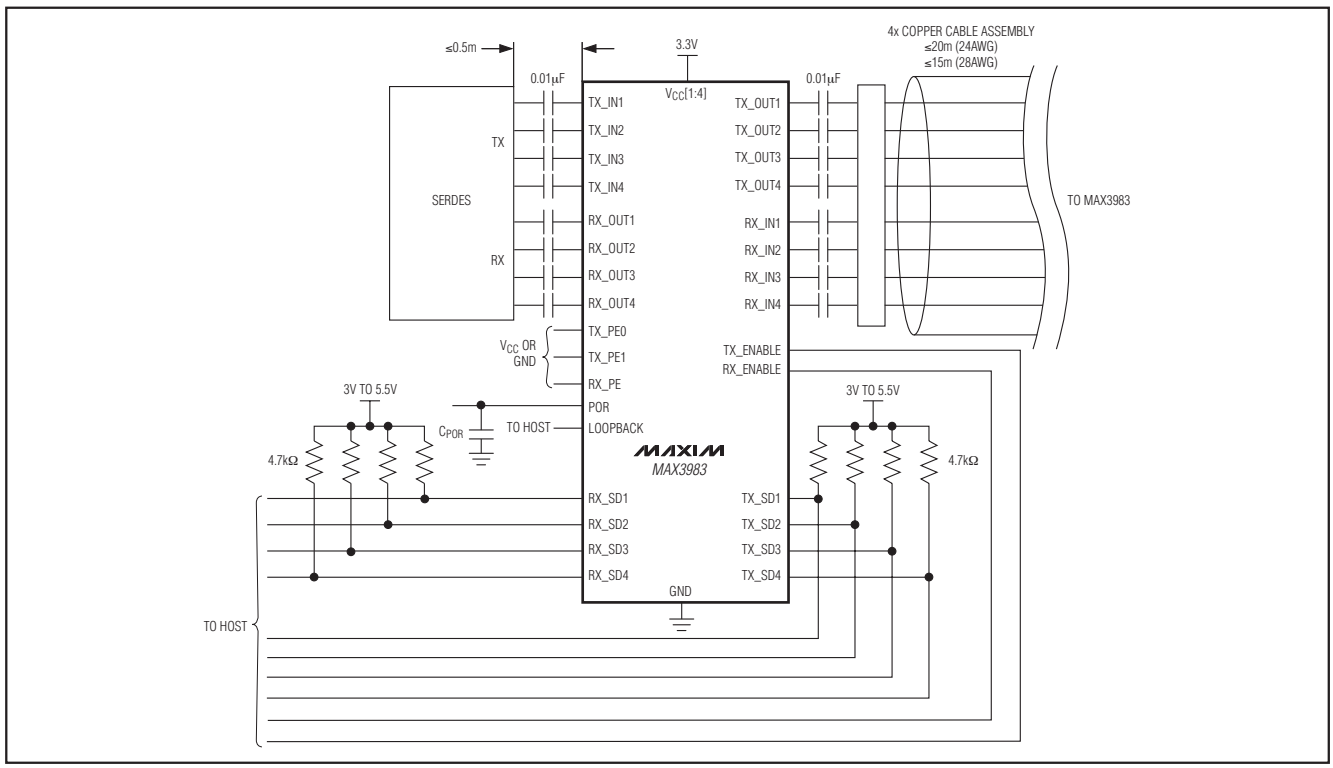
- ♦ 链路特性
  - 24AWG跨距20米，28AWG跨距15米
  - 每个主机允许0.5m的FR4跨距
  - 3.3V电源下总功耗为1.6W
  - 环回功能
- ♦ 电缆驱动器特性
  - 可选的输出预加重
  - FR4输入均衡
  - 每个通道均具有信号检测
  - 可禁止输出
- ♦ 电缆接收器特性
  - 可选的FR4输出预加重
  - 电缆输入均衡
  - 每个通道均具有信号检测
  - 可禁止输出

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3983UGK	0°C to +85°C	68 QFN	G6800-4
MAX3983UGK+	0°C to +85°C	68 QFN	G6800-4

+表示无铅封装。

典型应用电路



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +6.0V
Continuous CML Output Current at
TX_OUT[1:4]±, RX_OUT[1:4]± .....±25mA
Voltage at TX_IN[1:4]±, RX_IN[1:4]±, RX_SD[1:4], TX_SD[1:4], RX_ENABLE, TX_ENABLE, RX_PE, TX_PE[0:1], LOOPBACK, POR (with series resistor ≥4.7kΩ).....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
68-Pin QFN (derate 41.7mW/°C above +85°C).....2.7W
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (T_S) .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		RX_EN = V_{CC}, TX_EN = 0V		360	430	mA
		RX_EN = 0V, TX_EN = V_{CC}		365	430	
		RX_EN = V_{CC}, TX_EN = V_{CC}		495	580	
OPERATING CONDITIONS						
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Noise Tolerance		1MHz ≤ f < 2GHz		40		mV_{P-P}
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data (Note 1)	2.5		3.2	Gbps
CID		Consecutive identical digits (bits)			10	Bits
STATUS OUTPUTS: RX_SD[1:4], TX_SD[1:4]						
Signal-Detect Open-Collector Current Sink		Signal detect asserted	0		25	µA
		Signal detect unasserted V_{OL} ≤ 0.4V with 4.7kΩ pullup resistor	1.0	1.11		mA
		V_{CC} = 0V, pullup supply = 5.5V, external pullup resistor ≥4.7kΩ	0		25	µA
Signal-Detect Response Time		Time from RX_IN[1:4] or TX_IN[1:4] dropping below $85mV_{P-P}$ or rising above $175mV_{P-P}$ to 50% point of signal detect		0.35		µs
Signal-Detect Transition Time		Rise time or fall time (10% to 90%)		200		ns
Power-On Reset Delay		1µF capacitor on POR to GND		6		ms
CONTROL INPUTS: RX_ENABLE, TX_ENABLE, RX_PE, TX_PE0, TX_PE1, LOOPBACK						
Voltage, Logic High	V_{IH}		1.5			V
Voltage, Logic Low	V_{IL}				0.5	V
Current, Logic High	I_{IH}	V_{IH} = V_{CC}	-150		+150	µA
Current, Logic Low	I_{IL}	V_{IL} = 0V	-150		+150	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
TX SECTION (CABLE DRIVER)									
PC Board Input Swing		Measured differentially at the signal source (Note 1)				800		1600	mV_{P-P}
Input Resistance		TX_IN[1:4]+ to TX_IN[1:4]-, differential				85	100	115	Ω
Input Return Loss		100MHz to 2GHz (Note 1)				10	17		dB
Output Swing		TX_ENABLE = high (Notes 1, 2)				1300	1500	1600	mV_{P-P}
		TX_ENABLE = low						30	
Output Resistance		TX_OUT[1:4]+ or TX_OUT[1:4]- to V_{CC}, single ended				42	50	58	Ω
Output Return Loss		100MHz to 2GHz (Note 1)				10	13		dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 1, 3)						80	ps
Random Jitter		(Notes 1, 3)						1.6	ps_{RMS}
Output Preemphasis		See Figure 1	**TX_PE1**	**TX_PE0**					dB
			0	0			3		
			0	1			6		
			1	0			9		
			1	1			12		
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 4, 5)		**Source to TX_IN**	**TX_OUT to Load**	**TX_PE1**	**TX_PE0**				UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 28AWG	0	0		0.10	0.15	
			5m, 28AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 4, 5)		**Source to TX_IN**	**TX_OUT to Load**	**TX_PE1**	**TX_PE0**				UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 28AWG	0	0		0.15	0.20	
			5m, 28AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				
Signal-Detect Assert Level		TX_IN for TX_SD = high (Note 6)				800			mV_{P-P}
Signal-Detect Off		TX_IN for TX_SD = low (Note 6)						200	mV_{P-P}
RX SECTION (CABLE RECEIVER)									
Cable Input Swing		Measured differentially at the signal source (Note 1)				1000		1600	mV_{P-P}
Input Vertical Eye Opening		Measured differentially at the input of the MAX3983 (Note 1)				175		1600	mV_{P-P}
Input Resistance		RX_IN[1:4]+ to RX_IN[1:4]-, differential				85	100	115	Ω
Input Return Loss		100MHz to 2GHz (Note 1)				10	18		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS						MIN	TYP	MAX	UNITS
Output Swing		RX_ENABLE = high (Notes 1, 7)						1100		1500	mV_{P-P}
		RX_ENABLE = low								30	
Output Resistance		RX_OUT[1:4]+ or RX_OUT[1:4]- to V_{CC}, single ended						42	50	58	Ω
Output Return Loss		100MHz to 2GHz (Note 1)						10	15		dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 1, 8)							45	80	ps
Random Jitter		(Notes 1, 8)								1.6	ps_{RMS}
Output Preemphasis		RX_PE = low							3		dB
		RX_PE = high							6		
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 5, 9, 10)		**Source to RX_IN**	**RX_OUT to Load**	**RX_PE**					0.10	0.15	UI_{P-P}
		5m, 28AWG IB Cable Assembly without preemphasis	0in, 6-mil FR4	0							
			20in, 6-mil FR4	1							
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 5, 9, 10)		**Source to RX_IN**	**RX_OUT to Load**	**RX_PE**					0.15	0.20	UI_{P-P}
		5m, 28AWG IB cable assembly without preemphasis	0in, 6-mil FR4	0							
			20in, 6-mil FR4	1							
Signal-Detect Assert Level		RX_IN for RX_SD = high (Note 11)						175			mV_{P-P}
Signal-Detect Off		RX_IN for RX_SD = low (Note 11)								85	mV_{P-P}
END-TO-END JITTER (TX AND RX COMBINED PERFORMANCE)											
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 12, 13, 14)		**Source to TX_IN**	**TX_OUT to RX_IN**	**TX_PE1**	**TX_PE0**	**RX_OUT to Load**	**RX_PE**		0.15	0.20	UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 24AWG	0	0	0in	0				
			15m, 24AWG	1	1	20in	1				
			20m, 24AWG	1	1	20in	1		0.2	0.25	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS						MIN	TYP	MAX	UNITS
		Source to TX_IN	TX_OUT to RX_IN	TX_PE1	TX_PE0	RX_OUT to Load	RX_PE				
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 12, 13, 14)		6-mil FR4 ≤ 20 in	1m, 24AWG	0	0	5in	0		0.20	0.25	UI_{P-P}
			15m, 24AWG	1	1	20in	1				
			20m, 24AWG	1	1	20in	1		0.25	0.3	

Note 1: Guaranteed by design and characterization.

Note 2: Measured with 2in of FR4 through InfiniBand connector with TX_PE1 = TX_PE0 =1.

Note 3: Measured at the chip using 0000011111 or equivalent pattern. TX_PE1 = TX_PE0 = 0 for minimum preemphasis.

Note 4: All channels under test are not transmitting during test. Channel tested with XAUI CJPAT, as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 5: Cables are unequalized, Amphenol Spectra-Strip 24AWG and 28AWG or equivalent equipped with Fujitsu "MicroGiga" connector or equivalent. All other channels are quiet. Residual deterministic jitter is the difference between the source jitter and the output jitter at the load. The deterministic jitter (DJ) at the output of the transmission line must be from media-induced loss and not from clock-source modulation. Depending upon the system environment, better results can be achieved by selecting different preemphasis levels.

Note 6: Tested with a 1GHz sine wave applied at TX_IN under test with less than 5in of FR4.

Note 7: Measured with 3in of FR4 with RX_PE = 1.

Note 8: Measured at the chip using 0000011111 or equivalent pattern. RX_PE = low (minimum). Signal source is $1V_{P-P}$ with 5m, 28AWG InfiniBand cable.

Note 9: All other receive channels are quiet. TX_ENABLE = 0. Channel tested with XAUI CJPAT as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 10: FR4 board material: 6-mil-wide, 100Ω, edge-coupled stripline ($\tan\delta$ = 0.022, 4.0 < ε_R < 4.4).

Note 11: Tested with a 1GHz sine wave applied at RX_IN under test with less than 5in of FR4.

Note 12: Channel tested with XAUI CJPAT as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 13: Cables are unequalized, Amphenol Spectra-Strip 24AWG or equivalent equipped with Fujitsu "MicroGiga" connector or equivalent. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter at point B in Figure 2. The deterministic jitter (DJ) at the output of the transmission line must be from media-induced loss and not from clock-source modulation. Depending upon the system environment, better results can be achieved by selecting different preemphasis levels.

Note 14: Valid with pattern generator deterministic jitter as high as $0.17UI_{P-P}$.

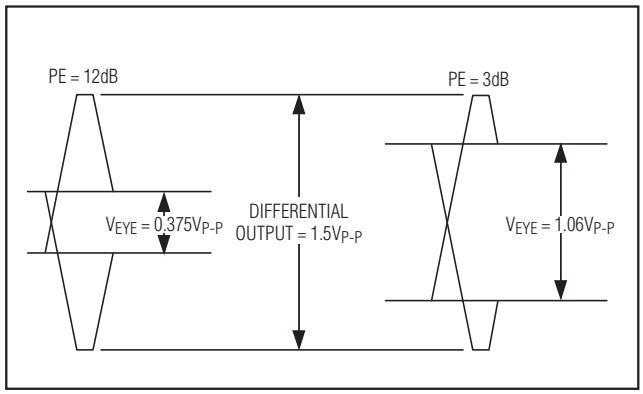


图1. 以dB表示的TX预加重

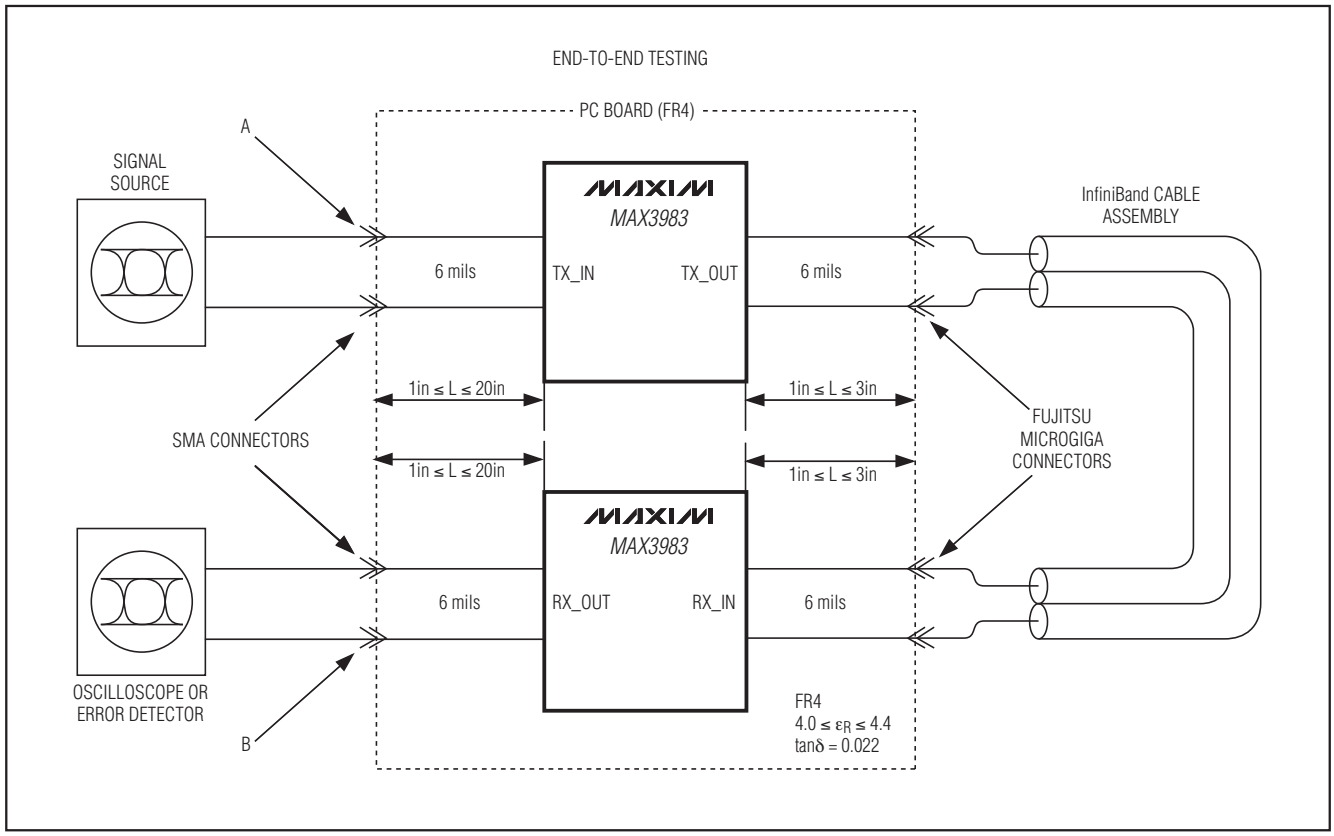
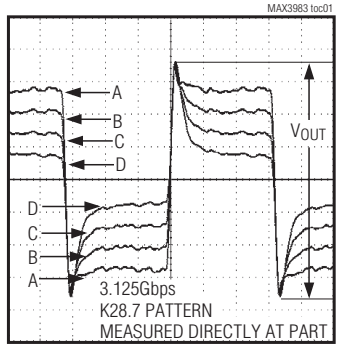


图2. 端-端测试装置。A、B标注点为交流参数测试的参考。

典型工作特性

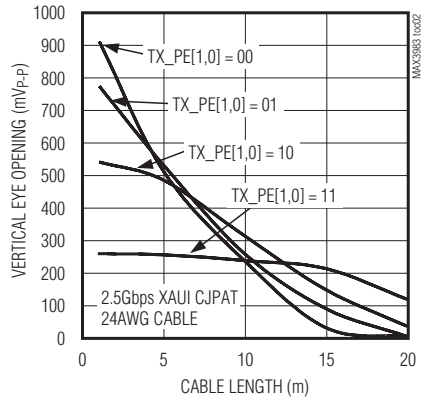
(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

TRANSIENT REPSONSE

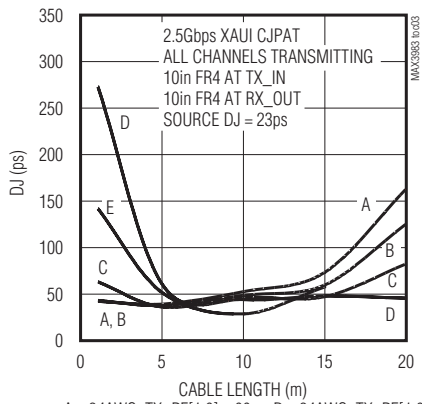


A = 3dB, TX_PE = 00
B = 6dB, TX_PE = 01
C = 9dB, TX_PE = 10
D = 12dB, TX_PE = 11

VERTICAL EYE OPENING vs. CABLE LENGTH

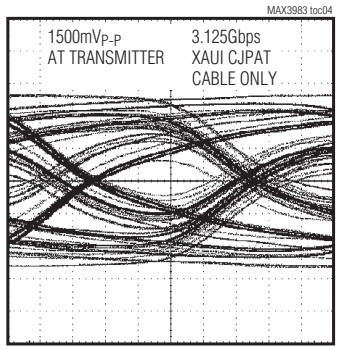


END-TO-END DETERMINISTIC JITTER vs. CABLE LENGTH



A = 24AWG, TX_PE[1,0] = 00
B = 24AWG, TX_PE[1,0] = 01
C = 24AWG, TX_PE[1,0] = 10
D = 24AWG, TX_PE[1,0] = 11
E = 28AWG, TX_PE[1,0] = 11

10m 24AWG UNEQUALIZED CABLE ASSEMBLY OUTPUT WITHOUT MAX3983



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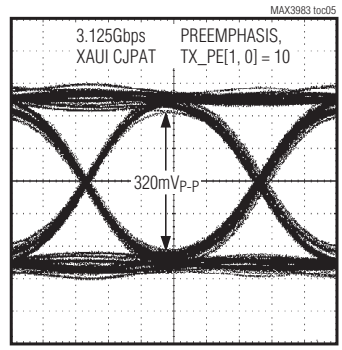
10m 24AWG UNEQUALIZED CABLE ASSEMBLY OUTPUT WITH MAX3983 PREEMPHASIS



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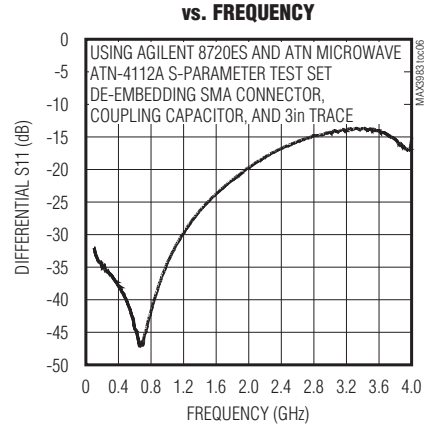
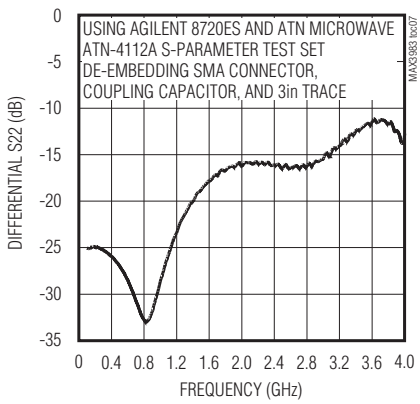
TX_IN INPUT RETURN LOSS vs. FREQUENCY



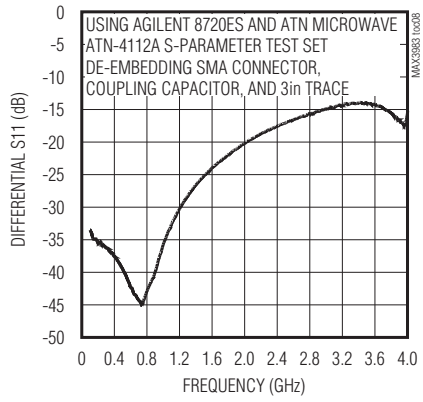
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

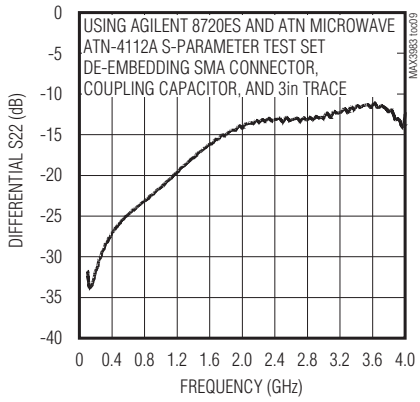
TX_OUT OUTPUT RETURN LOSS vs. FREQUENCY



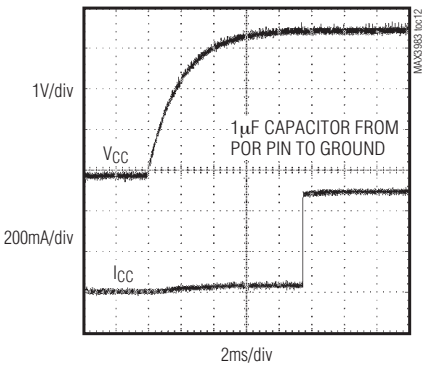
RX_IN INPUT RETURN LOSS vs. FREQUENCY



RX_OUT OUTPUT RETURN LOSS vs. FREQUENCY



POWER-ON RESET DELAY WITH SUPPLY RAMP



引脚说明

引脚	名称	功能
1, 2, 16, 17	TX_SD1至TX_SD4	PCB接收器信号检测，TTL输出。该输出是集电极开路TTL，因此需要与V_{CC}之间外接一个4.7kΩ至10kΩ的上拉电阻。当输入信号电平无效时这些输出吸收电流。
3, 15	V_{CC}1	TX输入电源，为+3.3V。
4, 7, 10, 13	TX_IN1-至TX_IN4-	PCB接收器数据输入负端，CML。这些输入在内部用100Ω差分端接至对应的TX_IN+。
5, 8, 11, 14	TX_IN1+至TX_IN4+	PCB接收器数据输入正端，CML。这些输入在内部用100Ω差分端接至对应的TX_IN-。
6, 9, 12, 40, 43, 46	GND	电路地。
18	TX_ENABLE	电缆发送器使能输入，含内部40kΩ上拉的LVTTL。该引脚使能所有四路电缆发送器输出TX_OUT[1:4]。LVTTL为低时，差分输出低于30mV_{P-P}。置高或开路时正常工作。
19	N.C.	无连接。不要连接此引脚。
20, 23, 26, 29, 32	V_{CC}2	用于TX输出的电源连接。接至+3.3V。
21, 24, 27, 30	TX_OUT1+至TX_OUT4+	电缆发送器数据输出正端，CML。这些输出通过50Ω端接至V_{CC}2。
22, 25, 28, 31	TX_OUT1-至TX_OUT4-	电缆发送器数据输出负端，CML。这些输出通过50Ω端接至V_{CC}2。
33	TX_PE0	电缆发送器预加重控制输入，含内部40kΩ上拉的LVTTL。2位预加重控制字的最低有效位。置高或开路触发该位。
34	TX_PE1	电缆发送器预加重控制输入，含内部40kΩ上拉的LVTTL。2位预加重控制字的最高有效位。置高或开路触发该位。
35, 36, 50, 51	RX_SD4至RX_SD1	电缆接收器信号检测，TTL输出。该输出为集电极开路TTL，因此需要与V_{CC}之间外接一个4.7kΩ至10kΩ的上拉电阻。当输入信号电平无效时这些输出引脚吸收电流。
37, 49	V_{CC}3	RX输入电源，接至+3.3V。
38, 41, 44, 47	RX_IN4-至RX_IN1-	电缆接收器数据输入负端，CML。这些输入在内部用100Ω差分端接至对应的RX_IN+。
39, 42, 45, 48	RX_IN4+至RX_IN1+	电缆接收器数据输入正端，CML。这些输入在内部用100Ω差分端接至对应的RX_IN-。
52	RX_ENABLE	PCB发送器使能输入，含内部40kΩ上拉的LVTTL。该引脚使能所有四路PCB发送器输出RX_OUT[1:4]。为低时，差分输出低于30mV_{P-P}。置高或开路时正常工作。
53	POR	上电复位连接引脚。外接一个0.1µF ≤ C_{POR} ≤ 10µF的电容到地。参见*详细说明*。
54, 57, 60, 63, 66	V_{CC}4	RX输出电源，接至+3.3V。

引脚说明(续)

引脚	名称	功能
55, 58, 61, 64	RX_OUT4+至 RX_OUT1+	PCB发送器数据输出正端，CML。这些输出通过50Ω端接至$V_{CC}4$。
56, 59, 62, 65	RX_OUT4-至 RX_OUT1-	PCB发送器数据输出负端，CML。这些输出通过50Ω端接至$V_{CC}4$。
67	RX_PE	PCB发送器预加重控制输入，含内部40kΩ上拉的LVTTL。置高或开路时使能。
68	LOOPBACK	环回使能输入，含内部40kΩ上拉的LVTTL。置低为正常工作。置高或开路时TX_IN内部连接至RX_OUT。环回使能后TX_OUT继续发送数据。
EP	裸焊盘	裸焊盘。信号和电源地。为获得最佳的高频和导热性能，必须将底盘焊接在电路板地上。

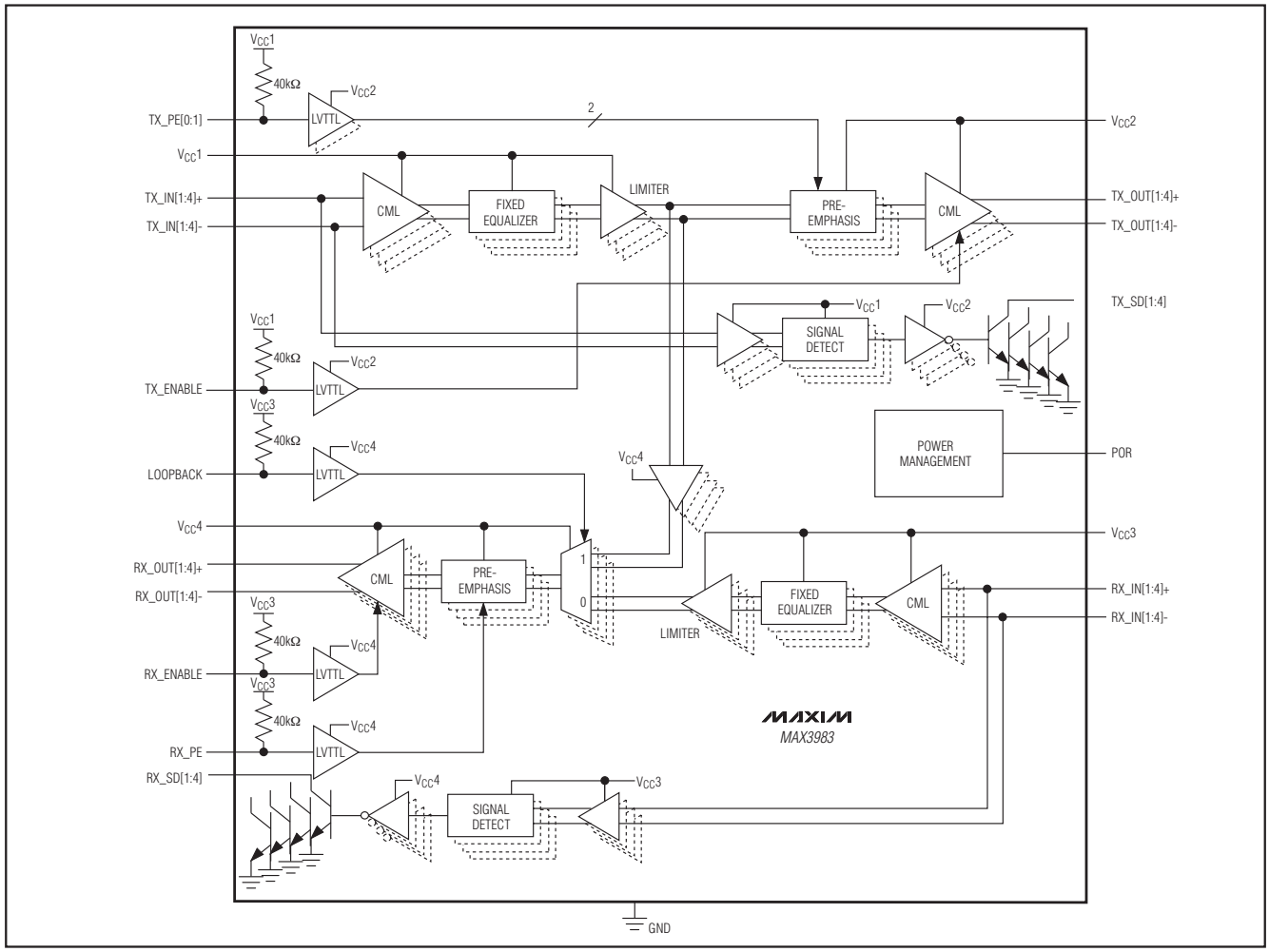


图3. 功能框图

详细说明

MAX3983包含一组PCB接收器和电缆驱动器单元(TX)，以及一组电缆接收器和PCB驱动器单元(RX)。每个接收器都具有均衡和信号检测功能，每个发送器都包含预加重。MAX3983具有独立的TX输出和RX输出使能控制，还提供用于诊断测试的环回功能。

PCB接收器和电缆驱动器 (TX_IN和TX_OUT)

数据由主机馈入MAX3983，经过CML输入级进入固定均衡级。PCB接收器内的固定均衡器可以补偿长达20英寸的FR4 PCB损耗。电缆驱动器采用四态预加重电路补偿长达20米的24AWG、100Ω平衡电缆损耗。表1给出了几种不同预加重表达方式间的简单转换。MAX3983的残余抖动与最高至0.17UI_{P-P}的源抖动无关。

电缆接收器和PCB驱动器 (RX_IN和RX_OUT)

每个RX输入端的固定均衡器提供将近6dB的均衡，可补偿最长为5米的28AWG、100Ω平衡电缆。PCB驱动器包含有两态预加重，可补偿最长达20英寸的FR4板材。

信号检测输出

全部八个数据输入端都集成了信号检测(SD)功能。SD输出应通过外部上拉电阻连接至3.0V至5.5V的电源电压。信号检测器的输出在完全上电之前是无效的。信号检测器的响应时间典型值为0.35µs。

在RX单元，当RX_IN信号幅度大于175mV_{P-P}时SD输出触发为高。当RX_IN信号幅度降低到85mV_{P-P}以下时RX_SD恢复为低。

在TX单元，当TX_IN信号幅度大于800mV_{P-P}时SD输出触发为高。当TX_IN信号幅度降低到200mV_{P-P}以下时TX_SD恢复为低。

TX和RX使能

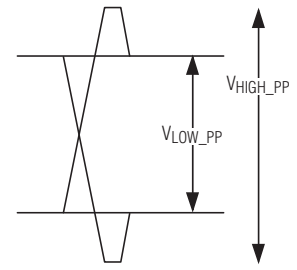
TX_ENABLE和RX_ENABLE引脚分别使能TX和RX。典型的使能时间是15ns，典型禁止时间是25ns。可将使能输入与信号检测输出相连实现对输入信号的自动检测(参见*自动检测*部分)。

上电复位

为限制浪涌电流，MAX3983内部集成了上电复位电路。在POR引脚和地之间连接一只0.1µF ≤ C_{POR} ≤ 10µF的电容。当C_{POR} = 1µF时，上电延迟时间为6ms (典型值)。

表1. 预加重转换表

RATIO	α	10Gbase-CX4	IN dB	
$\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}$	$\frac{V_{HIGH\_PP} - V_{LOW\_PP}}{V_{HIGH\_PP} + V_{LOW\_PP}}$	$1 - \frac{V_{LOW\_PP}}{V_{HIGH\_PP}}$	$20\left[\log\left(\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}\right)\right]$	
1.41	0.17	0.29	3	
2.00	0.33	0.50	6	
2.82	0.48	0.65	9	
4.00	0.60	0.75	12	



应用信息

信号检测输出漏电流的考虑

若需要将四路RX或TX信号检测输出连在一起形成一路信号检测输出时，则需要考虑输出级的漏电流。当被触发时，每路SD输出最多可吸收25µA电流，因此四路连接在一起时最大电流为100µA。在选择上拉至V_{PULLUP}的上拉电阻值时，应该保证该漏电流不会使输出电压降低到下一级电路的门限以下。例如，若将信号检测输出脚接在一起连接到一个逻辑高门限为1.5V的电路时，上拉电阻的取值应该保证$V_{PULLUP} - I_{LEAKAGE} \times R_{PULLUP} > 1.5V$。在此情况下，若$V_{PULLUP} = 3.0V$，则$R_{PULLUP}$应该小于15kΩ。

自动检测

MAX3983能自动检测输入信号并使能相应的输出。RX侧的自动检测功能是将RX_SD[1:4]通过一只电阻上拉后(阻值4.7kΩ至10kΩ，上拉至V_{CC})与RX_ENABLE相连实现的。对于TX侧，可将TX_SD[1:4]通过一只电阻上拉后(阻值4.7kΩ至10kΩ，上拉至V_{CC})与TX_ENABLE (图4)相连实现。若在所有通道上检测到信号，则SD置高，并使相应的ENABLE置高。由于会放大噪声并出现不希望的输出信号，建议不要使MAX3983的输入脚处于未连接(浮空)状态。建议使用自动检测以消除噪声放大或可能的振荡。当使用自动检测时，链路长度取决于接收信号的强度。若未使用自动检测结构，则有可能达到更长的距离。

使用环回和自动检测

若将MAX3983设置成自动检测，则RX_ENABLE由RX_SD[1:4]输出来控制。由于环回要求将RX_ENABLE置高，可用一个简单的或门使能RX输出，当RX_SD[1:4]为高或LOOPBACK为高都可使能RX (图5)。

InfiniBand和10Gbase-CX4对于转换时间的规定

InfiniBand规定了100ps的最小转换时间(20%至80%)，CX4规定了60ps的最小转换时间。两者都是针对电缆接口的连接器位置规定的。MAX3983的输出转换时间是45ps(典型值)，因此需要仔细考虑延长该时间。3英寸左右长、4mil宽的FR4引线足以将转换时间延长至60ps。对于100ps转换时间，可增加长度或在MAX3983的输出脚并联一个1.5pF电容。若应用中需要使用InfiniBand或者CX4类型的连接器，电路板不要用高速电介质的板材。使用此种材料时，MAX3983的快速边沿会在InfiniBand和CX4电缆组件中产生过大的串扰。

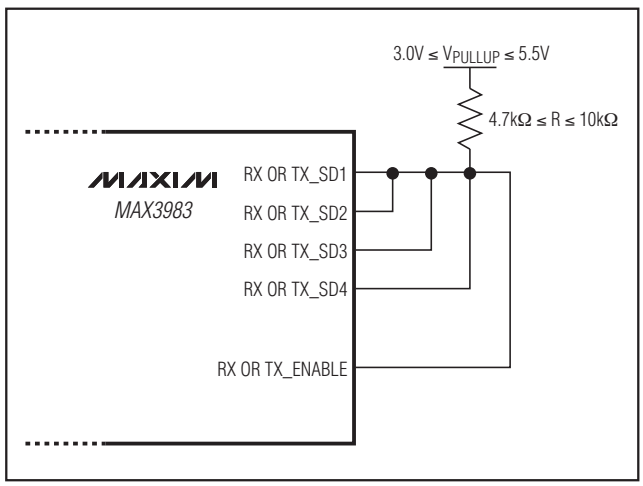


图4. 使用相应的信号检测输出和使能输入实现自动检测

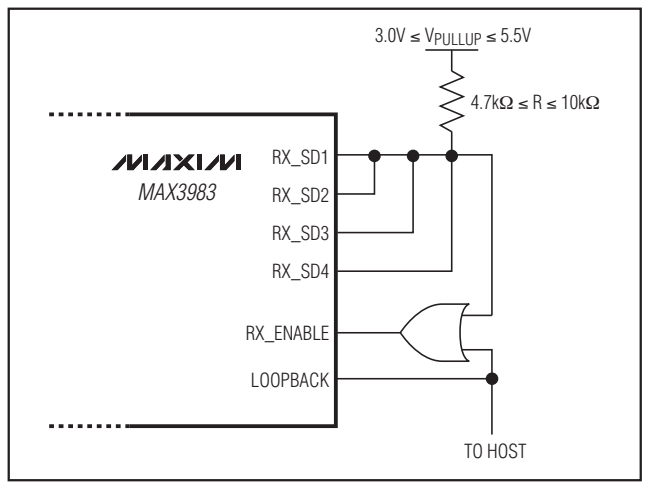


图5. 环回和自动检测模式

串扰

对于InfiniBand和10Gbase-CX4应用，必须了解电缆组件的近端串扰特性。10Gbase-CX4已规定了一个或多个侵入信号时，近端串扰(NEXT)在整个频段的上限。InfiniBand只是相对于发送器输出，规定了一个在时域测得的百分比。无论采用何种方法规定，NEXT对于链路性能来讲都是一项关键因素。当使用较大量的预加重时，接收眼图高度会更小，更容易发生串扰。在需要较高的发送预加重的情况下，NEXT在1GHz至3GHz频段应低于-30dB。需要注意的是，满足10Gbase-CX4 NEXT和MDNEXT要求的电缆应该具有足够的隔离度。

布局考虑

电路板布局和设计会显著影响MAX3983的性能。数据信号通道应采用优良的高频设计技术，尽量减小接地电感，并使用控制阻抗的传输线。电源去耦应尽可能地靠近V_{CC}引脚。应该有足够的电源滤波。所有V_{CC}应连接到电源层。注意隔离输入与输出信号以免串扰。均衡器的性能在损耗环境中最优。为得到最佳性能，应使用电介质损耗约为0.02的板材和4mil线宽的传输线。也可使用损耗小于0.01的高速板材，但需要特别注意降低电缆组件的近端串扰。

裸焊盘封装

带裸焊盘的68引脚QFN封装为IC提供了一个热阻非常低的散热通道。这个底盘是MAX3983的电气地，必须焊接在电路板上以获得良好的热、电性能。有关裸露底盘封装的更多信息，请参考Maxim应用笔记HFAN-08.1：*Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

接口电路

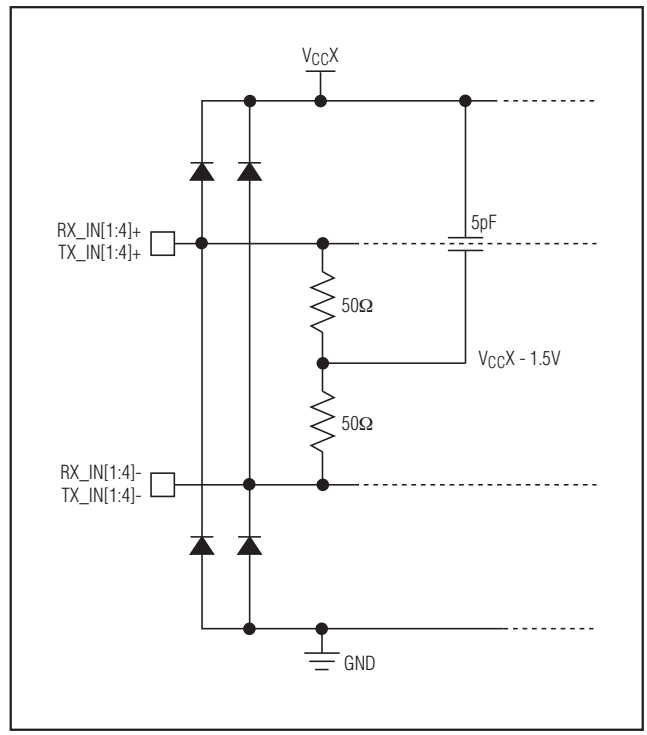


图6. RX_IN和TX_IN等效输入结构

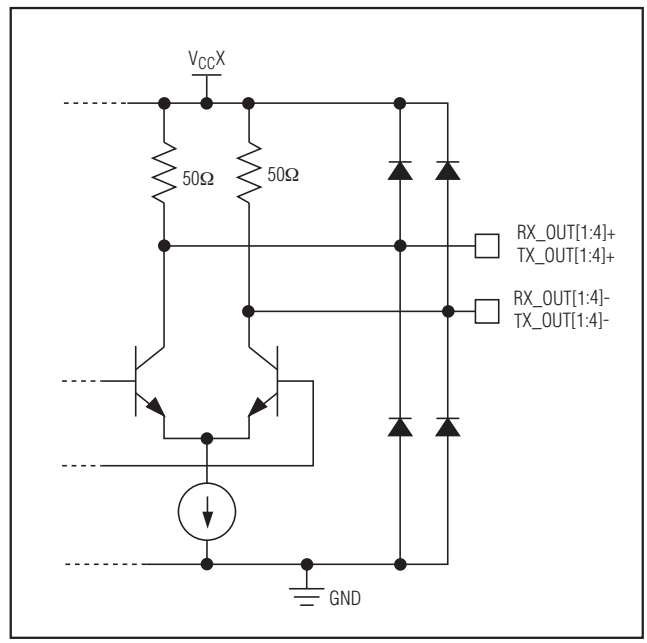
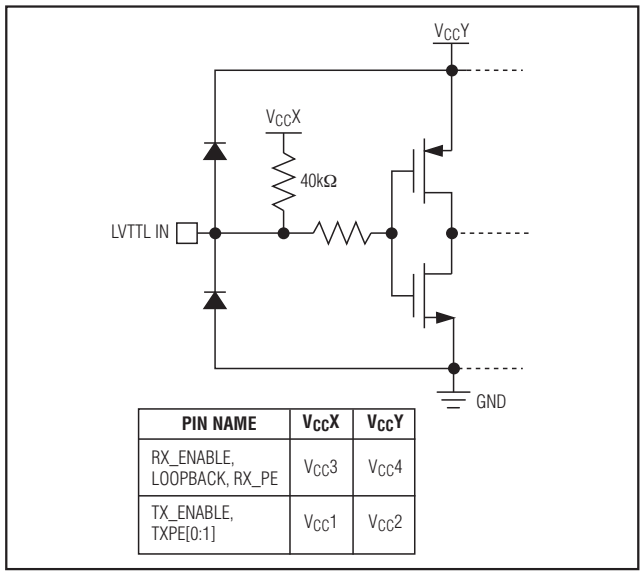


图7. RX_OUT和TX_OUT等效输出结构

四通道铜缆信号调理器



PIN NAME	VCCX	VCCY
RX_ENABLE, LOOPBACK, RX_PE	VCC3	VCC4
TX_ENABLE, TXPE[0:1]	VCC1	VCC2

图8. LVTTL等效输入结构

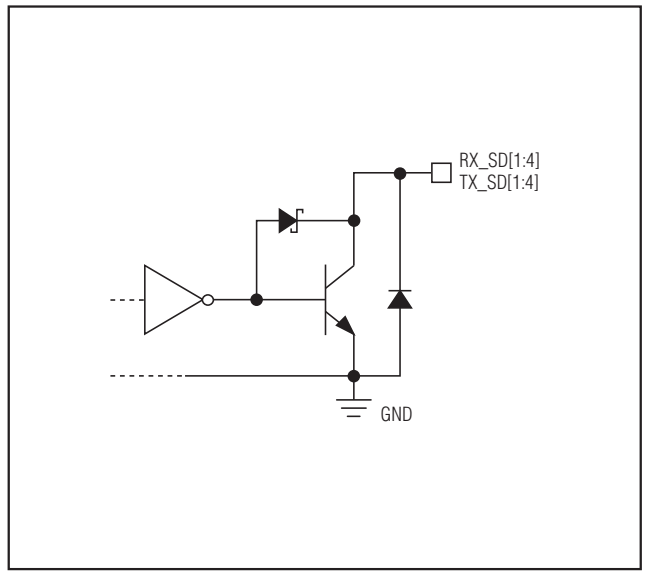
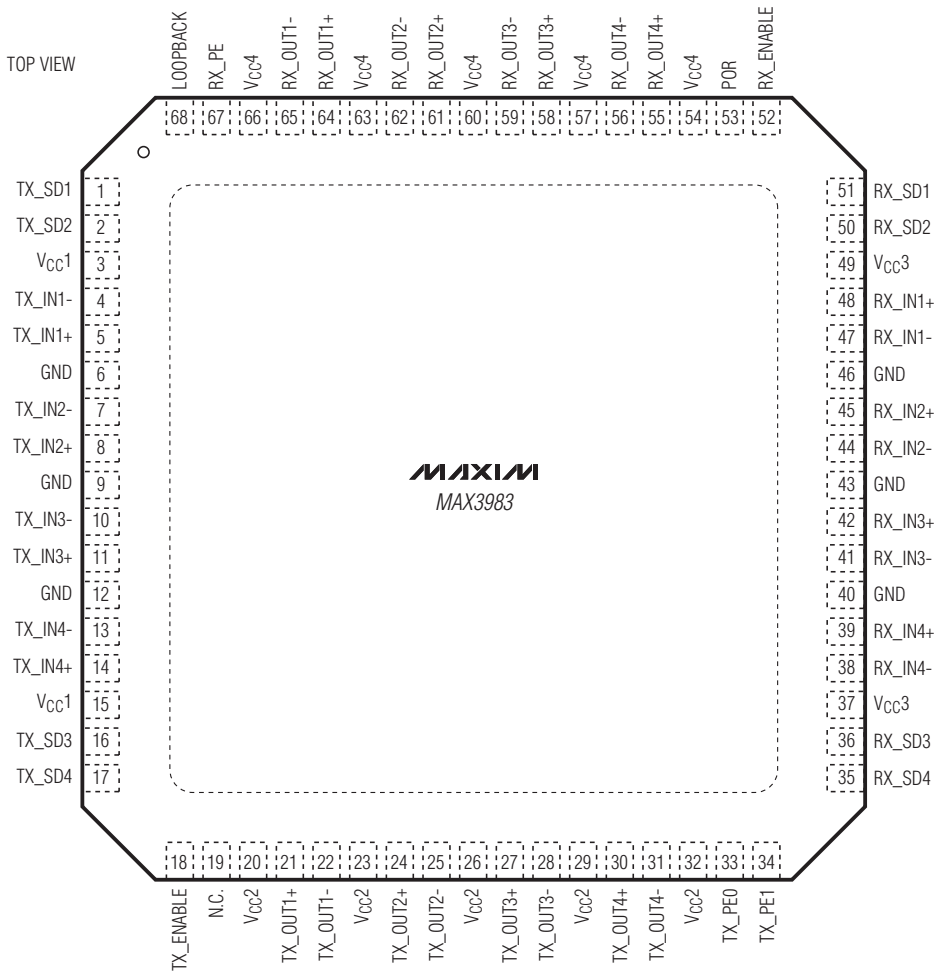


图9. 信号检测等效输出结构

引脚配置



68 QFN*

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION OF THE MAX3983.

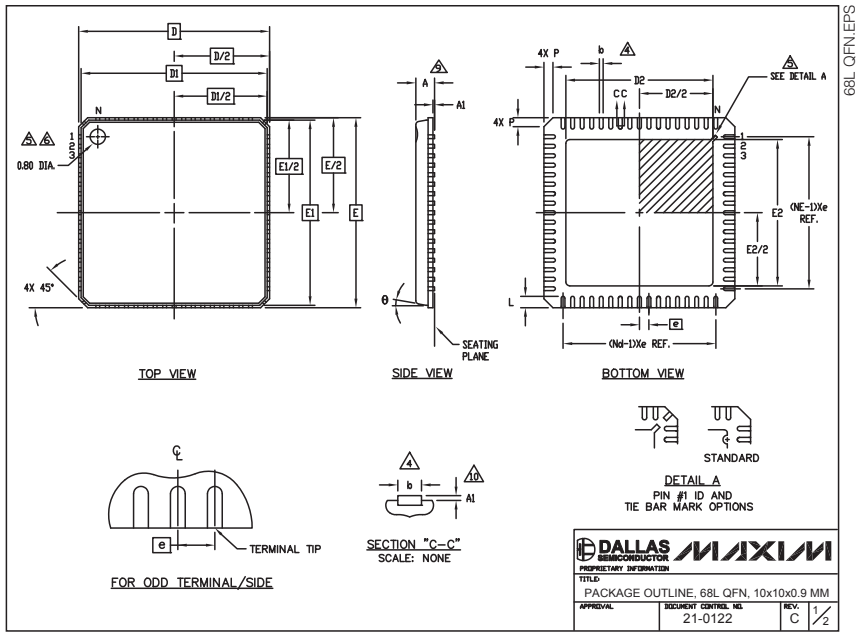
芯片信息

TRANSISTOR COUNT: 7493

PROCESS: SiGe Bipolar

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**.)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR
PROPRIETARY INFORMATION
MAXIM
TITLE:
PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0122
REV.
C
1/2

修订历史

Rev 0； 7/03： 首次发布数据资料。

Rev 1； 2/07： 在定购信息表中增加无铅封装(第1页)。

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