19-0406; Rev 2; 2/08

可提供评估板

1Gbps至12.5Gbps 无源均衡器，用于背板和电缆数据传输

MAX3787

概述

MAX3787为1Gbps至12.5Gbps均衡网络，用于补偿FR4和电缆的传输损耗。该均衡网络全部由无源器件构成，其性能在8b/10b或扰码信号时仍能保持良好效果。器件采用小尺寸1.5mm x 1.5mm晶片级封装(UCSP™)，可沿着传输介质放置在任何位置，提高了高速互连设计中的抖动裕量。芯片面积相当于两个0603器件，MAX3787可简单灵活地进行布线。

数据速率为8.5Gbps时，MAX3787可提供18英寸的FR4传输距离或7米的电缆传输距离。速率为12.5Gbps时，MAX3787可提供12英寸FR4传输距离和3米的电缆传输距离。输入、输出差分阻抗为100Ω。MAX3787无需电源供电，工作温度范围为-40°C至+125°C。

应用

背板互连补偿

电缆互连补偿

芯片间链路拓展

以太网与光纤通道模块

延长机架使用期限

UCSP是Maxim Integrated Products, Inc.的商标。

特性

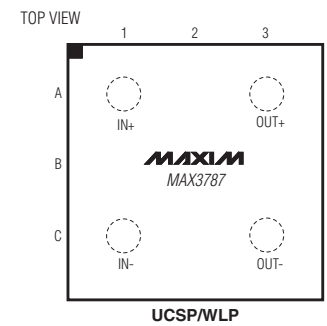
- ♦ 无需电源供电
- ♦ 1.5mm x 1.5mm微型晶片级封装
- ♦ 无源均衡降低了ISI
- ♦ 工作速率为1Gbps至12.5Gbps
- ♦ 可延长电路板连接
- ♦ 可延长电缆连接
- ♦ 与编码方式无关，8b/10b或扰码

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3787ABL	-40°C to +125°C	4 UCSP	B9-7
MAX3787AWL+	-40°C to +125°C	4 WLP	W91B1+3

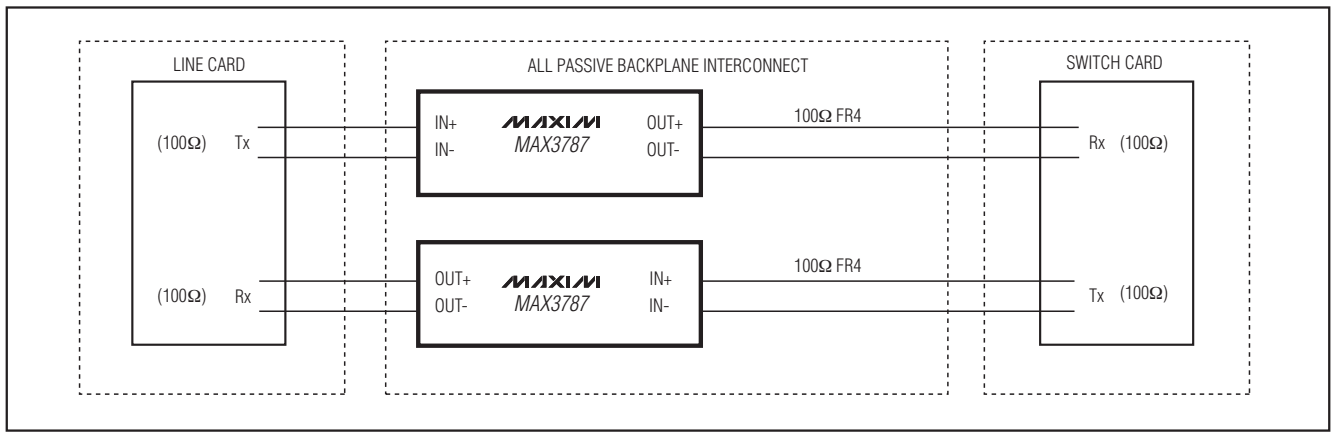
+表示无铅封装。

引脚配置



UCSP/WLP

典型应用电路



典型应用电路(续)在数据资料的最后给出。

ABSOLUTE MAXIMUM RATINGS

Voltage between (IN+ and OUT+) or (IN- and OUT-).....+2V
Voltage between (IN+ and IN-) or (OUT+ and OUT-).....+4V
Voltage between (IN+ and OUT-) or (IN- and OUT+).....+4V

Continuous Power Dissipation (T_A = +70°C)
4-Bump UCSP (derate 3.0mW/°C above +70°C).....238mW
Operating Junction Temperature.....+150°C
Storage Ambient Temperature Range .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A		-40	+25	+125	°C
Bit Rate		NRZ data	1		12.5	Gbps
CID Tolerance		Consecutive identical digits			100	Bits

ELECTRICAL CHARACTERISTICS

(Specifications guaranteed over specified operating conditions. Typical values measured at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current				0.0		mA
Input Swing		Measured differentially at point A in Figure 1			3600	mV_{P-P}
Compensation		5GHz relative to 100MHz		6		dB
Input Impedance		Differential, Z_{LOAD} = 100Ω		100		Ω
Output Impedance		Differential, Z_{SOURCE} = 100Ω		100		Ω
Through Response		Relative to ideal load, see Figure 2 for setup		See Figure 3 for limits		
Input Return Loss		100MHz to 6GHz		15		dB
Output Return Loss		100MHz to 6GHz		15		dB
Resistance IN+ to IN- and OUT+ to OUT-		No load, high impedance on all ports	112		152	Ω
Resistance IN+ to OUT+ and IN- to OUT-		No load, high impedance on all ports	32		44	Ω
Resistance IN+ to OUT- and IN- to OUT+		No load, high impedance on all ports	112		152	Ω
DC Gain (OUT/IN)		Z_{LOAD} = 100Ω		0.5		
Residual Deterministic Jitter (Table 1, Notes 1, 2)		3.125Gbps and 6.25Gbps, 18in of 6mil microstrip FR4		0.05		UI
		8.5Gbps, 10.0Gbps, and 12.5Gbps, 18in of 6mil microstrip FR4		0.10		

Note 1: Signal applied differentially at point A as shown in Figure 1. The deterministic jitter at point B is from media-induced loss, not from clock-source modulation. Deterministic jitter is measured at the 50% vertical level of the signal at point C.

Note 2: Difference in deterministic jitter between reference points A and C in Figure 1. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 27 PRBS, 100 ones, 0, 1, 0, 1.

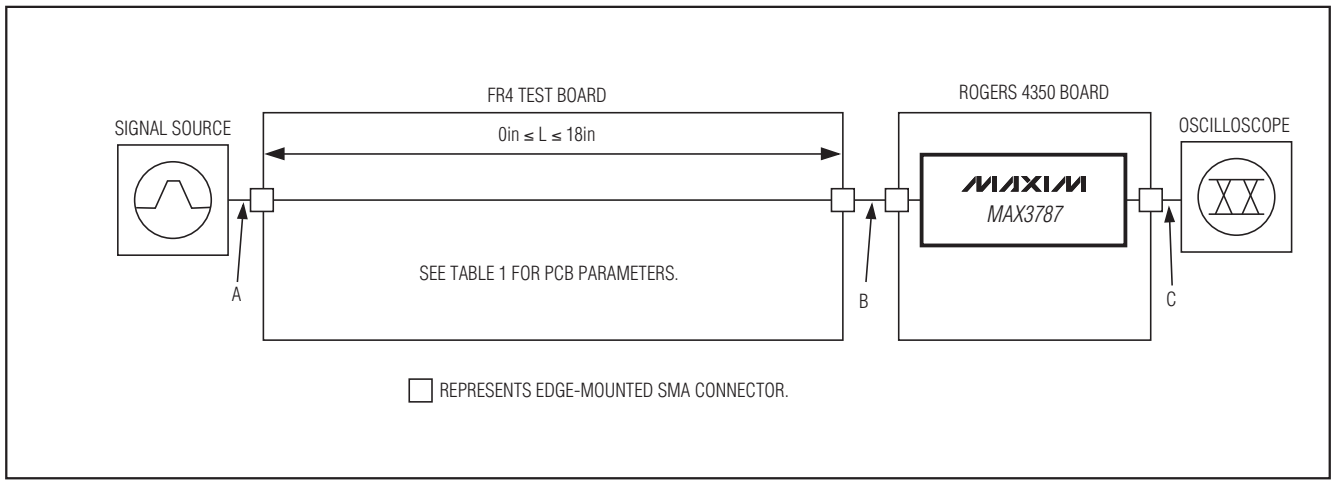


图1. 残余确定性抖动测试电路

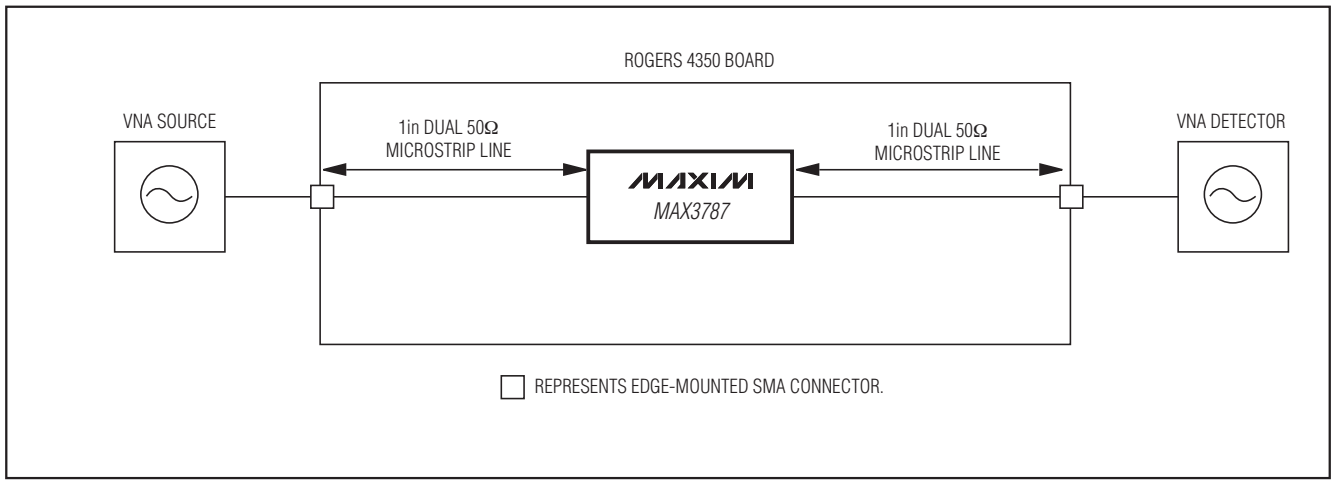


图2. 采用矢量网络分析仪(VNA)测试频率响应

FREQUENCY	MIN (dB)	TYP (dB)	MAX (dB)
100MHz	-8.2	-7.4	-6.8
200MHz	-7.9	-7.0	-6.4
300MHz	-7.5	-6.6	-6.0
500MHz	-6.8	-6.0	-5.3
1.0GHz	-5.5	-4.8	-4.2
2.0GHz	-4.2	-3.2	-2.5
3.0GHz	-3.1	-2.2	-1.5
4.0GHz	-2.3	-1.5	-0.8
5.0GHz	-2.1	-1.3	-0.5
5.5GHz	-2.4	-1.6	-0.6
6.0GHz	-2.9	-2.1	-1.1
6.5GHz	—	-2.6	—
7.0GHz	—	-3.1	—
7.5GHz	—	-3.6	—
8.0GHz	—	-4.1	—
8.5GHz	—	-4.7	—
9.0GHz	—	-5.5	—
9.5GHz	—	-7.0	—
10.0GHz	—	-9.0	—

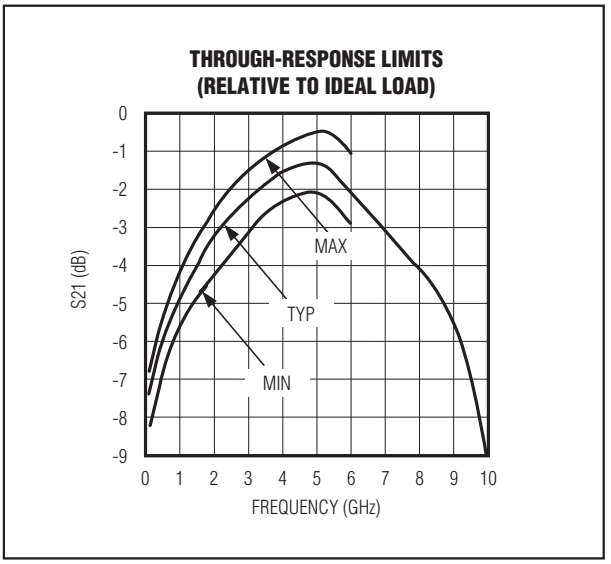


图3. 直通响应限制

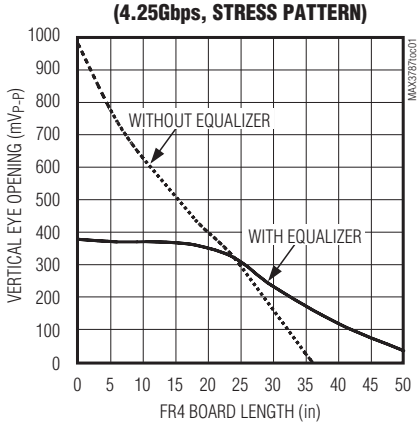
表1. PCB参数(FR4电路板)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmission Line	Edge-coupled microstrip line		6		mil
Relative Permittivity at 1GHz	FR4 or similar		4.0		—
Loss Tangent	FR4 or similar		0.02		—
Metal Thickness	1oz copper		1.4		mil
Impedance	Differential	90	100	110	Ω

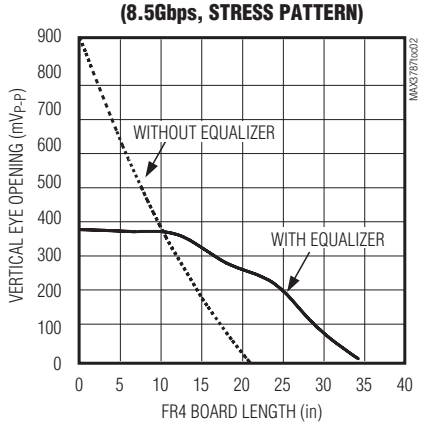
典型工作特性

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan®. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip® Skewclear® 100Ω 24AWG.)

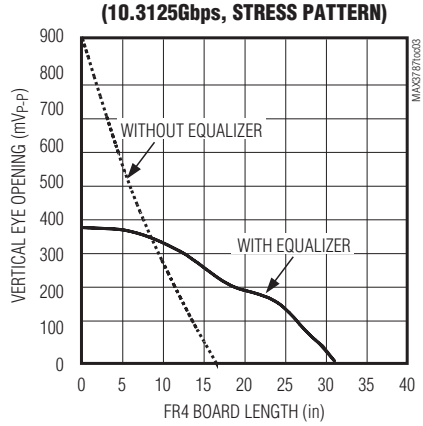
VERTICAL EYE OPENING vs. LENGTH (4.25Gbps, STRESS PATTERN)



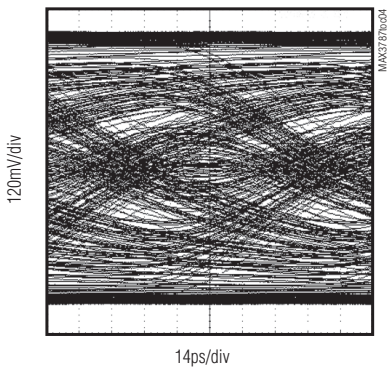
VERTICAL EYE OPENING vs. LENGTH (8.5Gbps, STRESS PATTERN)



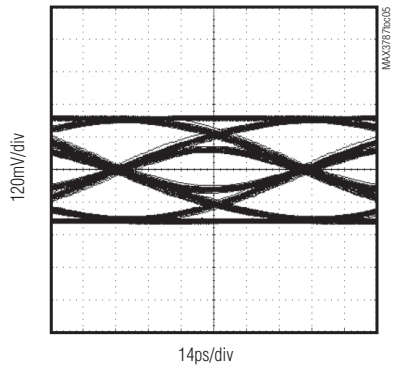
VERTICAL EYE OPENING vs. LENGTH (10.3125Gbps, STRESS PATTERN)



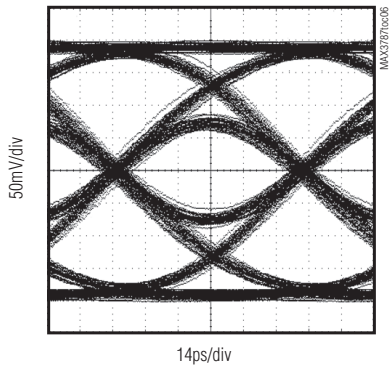
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



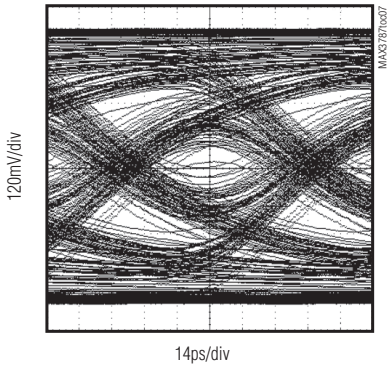
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 12.5Gbps, STRESS PATTERN)



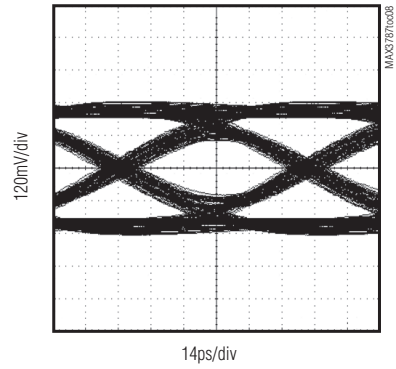
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 12.5Gbps, STRESS PATTERN)



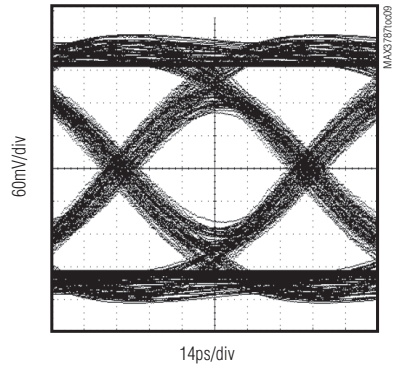
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 12.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 12.5Gbps, STRESS PATTERN)



FrameScan是Tektronix的注册商标。

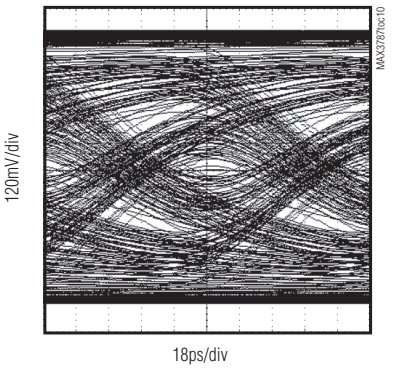
Spectra-Strip和Skewclear是Amphenol的注册商标。

1Gbps至12.5Gbps
无源均衡器，用于背板和电缆数据传输

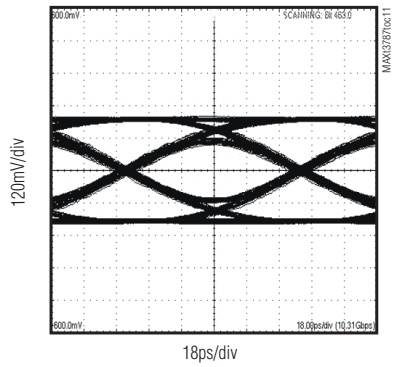
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

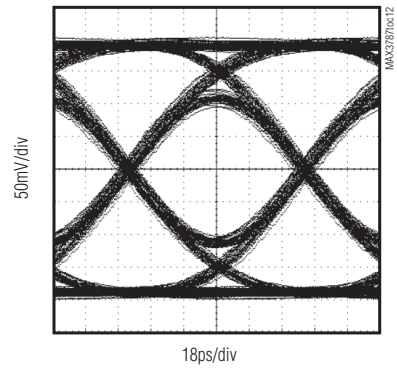
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



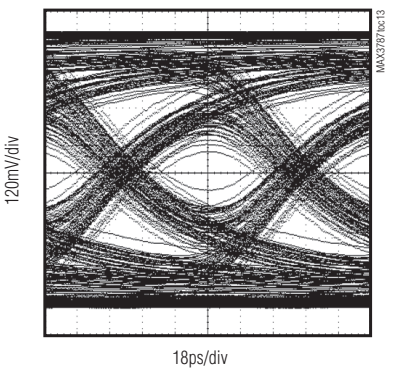
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 10.3125Gbps, STRESS PATTERN)



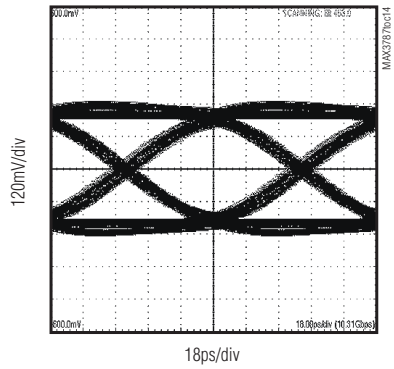
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 10.3125Gbps, STRESS PATTERN)



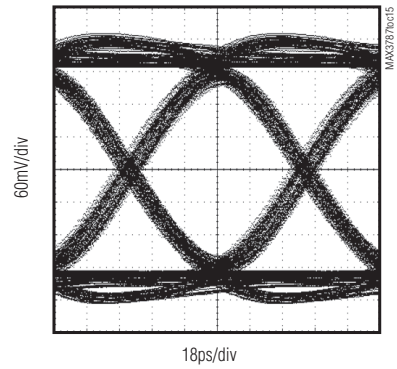
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



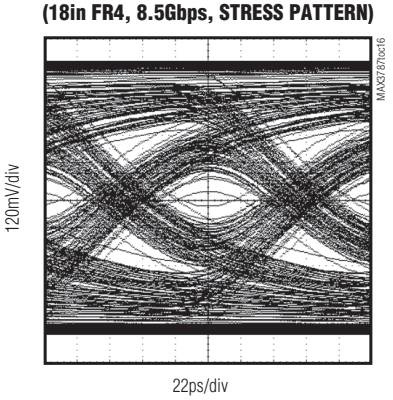
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 10.3125Gbps, STRESS PATTERN)



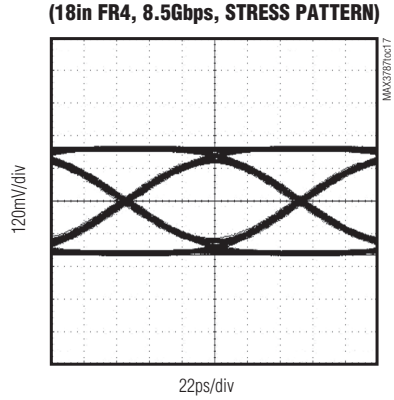
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 10.3125Gbps, STRESS PATTERN)



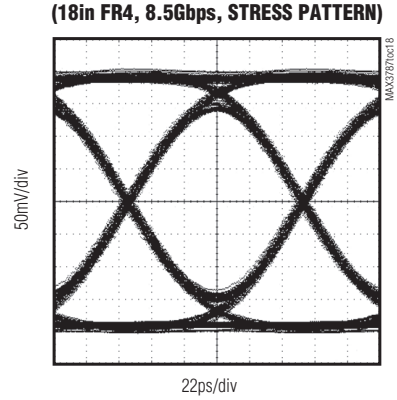
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 8.5Gbps, STRESS PATTERN)



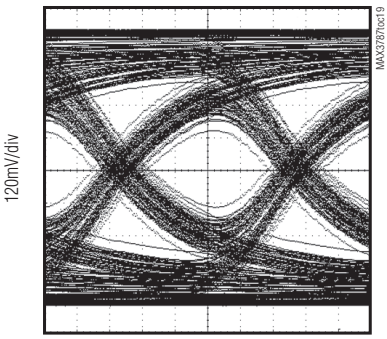
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 8.5Gbps, STRESS PATTERN)



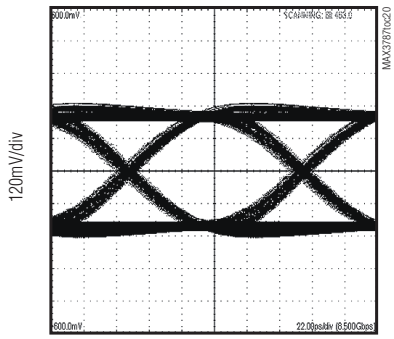
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

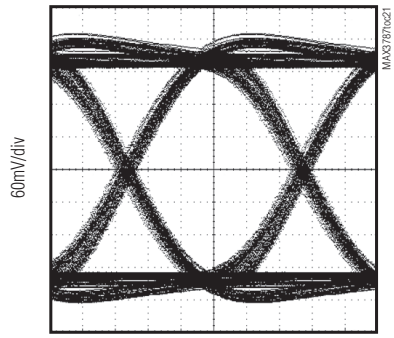
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



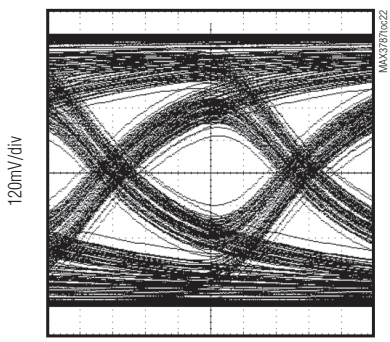
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 8.5Gbps, STRESS PATTERN)



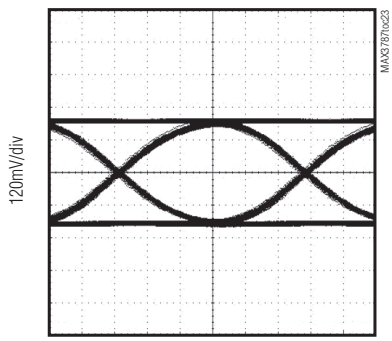
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 8.5Gbps, STRESS PATTERN)



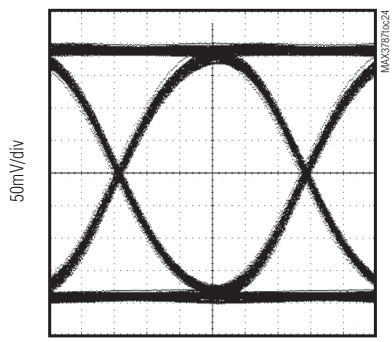
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



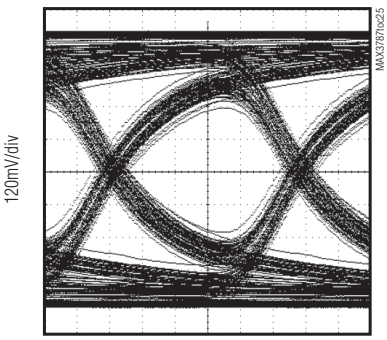
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 6.25Gbps, STRESS PATTERN)



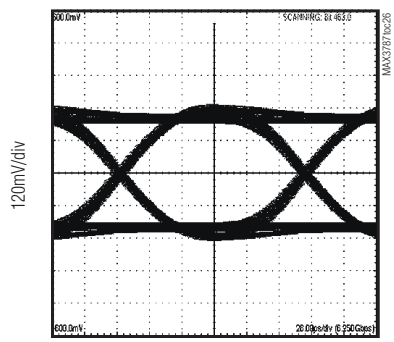
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 6.25Gbps, STRESS PATTERN)



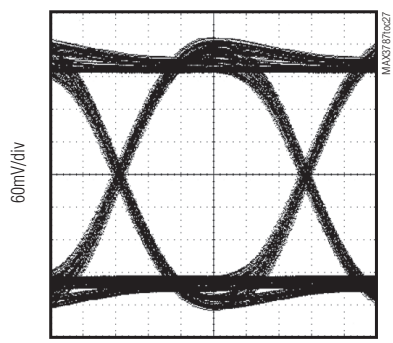
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 6.25Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 6.25Gbps, STRESS PATTERN)

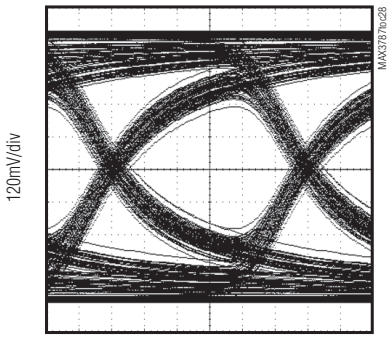


1Gbps至12.5Gbps
无源均衡器，用于背板和电缆数据传输

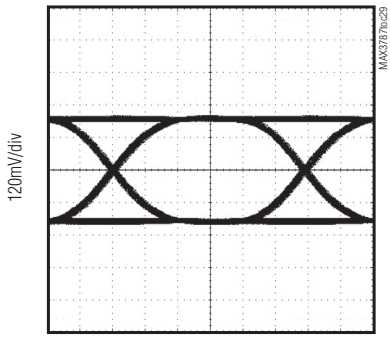
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

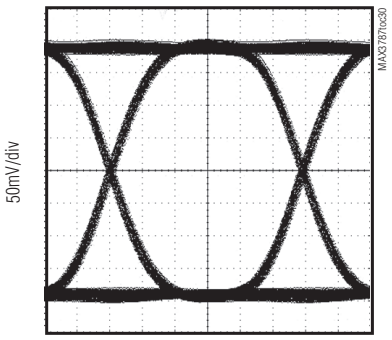
EYE DIAGRAM OF UNEQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



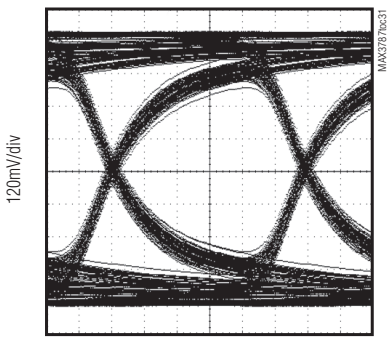
EYE DIAGRAM OF EQUALIZED SIGNAL (18in FR4, 4.25Gbps, STRESS PATTERN)



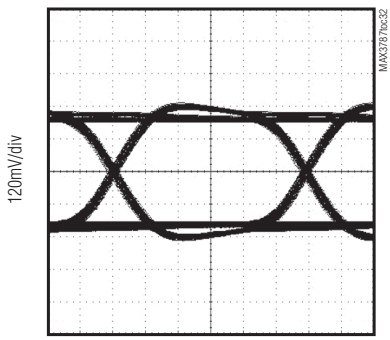
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (18in FR4, 4.25Gbps, STRESS PATTERN)



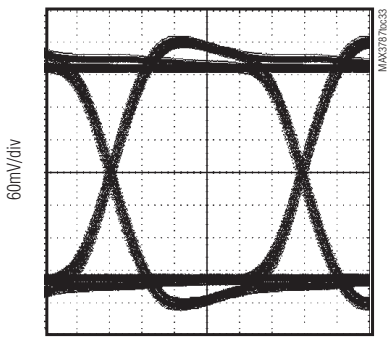
EYE DIAGRAM OF UNEQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



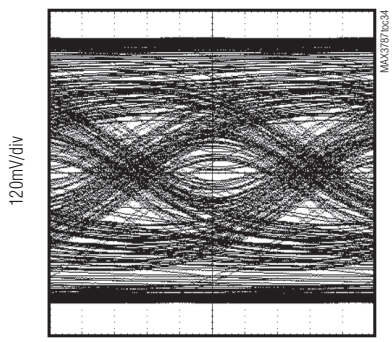
EYE DIAGRAM OF EQUALIZED SIGNAL (12in FR4, 4.25Gbps, STRESS PATTERN)



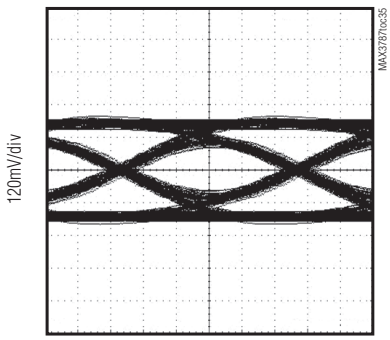
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (12in FR4, 4.25Gbps, STRESS PATTERN)



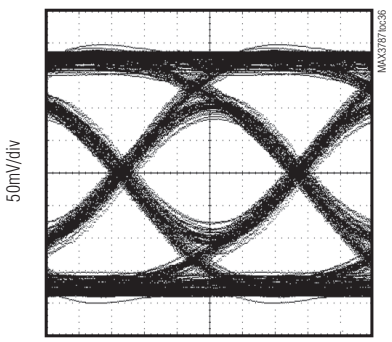
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



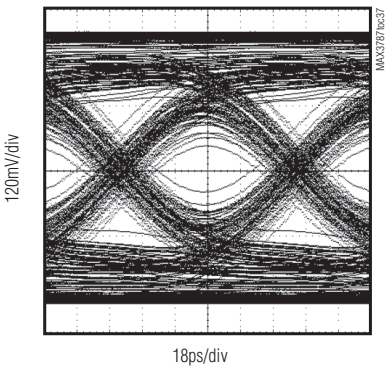
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



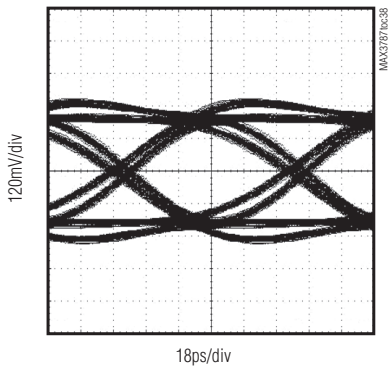
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

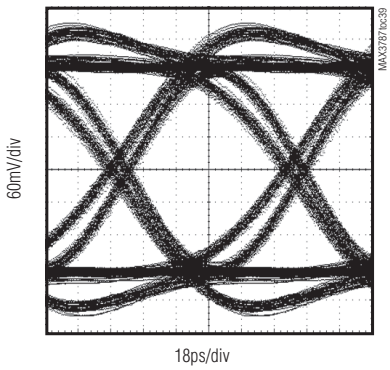
EYE DIAGRAM OF UNEQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



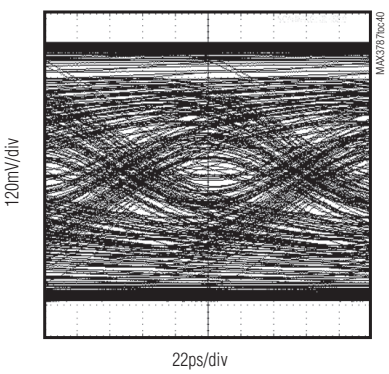
EYE DIAGRAM OF EQUALIZED SIGNAL (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



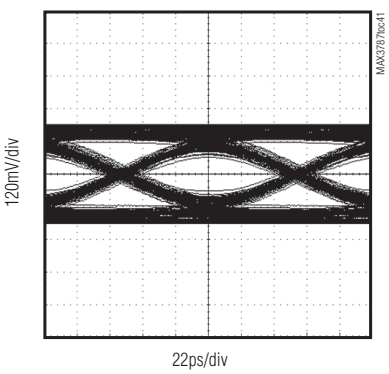
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (3m TWIN-AX CABLE, 10.3125Gbps, STRESS PATTERN)



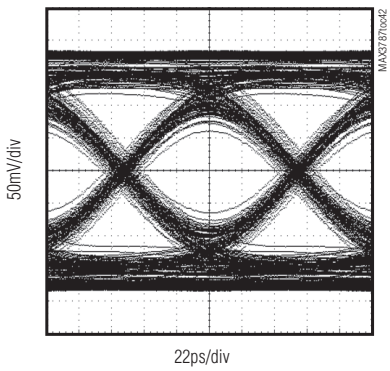
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



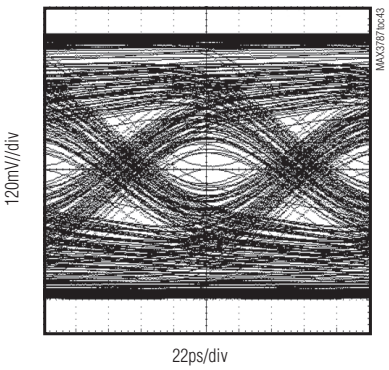
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



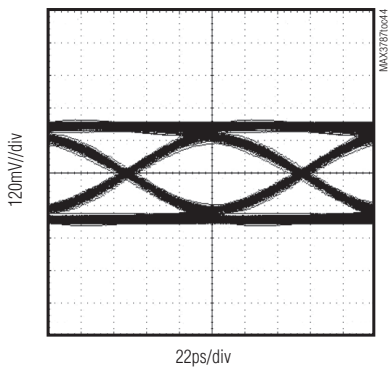
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



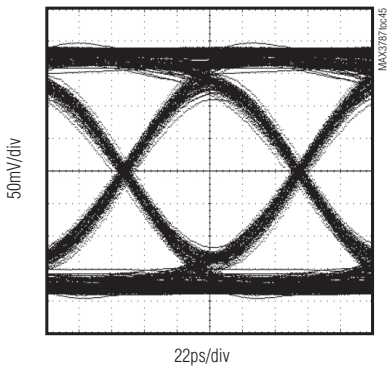
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 8.5Gbps, STRESS PATTERN)

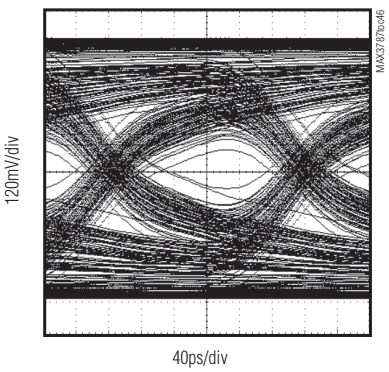


1Gbps至12.5Gbps
无源均衡器，用于背板和电缆数据传输

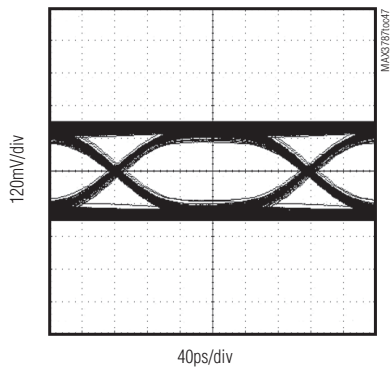
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

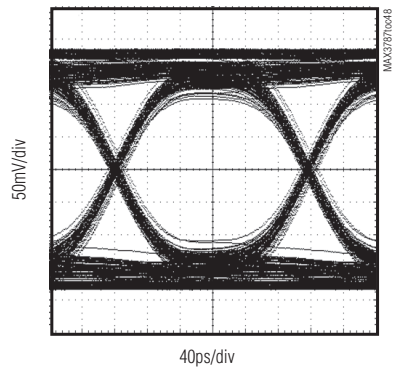
EYE DIAGRAM OF UNEQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



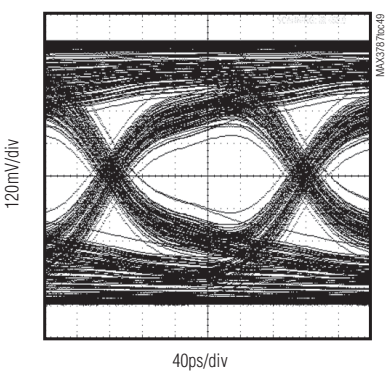
EYE DIAGRAM OF EQUALIZED SIGNAL (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



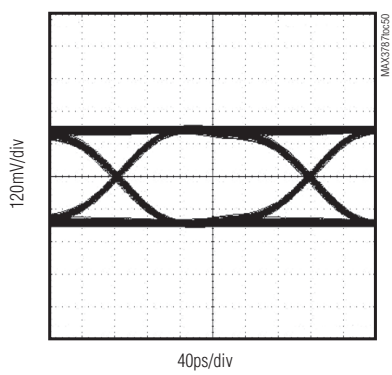
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (7m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



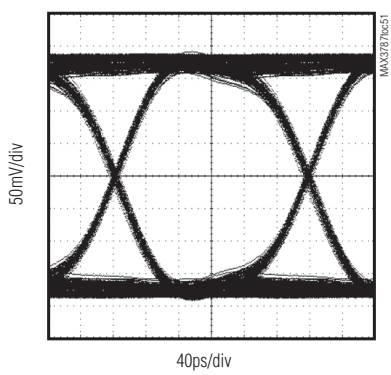
EYE DIAGRAM OF UNEQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



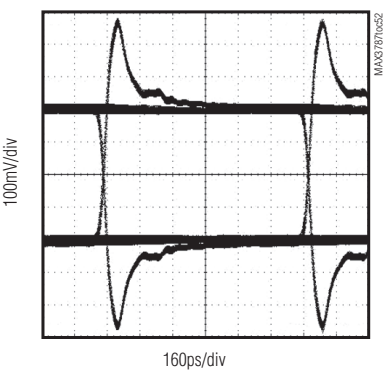
EYE DIAGRAM OF EQUALIZED SIGNAL (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



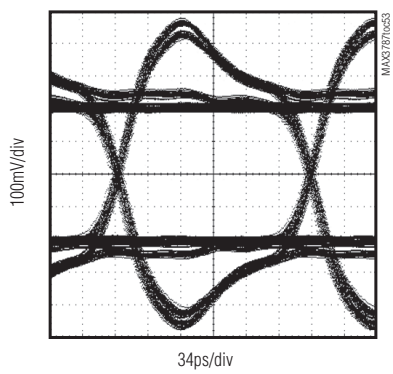
EYE DIAGRAM OF EQUALIZED SIGNAL (ZOOM) (5m TWIN-AX CABLE, 4.25Gbps, STRESS PATTERN)



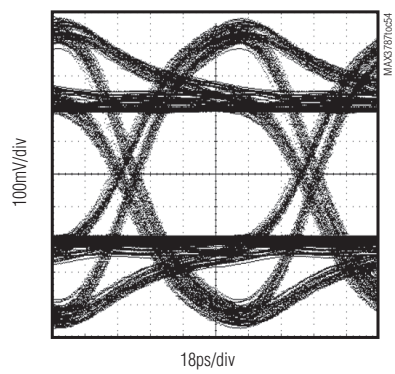
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 1Gbps, STRESS PATTERN)



EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 5Gbps, STRESS PATTERN)



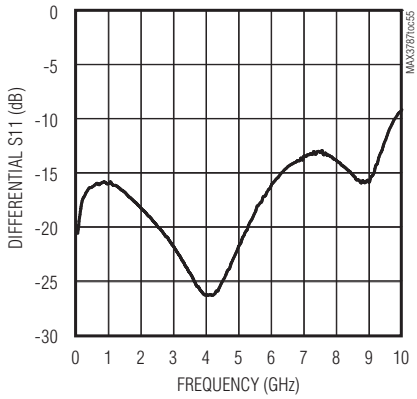
EYE DIAGRAM OF EQUALIZED SIGNAL (0in FR4, 10Gbps, STRESS PATTERN)



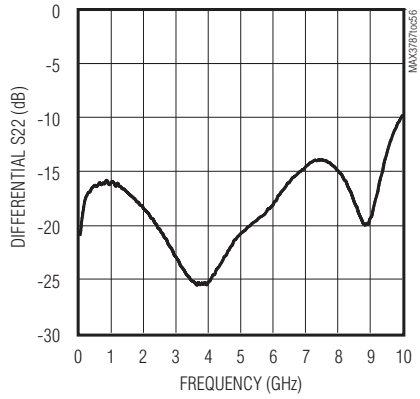
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

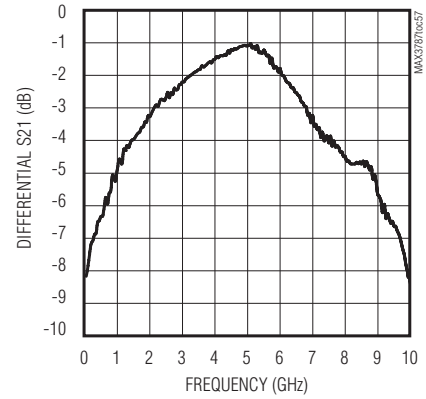
DIFFERENTIAL S11 vs. FREQUENCY



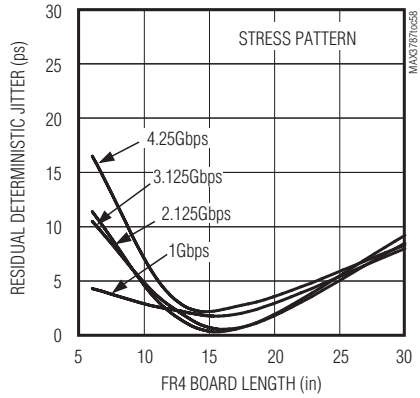
DIFFERENTIAL S22 vs. FREQUENCY



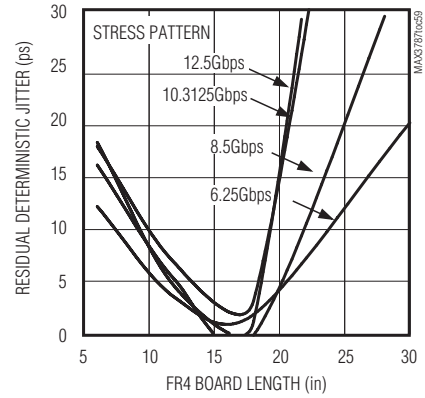
DIFFERENTIAL S21 vs. FREQUENCY



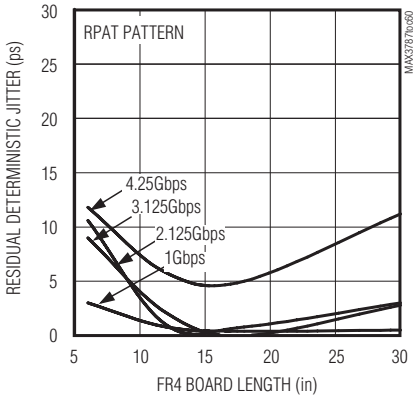
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



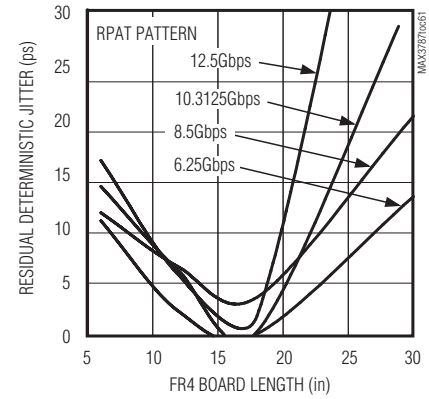
RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH



RESIDUAL DETERMINISTIC JITTER vs. FR4 BOARD LENGTH

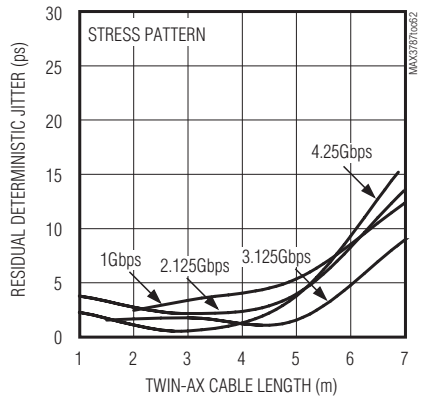


1Gbps至12.5Gbps
无源均衡器，用于背板和电缆数据传输

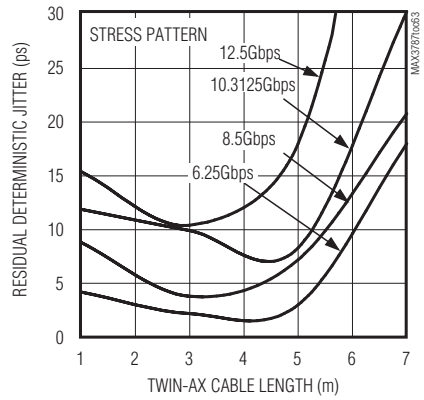
典型工作特性(续)

(T_A = +25°C, unless otherwise noted. All measurements were done with $1V_{P-P}$ at the source. Stress pattern: 2^7 PRBS, 100 zeros, 1, 0, 1, 0, 2^7 PRBS, 100 ones, 0, 1, 0, 1. Residual deterministic jitter graphs were measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams acquired by FrameScan include deterministic jitter of the system (approximately 9ps) but not random jitter. Twin-ax cable: Amphenol Spectra-Strip Skewclear 100Ω 24AWG.)

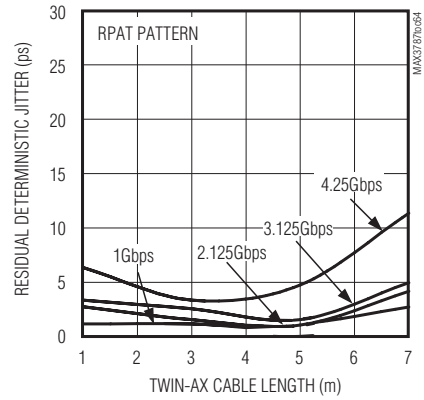
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



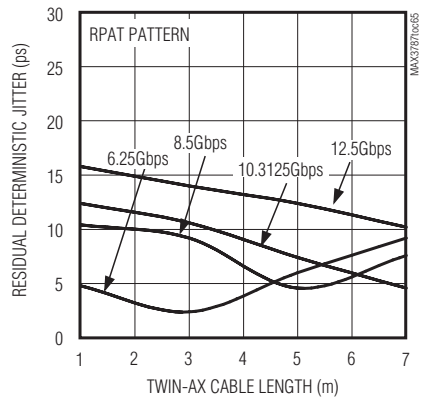
RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



RESIDUAL DETERMINISTIC JITTER vs. TWIN-AX CABLE LENGTH



引脚说明

引脚	名称	功能
A1	IN+	数据输入正端。
A3	OUT+	数据输出正端。
C1	IN-	数据输入负端。
C3	OUT-	数据输出负端。

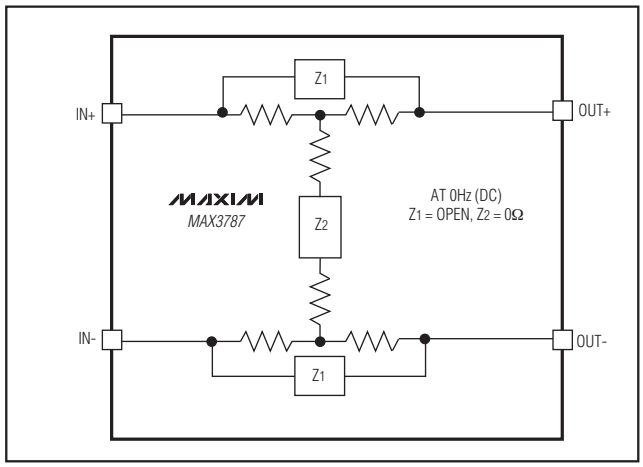


图4. 功能框图

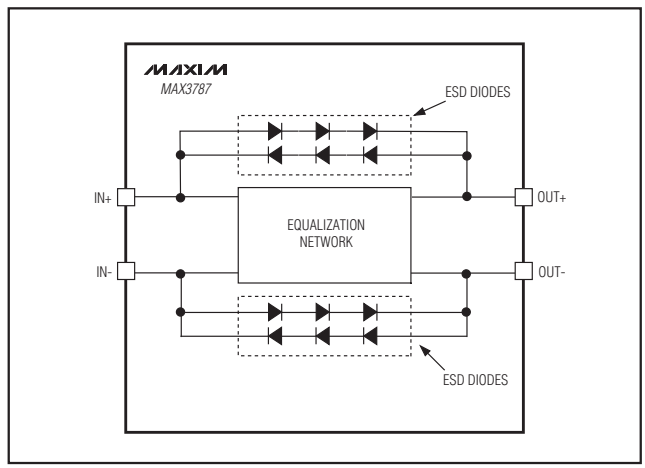


图5. ESD保护二极管

详细说明

MAX3787为无源网络，由阻性元件和电抗元件组成(图4)。带有旁路的两个对称T型网络提供高通特性，组成一个差分、对称的H型网络。整个网络相当于经过特殊调整的滤波器，用于补偿FR4和电缆的传输介质损耗。

输入、输出端接

MAX3787差分输入阻抗为100Ω，输出连接至100Ω差分负载。该网络设计用于传输100Ω平衡差分信号，不适合单端信号传输。

ESD保护二极管

MAX3787集成了ESD二极管，在静态放电时为均衡网络提供保护(图5)。

应用信息

均衡器的整合与放置

MAX3787采用小尺寸1.5mm x 1.5mm UCSP封装，可沿着传输介质放置在任何位置。器件的小尺寸使其易于布局和布线。

由于均衡网络的对称性，能够为从IN至OUT或从OUT至IN的信号提供同样的补偿。均衡器还可以放置在传输介质的任意端，在接收电路提供同样的补偿效果。例如，两个均衡器可以放置在同一收发模块中，一个用于发送路径补偿，另一个用于接收路径补偿(见*典型应用电路*)。

UCSP安装考虑

有关UCSP结构、尺寸、卷带包装信息、PCB技术、焊球-焊盘布局和推荐的回流焊温度曲线以及可靠性测试结果的最新信息，请参考Maxim网站www.maxim-ic.com.cn/ucsp的应用笔记1891：*UCSP—晶片级封装*。

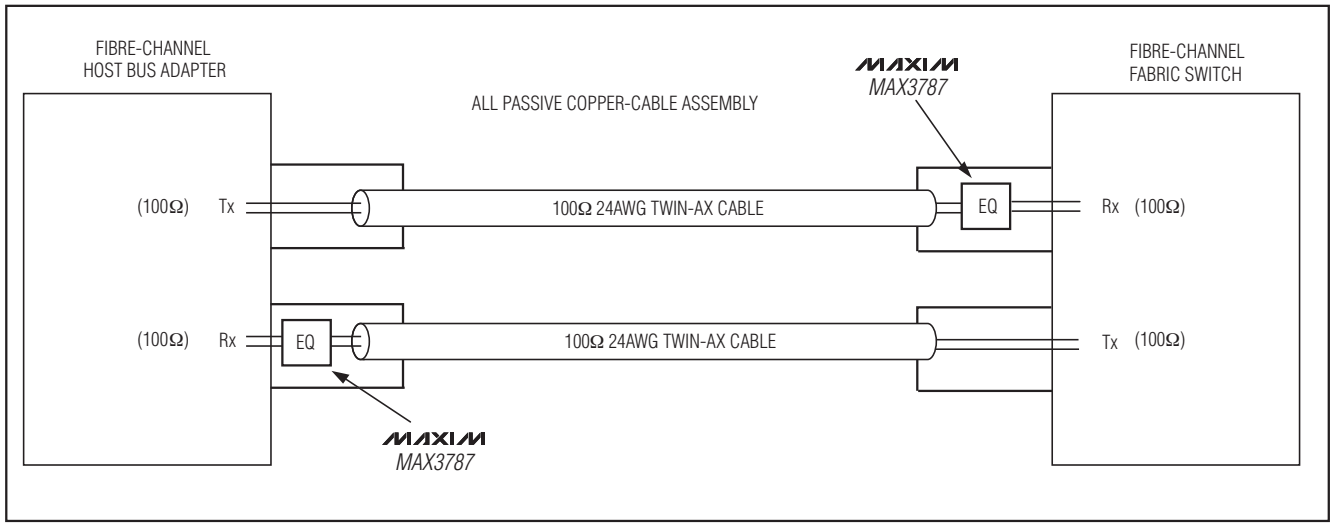
芯片信息

TRANSISTOR COUNT: 0

PROCESS: SiGe BiPOLAR

1Gbps至12.5Gbps
无源均衡器，用于背板和电缆数据传输

典型应用电路(续)



封装信息

(如需最近的封装外形信息，请查询
www.maxim-ic.com.cn/packages。)

封装类型	封装编码	文档编号
4 UCSP	B9-7	**21-0093**
4 WLP	W91B1+3	**21-0067**

修订历史

修订次数	修订日期	说明	修改页
0	7/05	最初版本。	—
1	12/05	在定购信息表中加入无铅封装。	1
2	2/08	将定购信息表中无铅器件的编号由ABL+修改为AWL+，并加入WLP封装类型。	1, 14

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