



### **General Description**

The MAX17108 includes a 10-channel high-voltage level-shifting scan driver and a VCOM amplifier. The device is optimized for thin-film transistor (TFT) liquidcrystal display (LCD) applications.

The high-voltage level-shifting scan driver can swing from +38V to -12V and can swiftly drive capacitive loads. There are two positive supply inputs, which provide flexibility for system design.

The operational amplifier features rail-to-rail output. high short-circuit output current, fast slew rate, and wide bandwidth.

The MAX17108 is available in a 28-pin, 5mm x 5mm, lead-free thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

**Applications** 

LCD TVs LCD Monitors

## **Features** ♦ High-Current, High-Speed Operational Amplifier

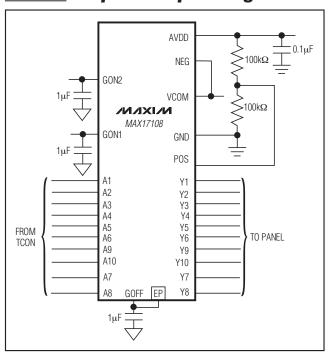
- ±200mA Output Short-Circuit Current 100V/µs Slew Rate 20MHz to 3dB Bandwidth **Rail-to-Rail Outputs**
- ♦ High-Voltage Level-Shifting Scan Drivers **Logic-Level Inputs** +38V to -12V Outputs
- **♦ Thermal-Overload Protection**
- ◆ 28-Pin. 5mm x 5mm Thin QFN Package

### **Ordering Information**

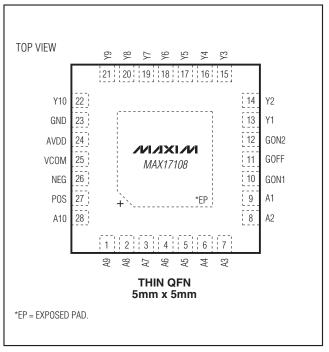
PART	TEMP RANGE	PIN-PACKAGE
MAX17108ETI+	-40°C to +85°C	28 Thin QFN-EP*

<sup>+</sup>Denotes a lead-free/RoHS-compliant package.

## Simplified Operating Circuit



## Pin Configuration



<sup>\*</sup>EP = Exposed pad.

#### **ABSOLUTE MAXIMUM RATINGS**

A1-A10 to GND	0.3V to +7.5V
AVDD to GND	
POS, NEG, VCOM to GND	0.3V to (V <sub>AVDD</sub> to +0.3V)
POS to NEG	6V to +6V
GON1, GON2 to GND	0.3V to +40V
GOFF to GND	14V to +0.3V
Y1-Y6, Y9, Y10 to GND(VGOF	F - 0.3V) to (VGON1 + 0.3V)
Y7, Y8 to GND(VGOF	F - 0.3V) to (V <sub>GON2</sub> + 0.3V)
Y1-Y10 Load RMS Current	140mA

GON1, GON2 RMS Current	350mA
GOFF RMS Current	450mA
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
28-Pin, 5mm x 5mm Thin QFN	
(derate 34.5mW/°C above +70°C)	2758.6mW
Junction Temperature	+150°C
Storage Temperature Range	
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

(Figure 1 circuit,  $V_{AVDD} = 16V$ ,  $V_{GON} = 38V$ ,  $V_{GOFF} = -12V$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE DRIVER BLOCK					
GON_ Input Voltage Range		12		38	V
GOFF Input Voltage Range		-12		-4	V
GOFF Supply Current	A1-A10 = GND, no load		150	300	μΑ
GON_ Total Supply Current	A1-A10 = GND, no load		330	540	μΑ
Output-Voltage Low (Y1-Y10)	I <sub>Y</sub> _ = 10mA		V <sub>GOFF</sub> + 0.03	V <sub>GOFF</sub> + 0.06	V
Output-Voltage High (Y1-Y10)	I <sub>Y</sub> _ = 10mA	V <sub>GON</sub> _ - 0.25	VGON_ - 0.15		V
Rise Time (Y9, Y10)	$T_A = +25$ °C, $V_{GON1} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)			200	ns
Fall Time (Y9, Y10)	$T_A = +25$ °C, $V_{GON1} = 30$ V and $V_{GOFF} = -6.2$ V (Note 1)			200	ns
Rise Time (Y1-Y6)	$T_A = +25$ °C, $V_{GON1} = 30$ V and $V_{GOFF} = -6.2$ V (Note 1)			450	ns
Fall Time (Y1-Y6)	$T_A = +25$ °C, $V_{GON1} = 30$ V and $V_{GOFF} = -6.2$ V (Note 1)			120	ns
Rise Time (Y7, Y8)	$T_A = +25$ °C, $V_{GON1} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)			1600	ns
Fall Time (Y7,Y8)	$T_A = +25$ °C, $V_{GON1} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)			700	ns
Propagation Delay High-to-Low Transition (Y1-Y10)	V <sub>GON</sub> _ = 30V and V <sub>GOFF</sub> = -6.2V (Note 1)		35		ns
Propagation Delay Low-to-High Transition (Y1-Y10)	V <sub>GON</sub> _ = 30V and V <sub>GOFF</sub> = -6.2V (Note 1)		35		ns

### **ELECTRICAL CHARACTERISTICS (continued)**

(Figure 1 circuit,  $V_{AVDD} = 16V$ ,  $V_{GON} = 38V$ ,  $V_{GOFF} = -12V$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIER		•			
AVDD Supply Range		6		20	V
AVDD Supply Current	Buffer configuration, VPOS = VAVDD/2, no load			6	mA
Input Offset Voltage	2V < (V <sub>NEG</sub> , V <sub>POS</sub> ) < (V <sub>AVDD</sub> - 2V), T <sub>A</sub> = +25°C	-10		+10	mV
Input Bias Current	V <sub>NEG</sub> , V <sub>POS</sub> = V <sub>AVDD</sub> /2, T <sub>A</sub> = +25°C	-50		+50	nA
Input Common-Mode Voltage Range		0		V <sub>AVDD</sub>	V
Input Common-Mode Rejection Ratio	2V < (V <sub>NEG</sub> , V <sub>POS</sub> ) < (V <sub>AVDD</sub> - 2V)		80		dB
Output-Voltage Swing High	IVCOM = 50mA	V <sub>AVDD</sub> - 400			mV
Output-Voltage Swing Low	Ivcom = -50mA			400	mV
Large-Signal Voltage Gain	$V_{VCOM} = 1V \text{ to } V_{AVDD} - 1V$		80		dB
Slew Rate			100		V/µs
-3dB Bandwidth			20		MHz
Short-Circuit Current	Short to V <sub>AVDD</sub> /2, sourcing		230		mA
Short-Circuit Current	Short to V <sub>AVDD</sub> /2, sinking		460		IIIA
FAULT DETECTION					
Thermal Shutdown	Rising edge, typical hysteresis = 10°C, not latched		+155		°C
CONTROL INPUTS					
Logic-Input Voltage Range (A1-A10)	(Note 3)			6	V
Logic-Input Voltage Low (A1-A10)				0.8	V
Logic-Input Voltage High (A1-A10)		2			V
Logic-Input Bias Current (A1-A10)	$0 < V_A < 6V, T_A = +25^{\circ}C$	-1		+1	μΑ

#### **ELECTRICAL CHARACTERISTICS**

(Figure 1 circuit, VAVDD = 16V, VGON = 38V, VGOFF = -12V, TA = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
HIGH-VOLTAGE DRIVER BLOCK	HIGH-VOLTAGE DRIVER BLOCK						
GON_ Input Voltage Range		12		38	V		
GOFF Input Voltage Range		-12		-4	V		
GOFF Supply Current	A1-A10 = GND, no load			300	μΑ		
GON_ Total Supply Current	A1-A10 = GND, no load			540	μΑ		
Output-Voltage Low (Y1-Y10)	I <sub>Y</sub> _ = 10mA			V <sub>GOFF</sub> + 0.06	V		
Output-Voltage High (Y1-Y10)	I <sub>Y</sub> _ = 10mA	VGON_ - 0.25			V		

### **ELECTRICAL CHARACTERISTICS (continued)**

(Figure 1 circuit,  $V_{AVDD} = 16V$ ,  $V_{GON} = 38V$ ,  $V_{GOFF} = -12V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
OPERATIONAL AMPLIFIER	OPERATIONAL AMPLIFIER						
AVDD Supply Range		6		20	V		
AVDD Supply Current	Buffer configuration, VPOS = VAVDD/2, no load			6	mA		
Input Common-Mode Voltage Range		0		V <sub>A</sub> VDD	V		
Output-Voltage Swing High	IVCOM = 50mA	V <sub>AVDD</sub> - 400			mV		
Output-Voltage Swing Low	Ivcom = -50mA			400	mV		
CONTROL INPUTS							
Logic-Input Voltage Range (A1-A10)	(Note 3)			6	V		
Logic-Input Voltage Low (A1-A10)				0.8	V		
Logic-Input Voltage High (A1-A10)		2			V		

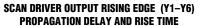
Note 1: The load models for different channels are illustrated in Figure 2.

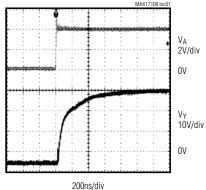
**Note 2:** T<sub>A</sub> = -40°C specifications are guaranteed by design, not production tested.

Note 3: For  $5.5V < V_{A} < 6V$ , use the IC for no longer than 1% of IC lifetime. For continuous operation, voltage should not exceed 5.5V.

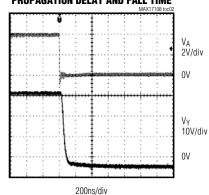
## Typical Operating Characteristics

(Circuit of Figure 1,  $V_{AVDD}$  = 16V,  $V_{GON}$  = 38V,  $V_{GOFF}$  = -12V,  $T_A$  = 0°C to +85°C. Typical values are at  $T_A$  = +25°C, unless otherwise noted.)





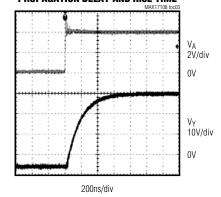
# SCAN DRIVER OUTPUT FALLING EDGE (Y1-Y6) PROPAGATION DELAY AND FALL TIME



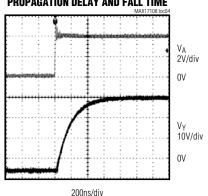
## Typical Operating Characteristics (continued)

(Circuit of Figure 1,  $V_{AVDD}$  = 16V,  $V_{GON}$  = 38V,  $V_{GOFF}$  = -12V,  $T_A$  = 0°C to +85°C. Typical values are at  $T_A$  = +25°C, unless otherwise noted.)

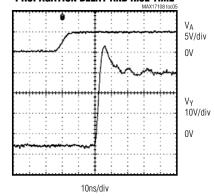
## SCAN DRIVER OUTPUT RISING EDGE (Y7 AND Y8) PROPAGATION DELAY AND RISE TIME



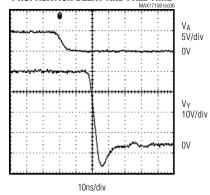
## SCAN DRIVER OUTPUT FALLING EDGE (Y7 AND Y8) PROPAGATION DELAY AND FALL TIME



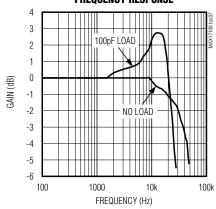
# SCAN DRIVER OUTPUT RISING EDGE (Y9 AND Y10) PROPAGATION DELAY AND RISE TIME



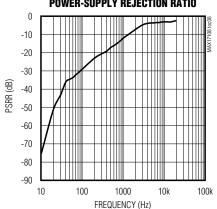
# SCAN DRIVER OUTPUT FALLING EDGE (Y9 AND Y10) PROPAGATION DELAY AND FALL TIME



## OPERATION AMPLIFIER FREQUENCY RESPONSE



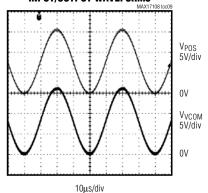
## OPERATIONAL AMPLIFIER POWER-SUPPLY REJECTION RATIO



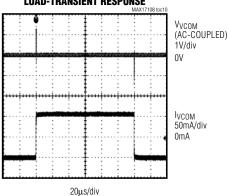
## Typical Operating Characteristics (continued)

(Circuit of Figure 1,  $V_{AVDD}$  = 16V,  $V_{GON}$  = 38V,  $V_{GOFF}$  = -12V,  $T_A$  = 0°C to +85°C. Typical values are at  $T_A$  = +25°C, unless otherwise noted.)

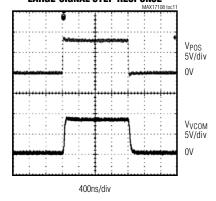
## OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



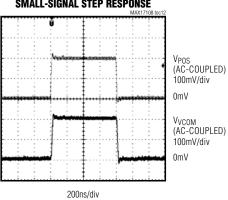
#### OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



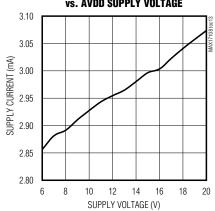
## OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



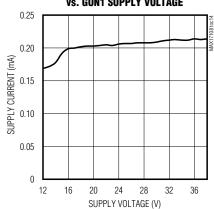
# OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



## AVDD SUPPLY QUIESCENT CURRENT vs. AVDD SUPPLY VOLTAGE

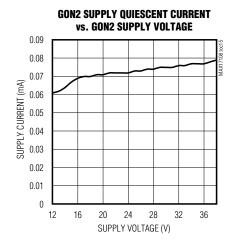


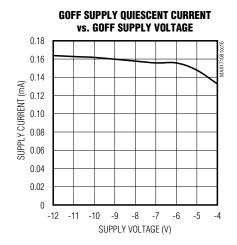
## GON1 SUPPLY QUIESCENT CURRENT vs. GON1 SUPPLY VOLTAGE



## Typical Operating Characteristics (continued)

(Circuit of Figure 1,  $V_{AVDD}$  = 16V,  $V_{GON}$  = 38V,  $V_{GOFF}$  = -12V,  $T_A$  = 0°C to +85°C. Typical values are at  $T_A$  = +25°C, unless otherwise noted.)





## **Pin Description**

PIN	NAME	FUNCTION	
1–9	A9-A1	Level-Shifter Logic-Level Input	
10	GON1	Gate-On Supply Input 1. GON1 is the positive supply for the Y1-Y6, Y9, and Y10 level shifters. Bypass GON1 with a minimum of 1µF ceramic capacitor to GND.	
11	GOFF	Gate-Off Supply Input. GOFF is the negative supply for the Y1–Y10 level shifters. Bypass GOFF with a minimum of $1\mu F$ ceramic capacitor to GND.	
12	GON2	Gate-On Supply Input 2. GON2 is the positive supply for the Y7 and Y8 level shifters. Bypass GON2 with a minimum of 1µF ceramic capacitor to GND.	
13–22	Y1-Y10	vel-Shifter Outputs	
23	GND	Ground	
24	AVDD	Operational Amplifier Supply Voltage. Bypass AVDD with a minimum of 1µF ceramic capacitor to GND.	
25	VCOM	Operational Amplifier Output	
26	NEG	Operational Amplifier Negative Input	
27	POS	perational Amplifier Positive Input	
28	A10	Level-Shifter Logic-Level Input	
_	EP	Exposed Backside Pad. Connect to V <sub>GOFF</sub> . Copper area should be maximized for thermal performance.	

## **Detailed Description**

The MAX17108 includes a 10-channel, high-voltage level-shifting scan driver, an operational amplifier for VCOM, and a linear regulator that provides the internal bias for the step-up controller. Figure 1 shows the MAX17108 functional block diagram and typical operating circuit.

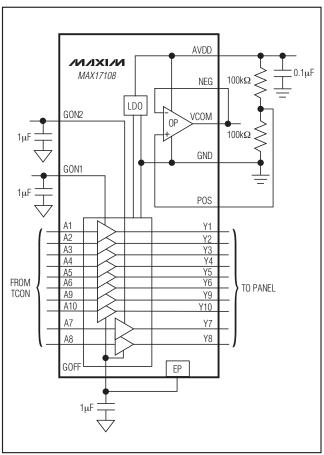


Figure 1. Functional Block Diagram and Typical Operating Circuit

## Load Models for Different Channels

Figure 2 shows the load models for different channels.

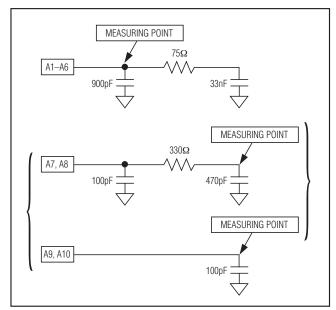


Figure 2. Load Models for Different Channels

#### **Operational Amplifier**

The MAX17108 has one operational amplifier that is typically used to drive the LCD backplane (VCOM). The operational amplifier features a ±200mA output short-circuit current, 100V/µs slew rate, 20MHz bandwidth, and rail-to-rail output.

#### Short-Circuit Current Limit

The operational amplifier limits the short-circuit current to approximately ±200mA. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+155°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor shuts off the operational amplifier. The thermal protection is not latched and the device recovers once the temperature drops below the hysteretic threshold (+10°C typ).

#### **Driving Pure Capacitive Loads**

The operational amplifier is typically used to drive the LCD backplane (VCOM). The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A  $5\Omega$  to  $50\Omega$  resistor placed between VCOM and the capacitive load reduces peaking but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between  $100\Omega$  and  $200\Omega$  and the typical value of the capacitor is 10pF.

#### **High-Voltage Level-Shifting Scan Driver**

The MAX17108 includes 10 logic-level to high-voltage level-shifting buffers, which can buffer 10 logic inputs (A1–A10) and shift them to a desired level (Y1–Y10) to drive TFT-LCD row logic. The driver outputs, Y1–Y10, swing between their power-supply rails, according to the input-logic level on A1–A10. The driver output is VGOFF when its respective input is logic-low, and VGON when its respective input is logic-high.

These 10 driver channels are grouped for different high-level supplies. A1–A6 and A9–A10 are supplied from GON1; A7 and A8 are supplied from GON2.

The high-voltage, level-shifting scan drivers swing from +38V to -12V and can swiftly drive capacitive loads. The typical propagation delays are 35ns.

#### Thermal Shutdown

The MAX17108 includes a thermal-protection circuit. When the local IC temperature exceeds +155°C (typ), the device shuts down and recovers when the die temperature drops by 10°C (typ).

## Design Procedure

All MAX17108 designs should be prototyped and tested prior to production. Table 1 provides a list of components for the typical operating circuit. Table 2 shows a component supplier.

#### **Table 1. Component List**

DESIGNATION	DESCRIPTION
1μF bypassing capacitors	1µF ±10%, 50V X7R ceramic capacitors (0805) Murata GRM21BR71H105K
0.1µF bypassing capacitors	0.1µF ±10%, 25V X5R ceramic capacitors (0603) Murata GRM188R61E104K

### **Table 2. Component Supplier**

SUPPLIER	PHONE	WEBSITE	
Murata Electronic North America, Inc.	770-436-1300	www.murata.com	

### \_Applications Information

#### **Power Dissipation**

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17108, with its exposed backside pad soldered to 1in² of PCB copper, can dissipate approximately 2700mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the operational amplifier and the high-voltage scan drivers.

#### Operational Amplifier

The power dissipated in the operational amplifiers depends on the output current, the output voltage, and the supply voltage:

 $PD_{SOURCE} = I_{VCOM\_SOURCE} \times (V_{AVDD} - V_{VCOM})$ 

$$PD_{SINK} = I_{VCOM\_SINK} \times V_{VCOM}$$

where IVCOM\_SOURCE is the output current sourced by one operational amplifier, and IVCOM\_SINK is the output current that the operational amplifier sinks.

In a typical case, where the supply voltage is 8V and the output voltage is 4V with an output source current of 30mA for the operational amplifier, the power dissipated is 120mW.

#### Scan Driver Outputs

When driving a pure capacitive load, the power dissipated by the scan driver outputs (A1–A6; A7–A10 are low-frequency outputs and the power dissipation by these outputs can be omitted) depends on the scan frequency, the capacitive load, and the difference between the GON1 and GOFF supply voltages:

$$PD_{SCAN} = 6 \times f_{SCAN} \times C_{PANEL} \times (V_{GON1} - V_{GOFF})^2$$

If the six scan drivers operate at a frequency of 50kHz, the load of the six outputs is 5nF, and the supply voltage difference is 30V, then the power dissipated is 1.35W.

#### **PCB Lavout Guidelines**

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

 Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

- Create VGOFF plane, connect it to EP.
- Create a ground island (GND) consisting of the input and output capacitor grounds and GND pin. Connect all these together with short, wide traces or a small ground plane.
- Place the voltage-divider resistors as close as possible to the POS pin. The divider's center trace should be kept short. Placing the resistors far away causes the POS trace to become an antenna that can pick up switching noise.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.

Refer to the MAX17108 Evaluation Kit for an example of proper board layout.

### **Chip Information**

TRANSISTOR COUNT: 2918

PROCESS: BICMOS

## Package Information

For the latest package outline information and land patterns, go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN	T2855-6	<u>21-0140</u>

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