19-3131; Rev 0; 3/08

MAXIM

50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

概述

MAX2065高线性度、模拟/数字调节可变增益放大器(VGA)针对50MHz至1000MHz频率范围的应用而设计，带有两级独立的衰减器(参见*典型应用电路*)。可通过SPI™兼容接口控制作为从机外设的数字衰减器；也允许以1dB步长通过并行总线控制，可调节范围为31dB。该器件增加了“速射”增益选择，可直接设置在4种增益选项的一种，用户可通过SPI接口预先设置四种增益选项。2个控制引脚允许用户快速选择4种定制衰减的任何一个，无需SPI总线编程。利用外部电压或通过SPI接口控制片上8位DAC实现衰减器模拟调节。

因为三级电路的每一级都具有RF输入和RF输出，通过适当配置可以优化NF (第1级为放大器)、OIP3 (最后一级为放大器)或在NF和OIP3之间进行折衷。该器件还包含具有22dB增益的放大器(放大器本身)，增益最大时NF为6.5dB(包括衰减器的插入损耗)，并提供+42dBm的高OIP3。这些特性使得MAX2065能够为众多接收器和发射器提供一个理想的VGA。

另外，MAX2065采用+5V单电源供电，提供功能完备的解决方案；工作在+3.3V时，性能指标略有降低，可以调节偏置电流在电流损耗和线性度方面进行折衷。器件采用紧凑、带裸焊盘的40引脚、薄型QFN封装(6mm x 6mm)。工作在扩展级温度范围(T_C = -40°C至+85°C)。

应用

IF和RF增益分级设计

温度补偿电路

蜂窝频段WCDMA和cdma2000®基站

GSM 850/GSM 900 EDGE基站

WiMAX和LTE基站以及用户驻地设备

固定宽带无线接入

无线本地环路

军用系统

视频点播(VOD)和DOCSIS®兼容于EDGE QAM调制电缆调制解调器端接系统(CMTS)

SPI是Motorola, Inc.的商标。

特性

- ♦ 50MHz到1000MHz RF频率范围
- ♦ 引脚兼容的系列产品包括：
  MAX2066 (数字VGA)
  MAX2067 (模拟VGA)
- ♦ +19.4dB (典型值)最大增益
- ♦ 100MHz带宽内保持0.5dB增益平坦度
- ♦ 62dB增益范围(31dB模拟控制增益 + 31dB数字控制增益)
- ♦ 内置用于模拟衰减控制的DAC
- ♦ 支持4种“速射”预编程衰减选项
  快速设置4种定制衰减之一，无需SPI总线编程
  理想用于快速响应和信号阻塞保护
  避免ADC过驱动
- ♦ 优异的线性指标(配置放大器为最后一级)
  +42dBm OIP3
  +63dBm OIP2
  +19dBm输出1dB压缩点
  -67dBc HD2
  -83dBc HD3
- ♦ 6.5dB典型噪声系数(NF)
- ♦ 25ns快速数字切换
- ♦ 超低数字VGA过冲/欠冲幅度
- ♦ 单电源+5V供电(可选择+3.3V单电源供电)
- ♦ 优异的外部电流设置电阻，提供降功率/降性能两种工作模式

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2065ETL+	-40°C to +85°C	40 Thin QFN-EP*	T4066-3
MAX2065ETL+T	-40°C to +85°C	40 Thin QFN-EP*	T4066-3

+表示无铅封装。
**EP = 裸焊盘。*
T = 卷带包装。

引脚配置在数据资料的最后给出。

cdma2000是电信工业协会的注册商标。
DOCSIS和CableLabs是Cable Television Laboratories, Inc. (CableLabs®)的注册商标。

ABSOLUTE MAXIMUM RATINGS

VCC_ to GND .....-0.3V to +5.5V
VDD_LOGIC, DATA, $\overline{CS}$, CLK, SER/PAR, VDAC_EN, VREF_SELECT.....-0.3V to (VCC_ + 0.3V)
STATE_A, STATE_B, D0–D4 .....-0.3V to (VCC_ + 0.3V)
AMP_IN, AMP_OUT, VREF_IN, ANALOG_VCTRL .....-0.3V to (VCC_ + 0.3V)
ATTEN1_IN, ATTEN1_OUT, ATTEN2_IN, ATTEN2_OUT.....-1.2V to + 1.2V
RSET to GND.....-0.3V to + 1.2V
RF Input Power (ATTEN1_IN, ATTEN1_OUT, ATTEN2_IN, ATTEN2_OUT).....+20dBm
RF Input Power (AMP_IN).....+18dBm
Continuous Power Dissipation (Note 1) 6.5W
θ_{JA} (Notes 2, 3).....+38°C/W
θ_{JC} (Note 3) .....+10°C/W
Operating Temperature Range (Note 4).....T_C = -40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com.cn/thermal-tutorial**.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, high-current (HC) mode, V_{CC} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Current	I_{CC}			60	80	mA
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}			2		V
Input Low Voltage	V_{IL}			0.8		V

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +4.75V to +5.25V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Low-current (LC) mode		73	93	mA
		High-current (HC) mode		124	146	
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Current Logic-High	I_{IH}		-1		+1	µA
Input Current Logic-Low	I_{IL}		-1		+1	µA

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, HC mode with attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 6, 7)	50		1000	MHz
Small Signal Gain	G			18.8		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, maximum gain setting		37.5		dBm
Noise Figure	NF	Maximum gain setting		6.7		dB
Total Attenuation Range		Analog and digital combined		61.5		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 6, 7)		50		1000	MHz
Small Signal Gain	G	200MHz			19.4		dB
		350MHz, T_C = +25°C		17.5	18.7	19.7	
		450MHz			18.2		
		750MHz			16.4		
		900MHz			15.6		
Gain Variation vs. Temperature					-0.006		dB/°C
Gain Flatness vs. Frequency		Any 100MHz frequency band from 50MHz to 500MHz			0.5		dB
Noise Figure	NF	200MHz			6.5		dB
		350MHz, T_C = +25°C (Note 7)			6.8	8	
		450MHz			7		
		750MHz			7.8		
		900MHz			8.2		
Total Attenuation Range		Analog and digital combined			61.5		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$			63		dBm
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, HC mode, Δf = 1MHz	200MHz		42		dBm
			350MHz		40		
			450MHz		39		
			750MHz		36		
			900MHz		35		
		P_{OUT} = 0dBm/tone, LC mode, Δf = 1MHz	200MHz		40		
			350MHz		38		
			450MHz		37		
			750MHz		35		
			900MHz		33		

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	350MHz, T_C = +25°C (Note 8)		17	18.7		dBm
Second Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 7)		-60	-67		dBc
Third Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 7)		-71	-83		dBc
Input Return Loss		50Ω source, maximum gain setting			18		dB
Output Return Loss		50Ω load, maximum gain setting			18		dB
DIGITAL ATTENUATOR							
Insertion Loss					2.5		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz, $f_1 + f_2$			52		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz			41		dBm
Attenuation Range					31.2		dB
Step Size					1		dB
Relative Step Accuracy					0.2		dB
Absolute Step Accuracy					0.45		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		4.8		Degrees
			24dB		8		
			31dB		10.8		
Amplitude Overshoot/Undershoot		Between any two states	ET = 15ns		1.0		dB
			ET = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss		50Ω source			19		dB
Output Return Loss		50Ω load			19		dB
ANALOG ATTENUATOR							
Insertion Loss					1.2		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz, $f_1 + f_2$			70		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz			36		dBm
Attenuation Range		Analog control input			31.1		dB
Gain Control Slope		Analog control input			-12.5		dB/V
Maximum Gain Control Slope		Over analog control input range			-35		dB/V
Insertion Phase Change		Over analog control input range			18		Degrees
Group Delay		Maximum gain setting			0.98		ns
Group Delay vs. Control Voltage		Over analog control input range			-0.25		ns
Analog Control Input Range				0.25		2.75	V

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +4.75 to +5.25V, HC mode with each attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Control Input Impedance				80		kΩ
Input Return Loss		50Ω source		22		dB
Output Return Loss		50Ω load		22		dB
D/A CONVERTER						
Number of Bits				8		Bits
Output Voltage		DAC code = 00000000			0.25	V
		DAC code = 11111111	2.75			
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed	f_{CLK}			20		MHz
Data-to-Clock Setup Time	t_{CS}			2		ns
Data-to-Clock Hold Time	t_{CH}			2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}			3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}			7		ns
$\overline{CS}$ Setup Time	t_{EWS}			3.5		ns
Clock Pulse Width	t_{CW}			5		ns

Note 5: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*.

Note 6: Operating outside this range is possible, but with degraded performance of some parameters.

Note 7: Guaranteed by design and characterization.

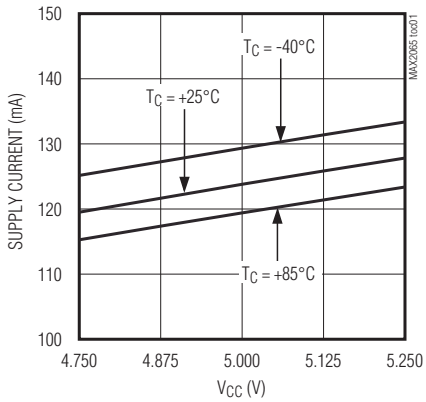
Note 8: It is advisable not to operate continuously the VGA RF input above +15dBm.

50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

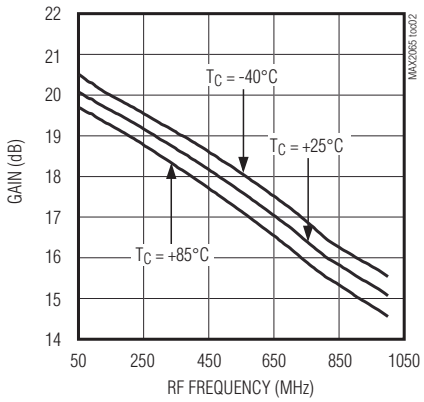
典型工作特性

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

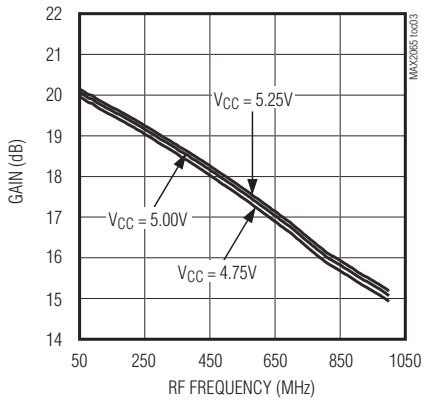
SUPPLY CURRENT vs. V_{CC}



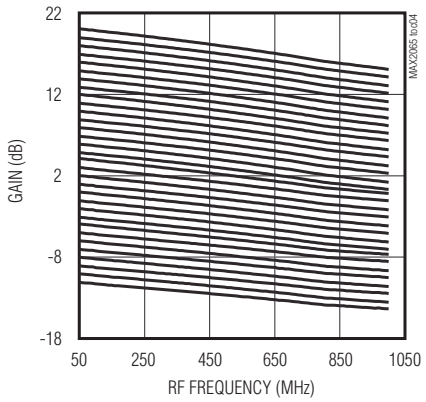
GAIN vs. RF FREQUENCY



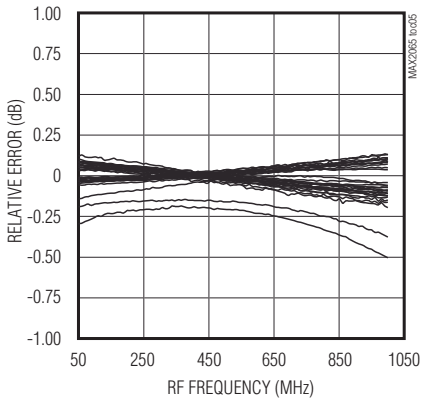
GAIN vs. RF FREQUENCY



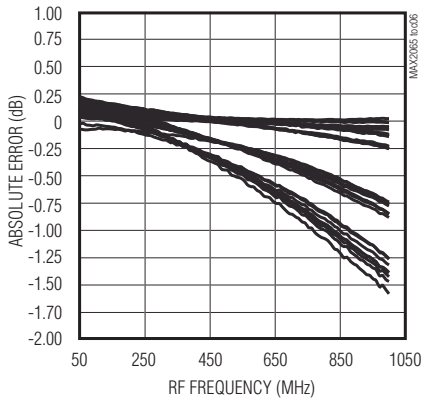
GAIN OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



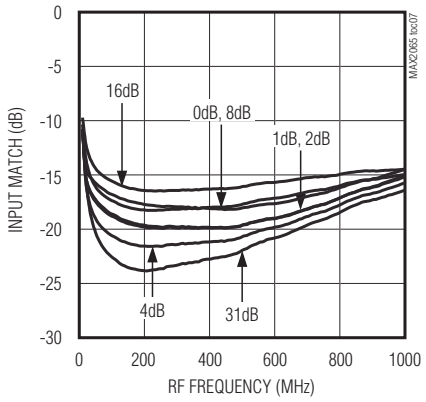
DIGITAL ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



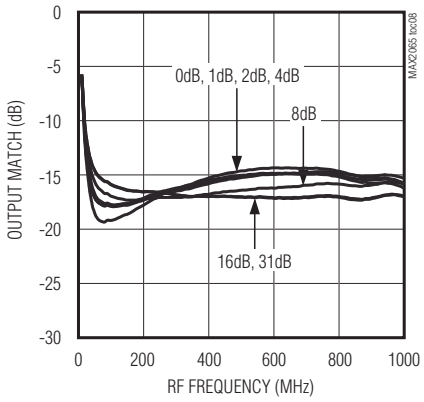
DIGITAL ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



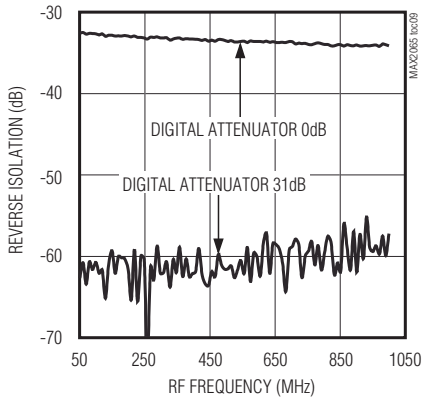
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



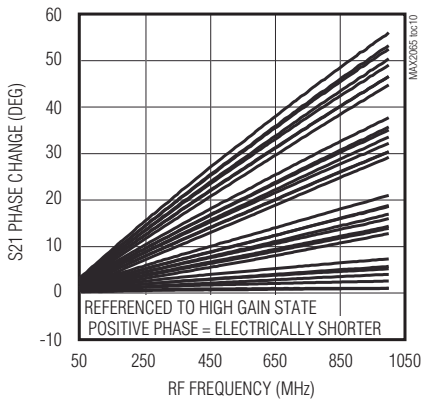
REVERSE ISOLATION OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



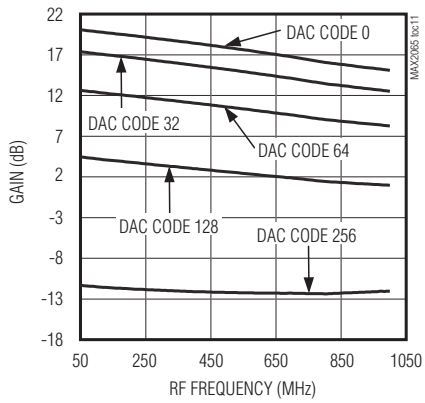
典型工作特性(续)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

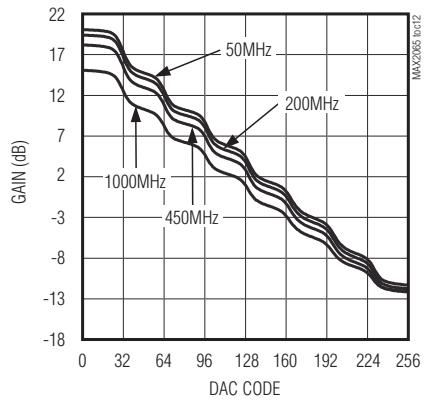
S21 PHASE CHANGE OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



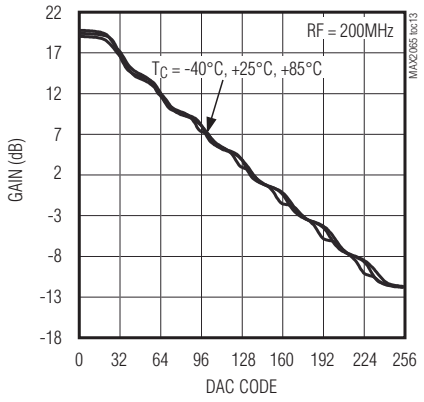
GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



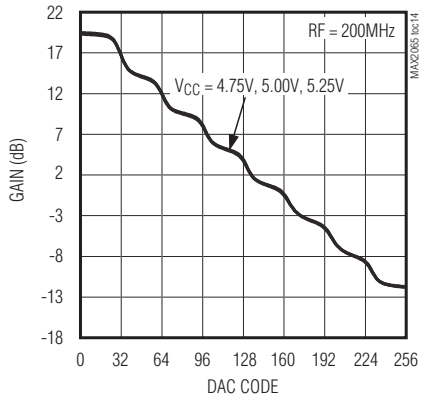
GAIN vs. ANALOG ATTENUATOR SETTING



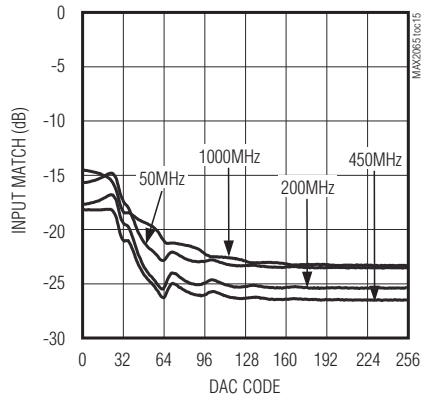
GAIN vs. ANALOG ATTENUATOR SETTING



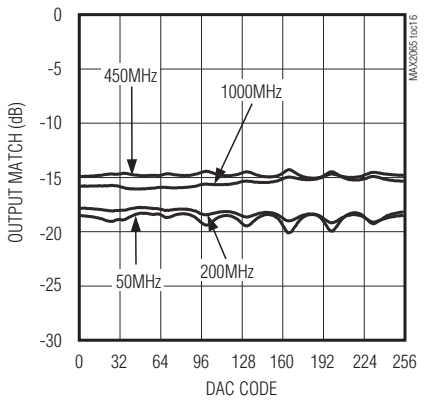
GAIN vs. ANALOG ATTENUATOR SETTING



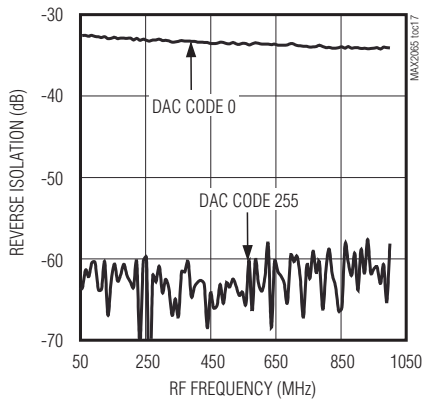
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



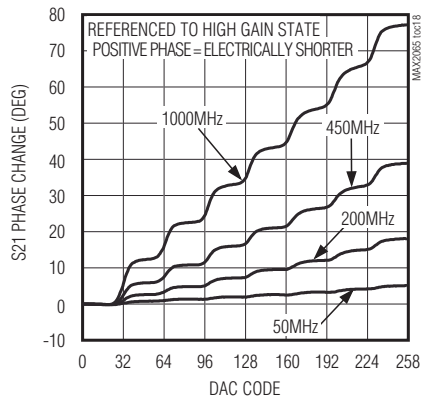
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



REVERSE ISOLATION OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY



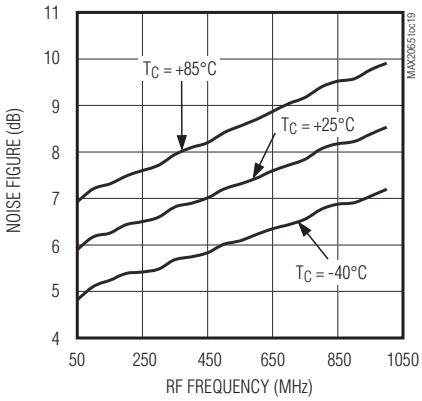
S21 PHASE CHANGE vs. ANALOG ATTENUATOR SETTING



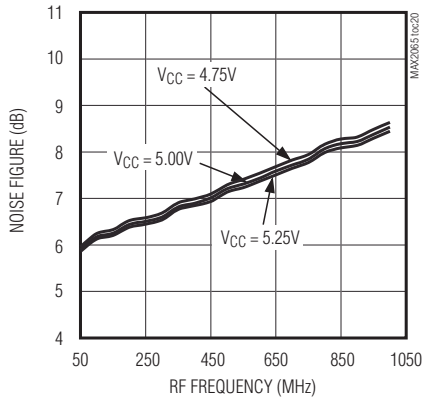
典型工作特性(续)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

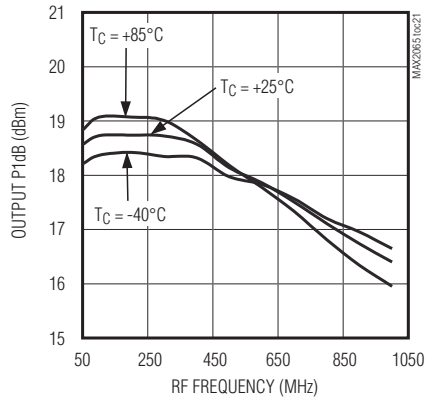
NOISE FIGURE vs. RF FREQUENCY



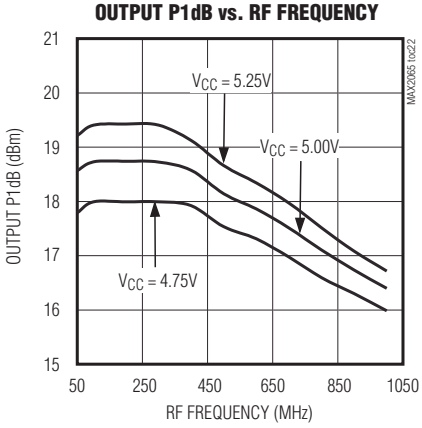
NOISE FIGURE vs. RF FREQUENCY



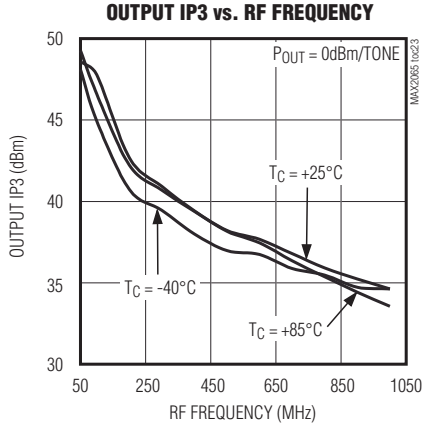
OUTPUT P1dB vs. RF FREQUENCY



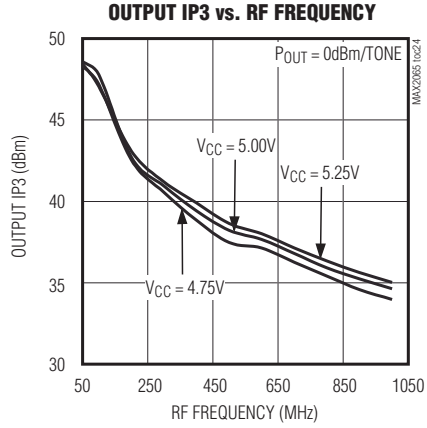
OUTPUT P1dB vs. RF FREQUENCY



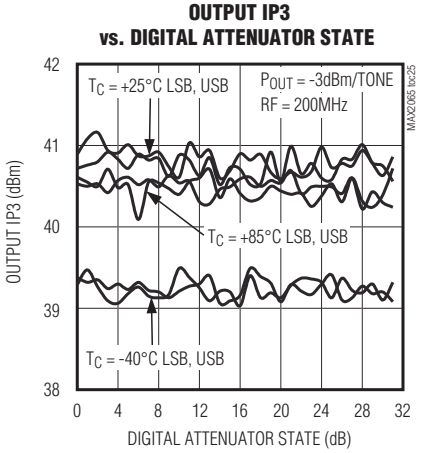
OUTPUT IP3 vs. RF FREQUENCY



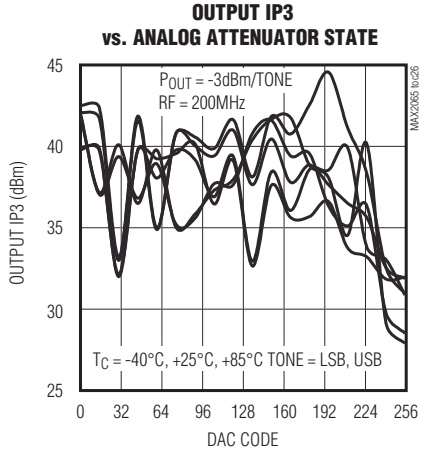
OUTPUT IP3 vs. RF FREQUENCY



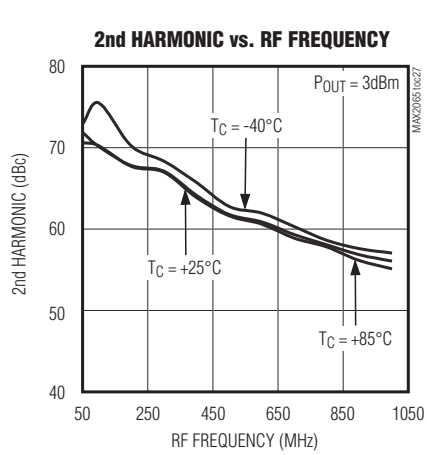
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



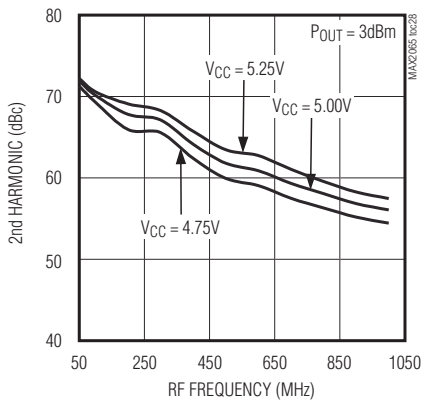
2nd HARMONIC vs. RF FREQUENCY



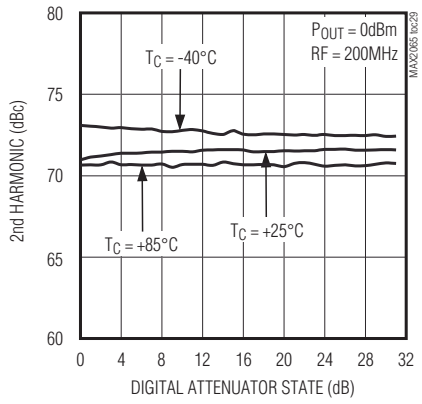
典型工作特性(续)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

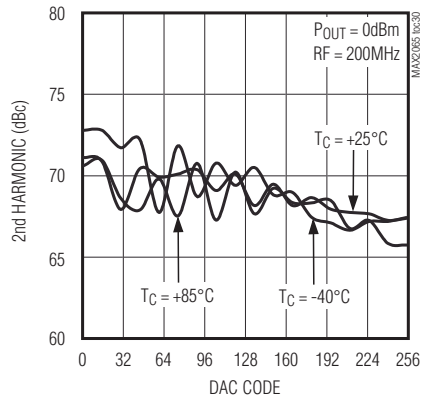
2nd HARMONIC vs. RF FREQUENCY



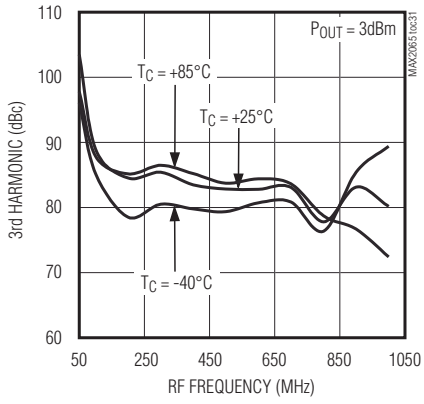
2nd HARMONIC vs. DIGITAL ATTENUATOR STATE



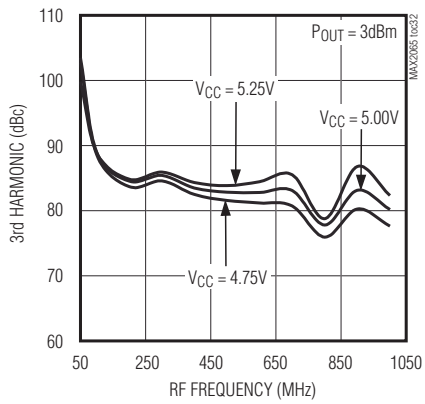
2nd HARMONIC vs. ANALOG ATTENUATOR STATE



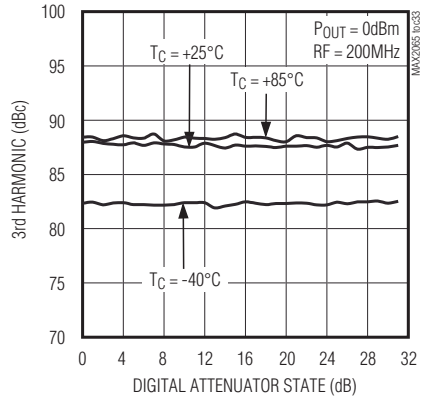
3rd HARMONIC vs. RF FREQUENCY



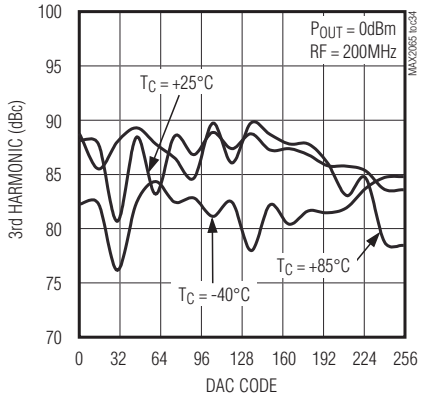
3rd HARMONIC vs. RF FREQUENCY



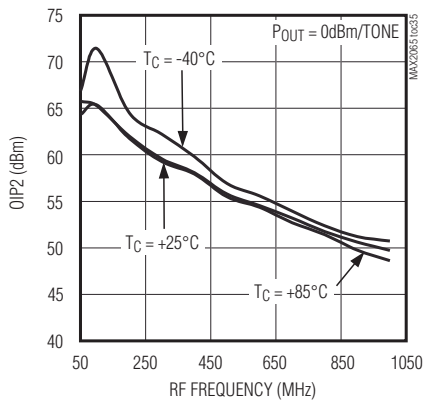
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE



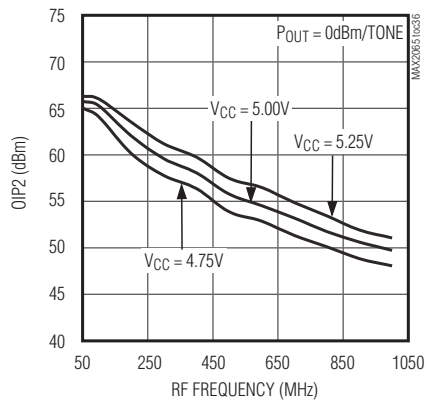
3rd HARMONIC vs. ANALOG ATTENUATOR STATE



OIP2 vs. RF FREQUENCY



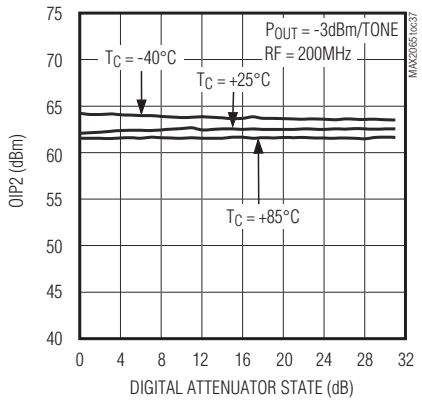
OIP2 vs. RF FREQUENCY



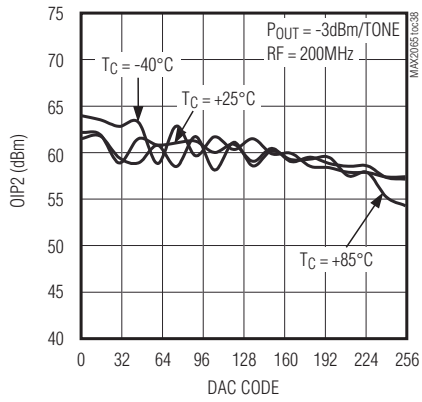
典型工作特性(续)

(**V_{CC} = +5.0V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

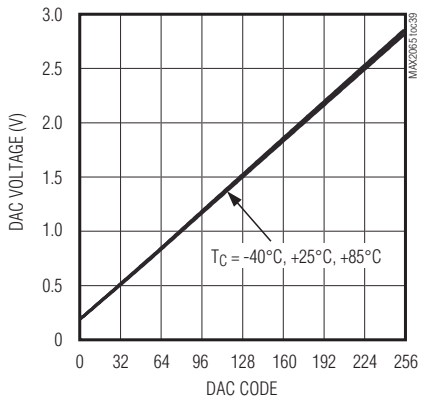
OIP2 vs. DIGITAL ATTENUATOR STATE



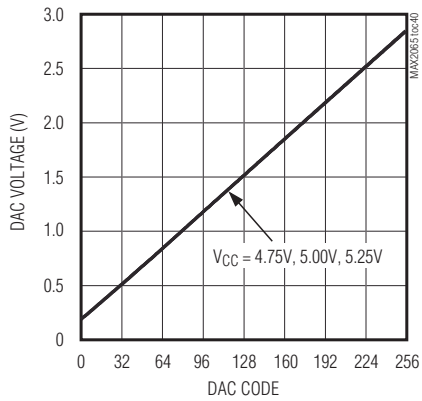
OIP2 vs. ANALOG ATTENUATOR STATE



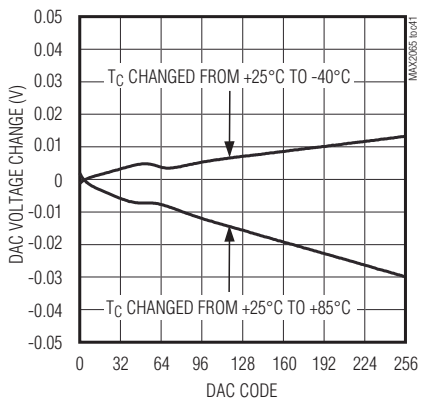
DAC VOLTAGE vs. DAC CODE



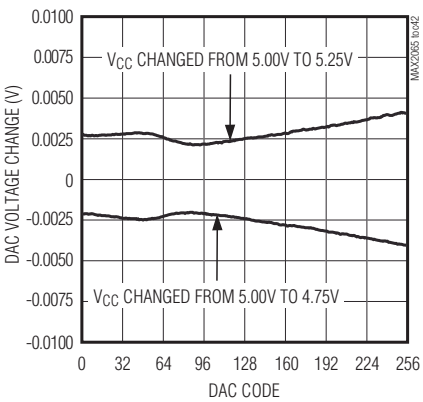
DAC VOLTAGE vs. DAC CODE



DAC VOLTAGE DRIFT vs. DAC CODE



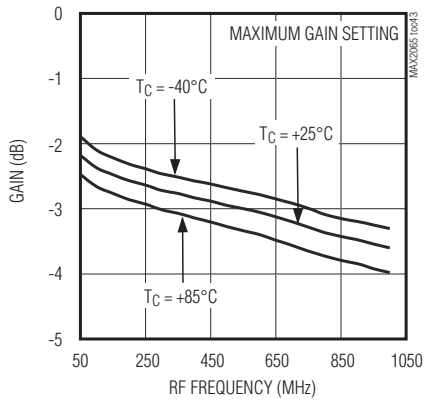
DAC VOLTAGE DRIFT vs. DAC CODE



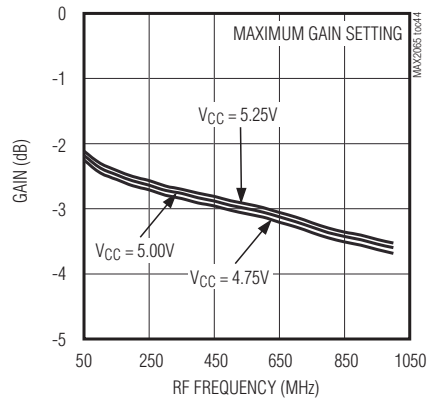
典型工作特性(续)

(**V_{CC} = +5.0V, attenuator only**, maximum gain, P_{IN} = -20dBm and T_C = +25°C, unless otherwise noted.)

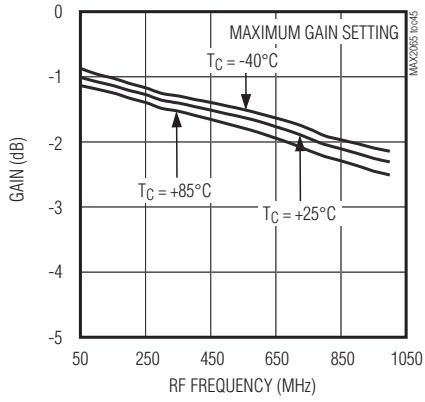
GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)



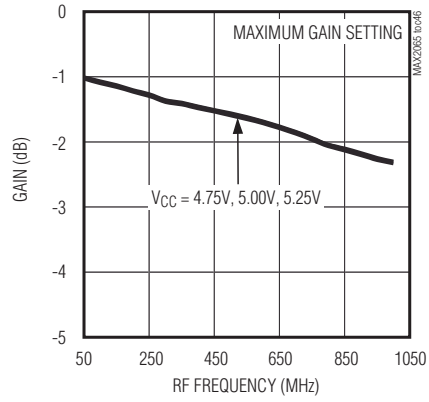
GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)



GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)

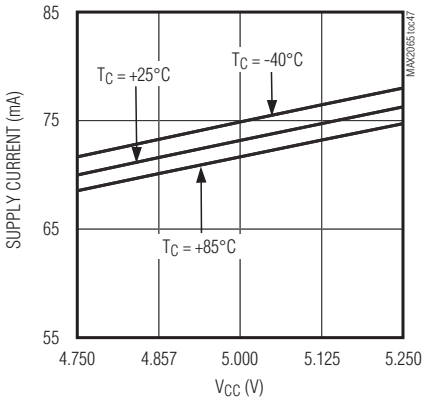


50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

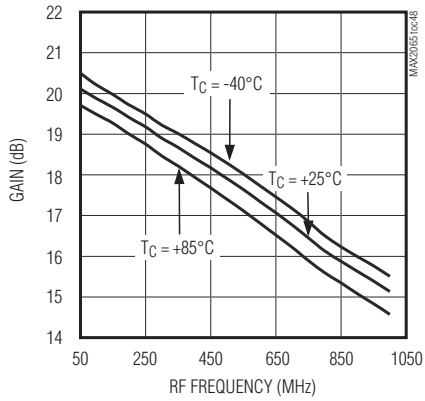
典型工作特性(续)

(**V_{CC} = +5.0V, LC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

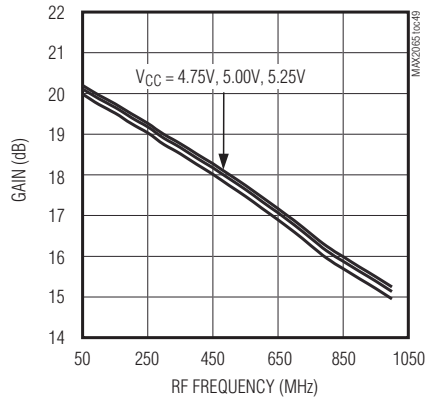
SUPPLY CURRENT vs. V_{CC} (LOW CURRENT MODE)



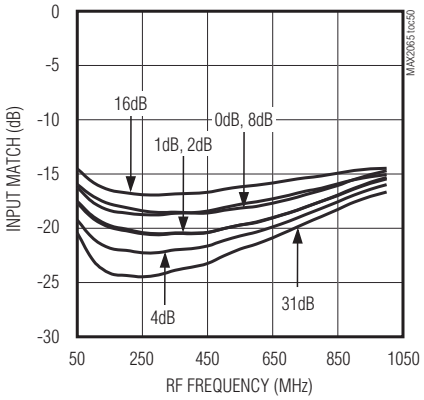
GAIN vs. RF FREQUENCY (LOW CURRENT MODE)



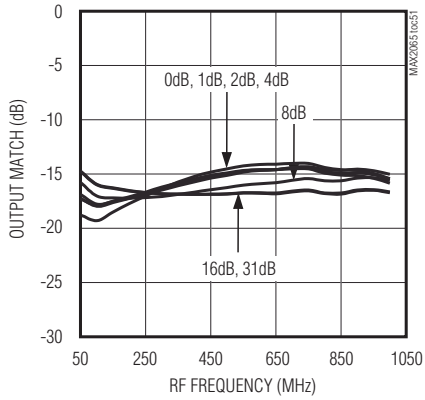
GAIN vs. RF FREQUENCY (LOW CURRENT MODE)



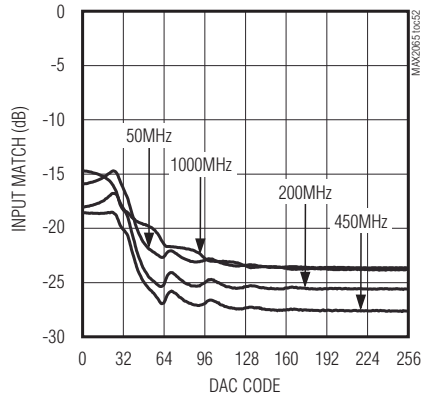
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



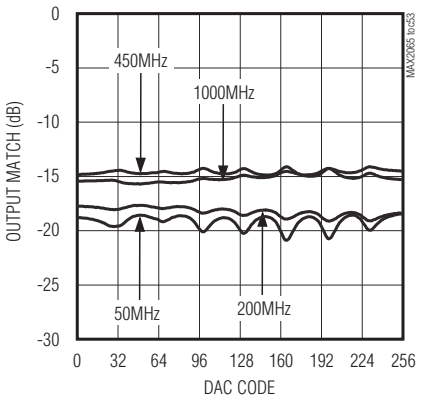
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



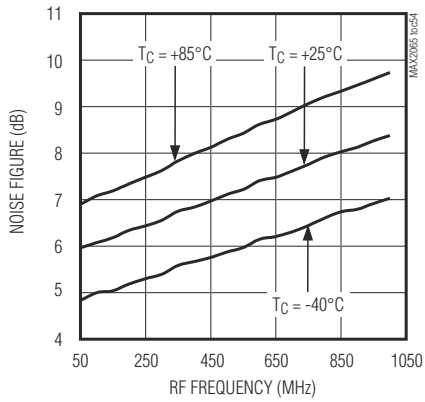
INPUT MATCH vs. ANALOG ATTENUATOR SETTING (LOW CURRENT MODE)



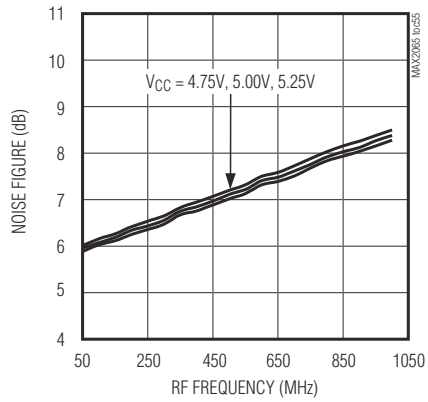
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING (LOW CURRENT MODE)



NOISE FIGURE vs. RF FREQUENCY (LOW CURRENT MODE)



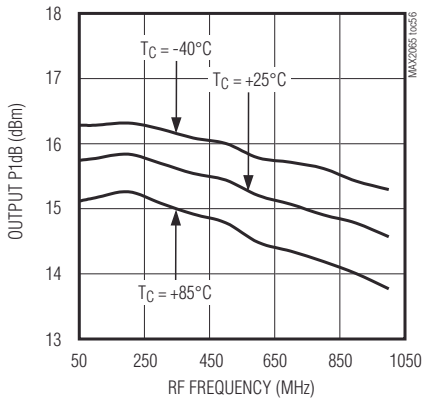
NOISE FIGURE vs. RF FREQUENCY (LOW CURRENT MODE)



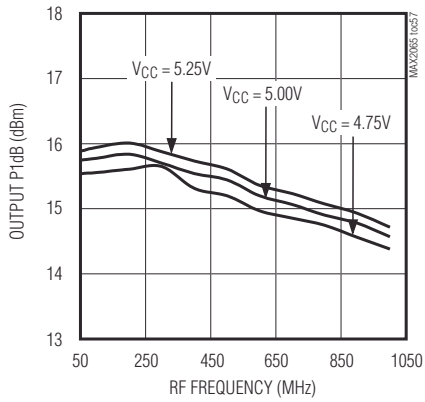
典型工作特性(续)

(**V_{CC} = +5.0V, LC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

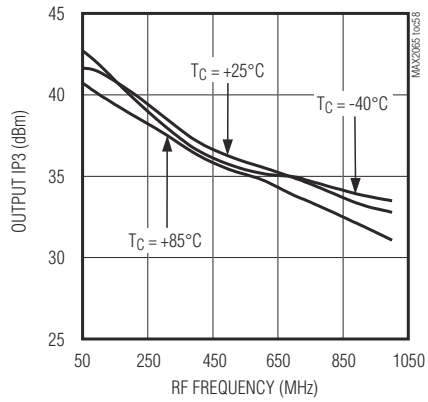
OUTPUT P1dB vs. RF FREQUENCY (LOW CURRENT MODE)



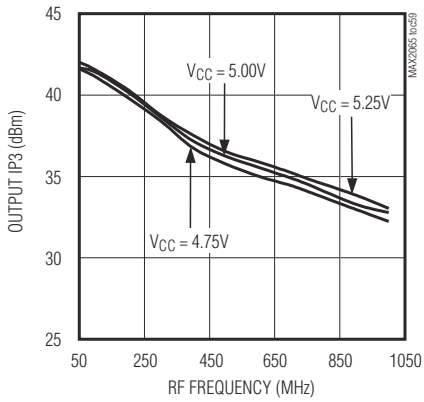
OUTPUT P1dB vs. RF FREQUENCY (LOW CURRENT MODE)



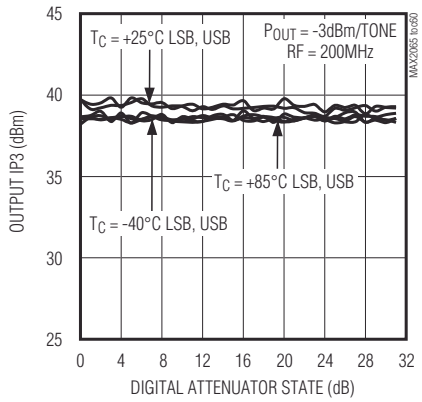
OUTPUT IP3 vs. RF FREQUENCY (LOW CURRENT MODE)



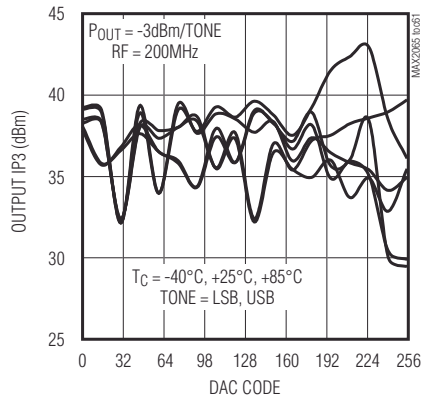
OUTPUT IP3 vs. RF FREQUENCY (LOW CURRENT MODE)



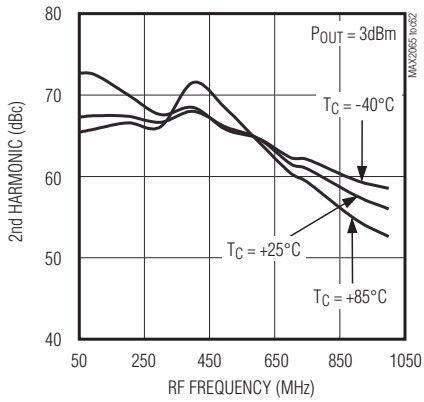
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



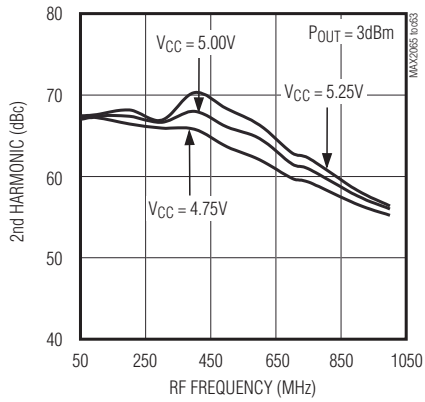
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



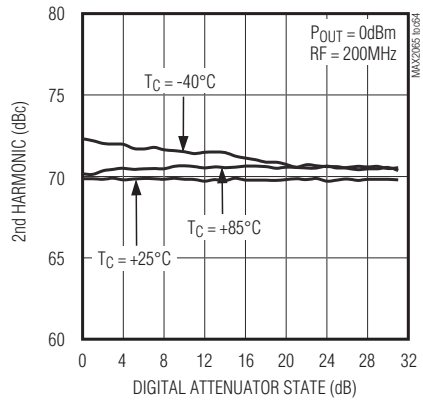
2nd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



2nd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



2nd HARMONIC vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)

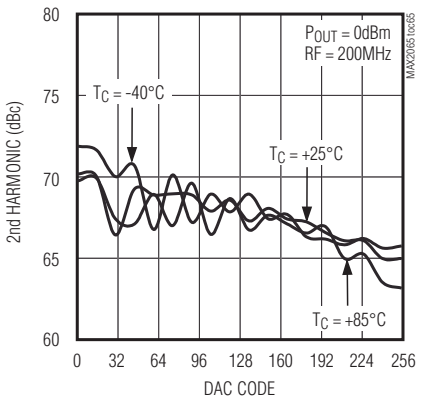


50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

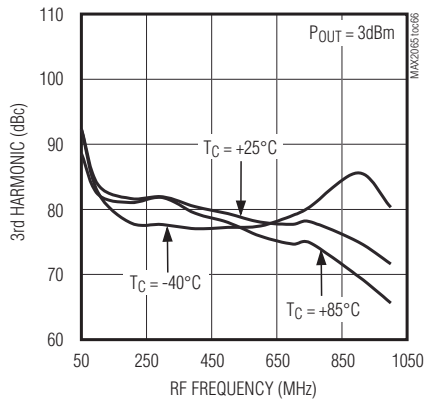
典型工作特性(续)

(**VCC = +5.0V, LC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal reference used, unless otherwise noted.)

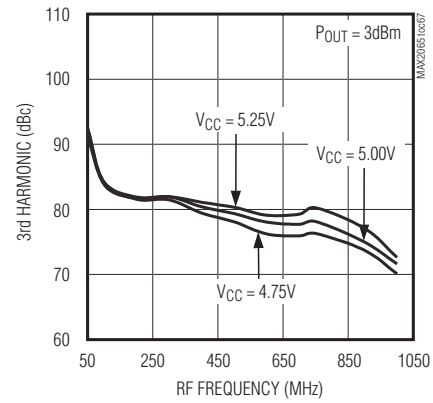
2nd HARMONIC vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



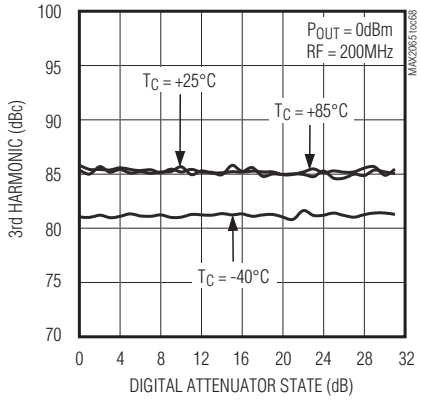
3rd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



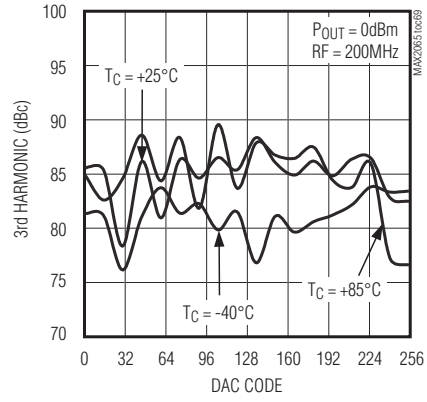
3rd HARMONIC vs. RF FREQUENCY (LOW CURRENT MODE)



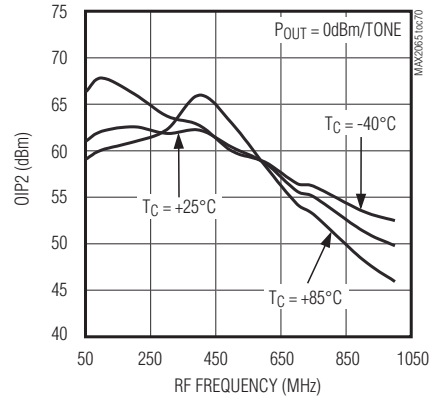
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



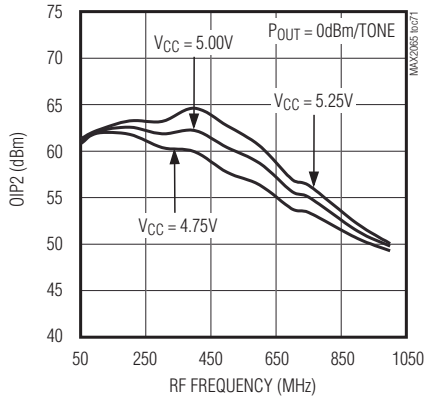
3rd HARMONIC vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



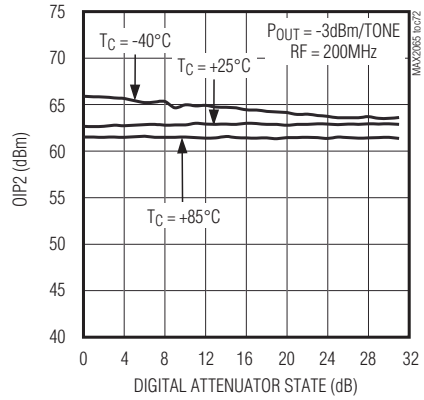
OIP2 vs. RF FREQUENCY (LOW CURRENT MODE)



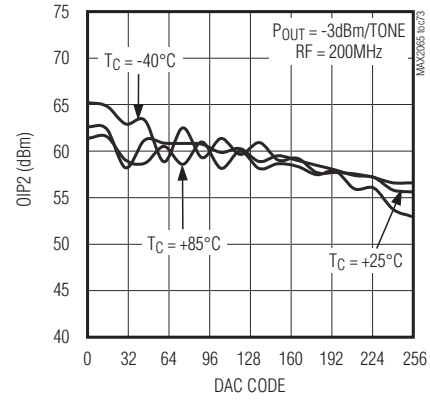
OIP2 vs. RF FREQUENCY (LOW CURRENT MODE)



OIP2 vs. DIGITAL ATTENUATOR STATE (LOW CURRENT MODE)



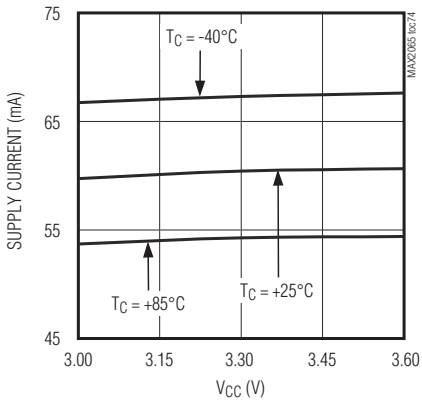
OIP2 vs. ANALOG ATTENUATOR STATE (LOW CURRENT MODE)



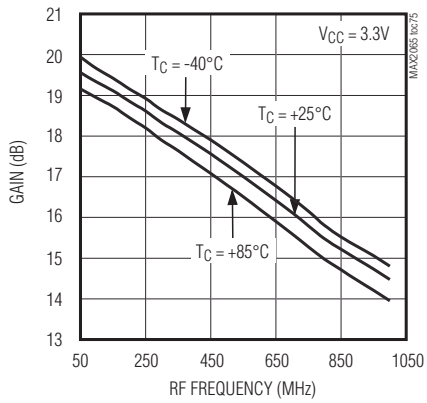
典型工作特性(续)

(**V_{CC} = +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

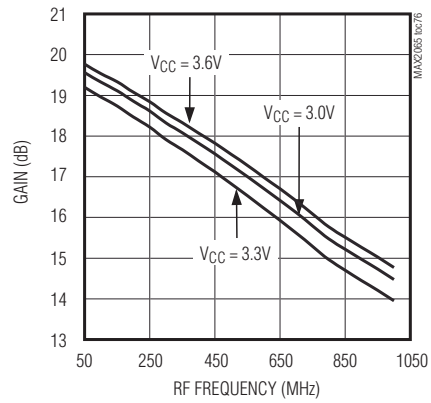
SUPPLY CURRENT vs. V_{CC}



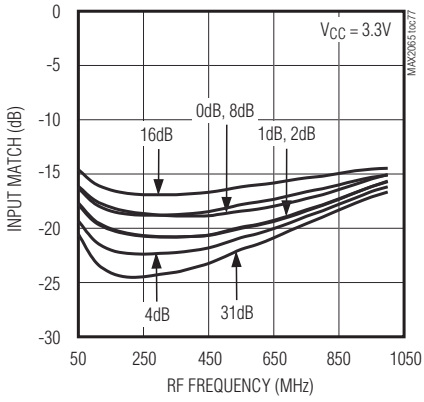
GAIN vs. RF FREQUENCY



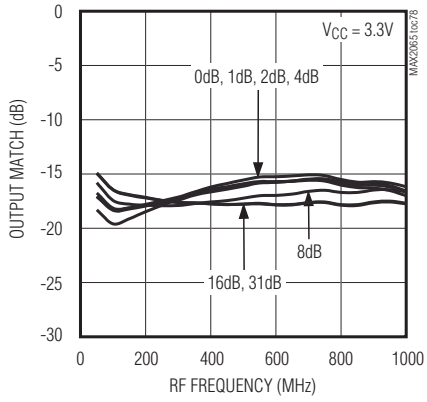
GAIN vs. RF FREQUENCY



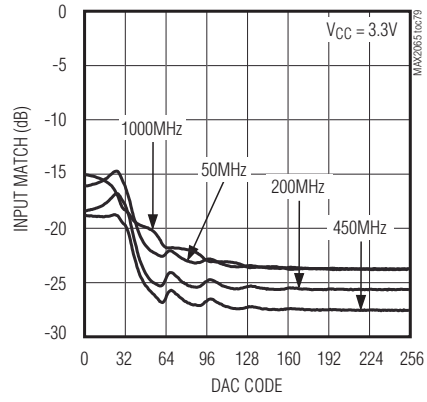
INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



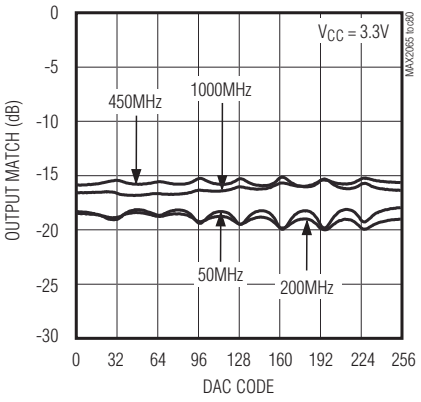
OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY



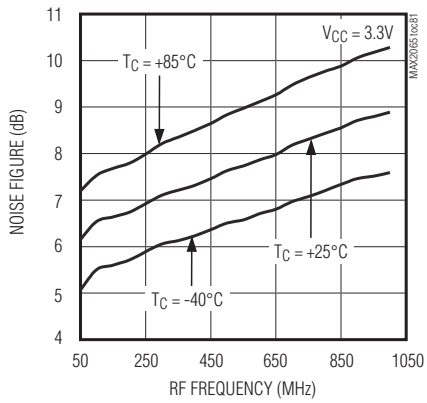
INPUT MATCH vs. ANALOG ATTENUATOR SETTING



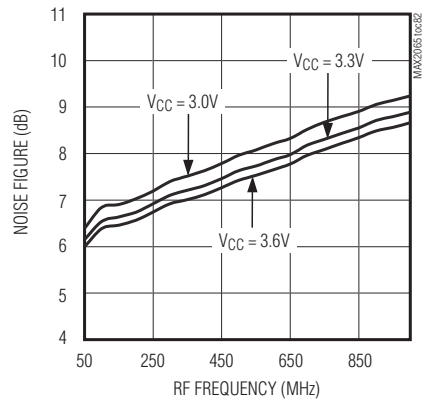
OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING



NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY

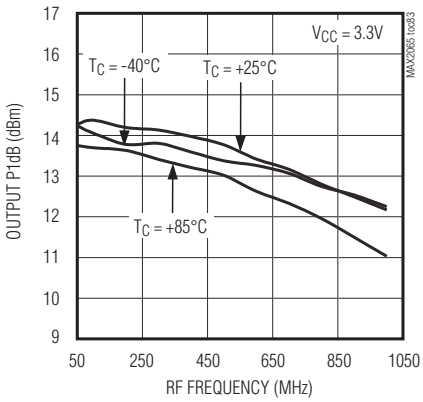


50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

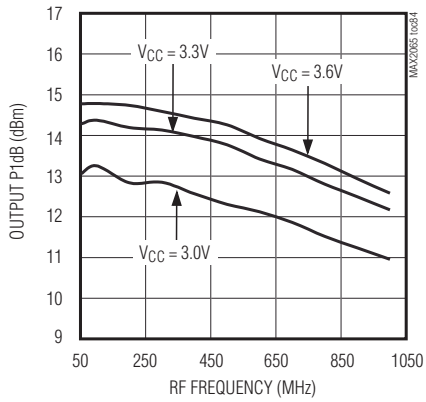
典型工作特性(续)

(**VCC = +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

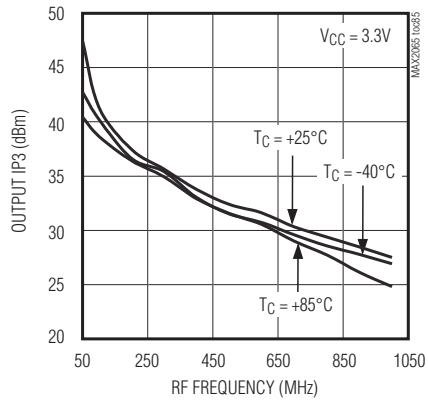
OUTPUT P1dB vs. RF FREQUENCY



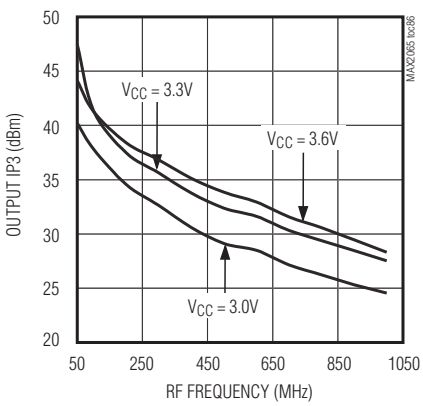
OUTPUT P1dB vs. RF FREQUENCY



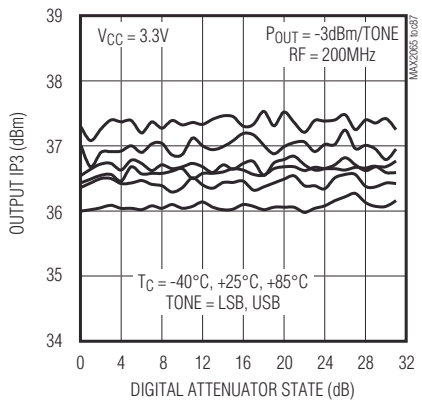
OUTPUT IP3 vs. RF FREQUENCY



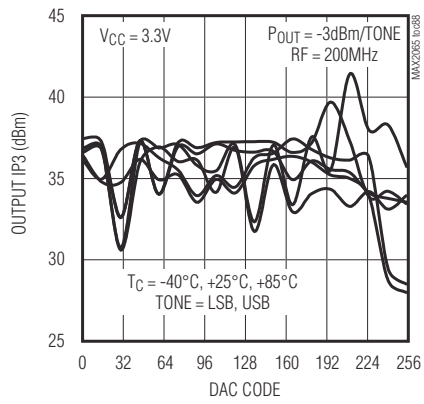
OUTPUT IP3 vs. RF FREQUENCY



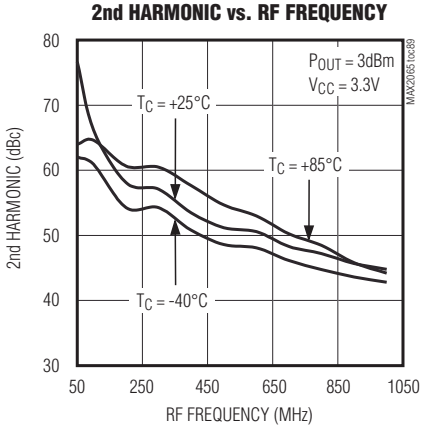
OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE



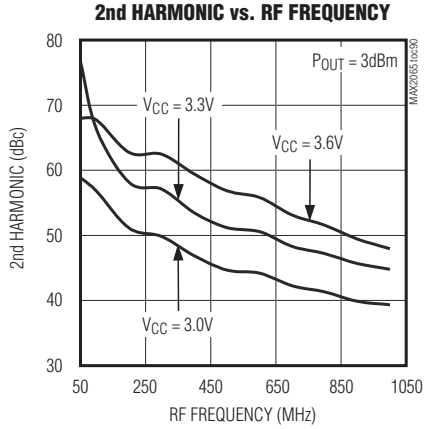
OUTPUT IP3 vs. ANALOG ATTENUATOR STATE



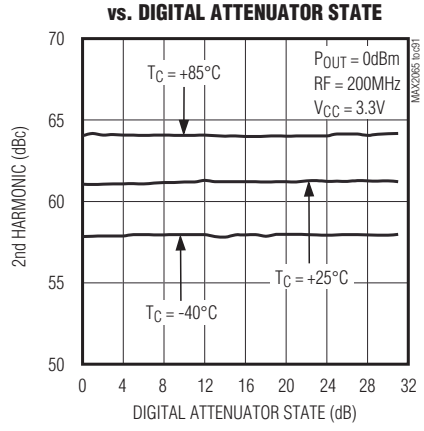
2nd HARMONIC vs. RF FREQUENCY



2nd HARMONIC vs. RF FREQUENCY



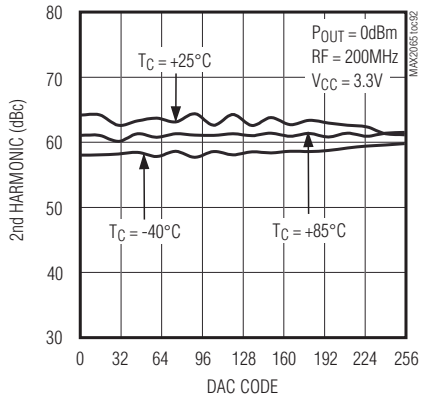
2nd HARMONIC vs. DIGITAL ATTENUATOR STATE



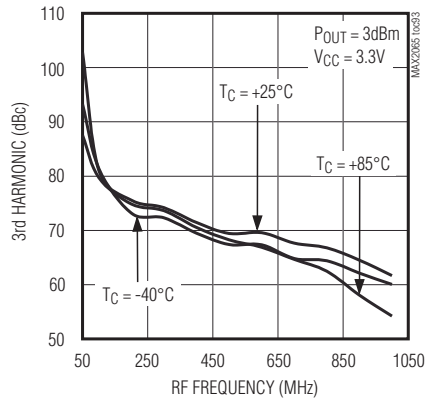
典型工作特性(续)

(**V_{CC} = +3.3V, HC mode**, both attenuators set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

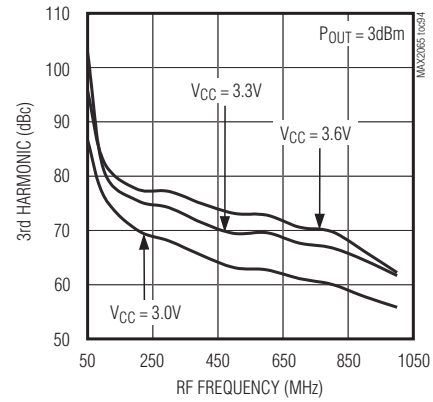
2nd HARMONIC vs. ANALOG ATTENUATOR STATE



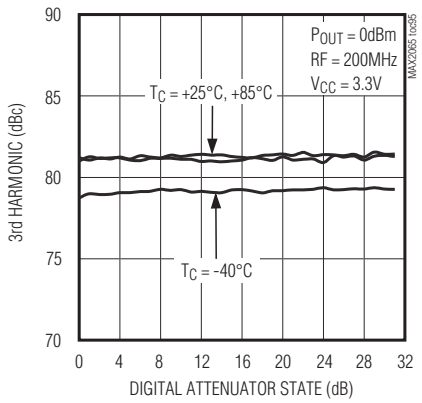
3rd HARMONIC vs. RF FREQUENCY



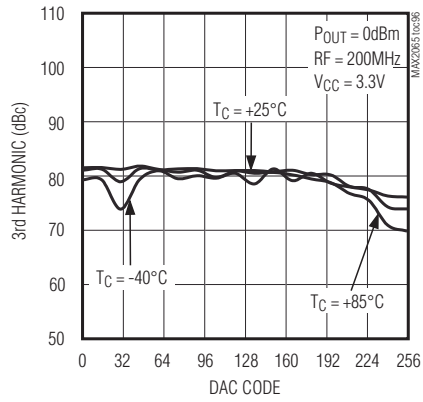
3rd HARMONIC vs. RF FREQUENCY



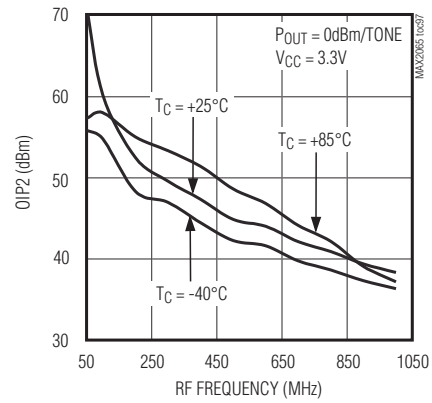
3rd HARMONIC vs. DIGITAL ATTENUATOR STATE



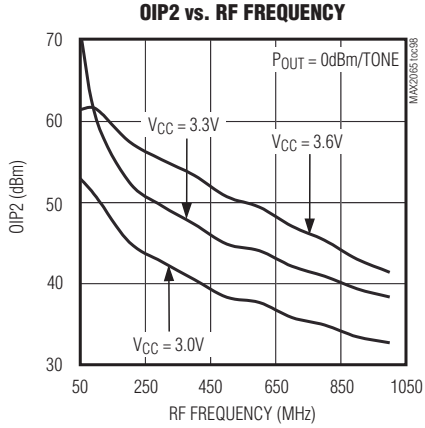
3rd HARMONIC vs. ANALOG ATTENUATOR STATE



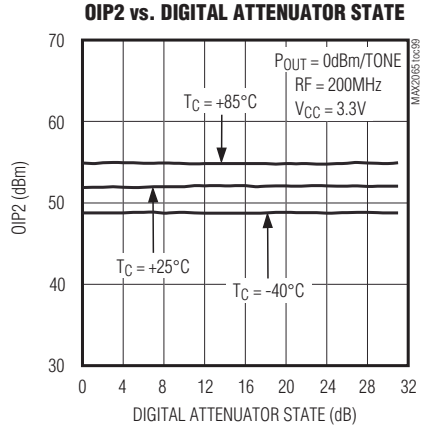
OIP2 vs. RF FREQUENCY



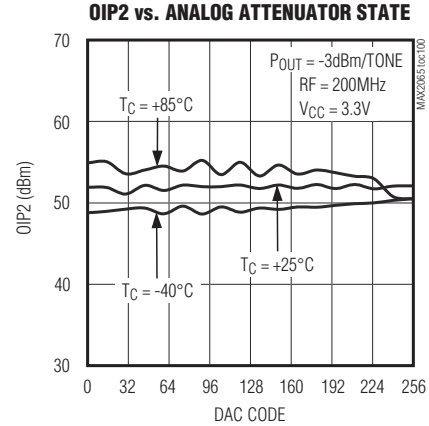
OIP2 vs. RF FREQUENCY



OIP2 vs. DIGITAL ATTENUATOR STATE



OIP2 vs. ANALOG ATTENUATOR STATE



引脚说明

引脚	名称	功能
1, 16, 19, 22, 24–28, 30, 31, 33–36	GND	地。
2	VREF_SELECT	DAC基准电压选择逻辑输入。逻辑1 = 内部DAC基准电压；逻辑0 = 外部DAC基准电压。 当VDAC_EN = 逻辑0时，逻辑输入被禁用(可忽略)。
3	VDAC_EN	DAC使能/关闭控制逻辑输入。逻辑0 = 关闭DAC电路；逻辑1 = 打开DAC电路。
4	DATA	SPI数字数据输入。
5	CLK	SPI数字时钟输入。
6	$\overline{CS}$	SPI数字片选输入。
7	VDD_LOGIC	数字逻辑电路供电输入。
8	SER/PAR	数字衰减器SPI或并行控制选择输入。逻辑0 = 并行控制；逻辑1 = 串行控制。
9	STATE_A	数字衰减器预编程衰减状态逻辑输入。
10	STATE_B	**状态A　　状态B　　数字衰减器** 逻辑电平 = 0　　逻辑电平 = 0　　预编程状态1 逻辑电平 = 1　　逻辑电平 = 0　　预编程状态2 逻辑电平 = 0　　逻辑电平 = 1　　预编程状态3 逻辑电平 = 1　　逻辑电平 = 1　　预编程状态4
11	D4	16dB衰减器逻辑输入。逻辑0 = 关闭；逻辑1 = 使能。
12	D3	8dB衰减器逻辑输入。逻辑0 = 关闭；逻辑1 = 使能。
13	D2	4dB衰减器逻辑输入。逻辑0 = 关闭；逻辑1 = 使能。
14	D1	2dB衰减器逻辑输入。逻辑0 = 关闭；逻辑1 = 使能。
15	D0	1dB衰减器逻辑输入。逻辑0 = 关闭；逻辑1 = 使能。
17	AMP_OUT	放大器驱动输出(50Ω)。
18	RSET	放大器驱动偏置电流设置，请参考*外部偏置*部分。
20	AMP_IN	放大器驱动输入(50Ω)。
21	VCC_AMP	放大器驱动电源输入。
23	ATTEN2_OUT	5位数字衰减器输出(50Ω)。
29	ATTEN2_IN	5位数字衰减器输入(50Ω)。
32	ATTEN1_OUT	模拟衰减器输出(50Ω)。
37	ATTEN1_IN	模拟衰减器输入(50Ω)。
38	VCC_ANALOG	模拟偏置和控制电路电源输入。
39	ANALOG_VCTRL	模拟衰减器控制电压输入。
40	VREF_IN	外部DAC基准电压输入。
—	EP	裸焊盘，内部连接到GND。将EP连接至GND有利于改善RF性能和散热。

50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

详细说明

MAX2065高线性度、模拟/数字可变增益放大器是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω系统接口的应用而设计。

MAX2065集成了一个数字衰减器和一个模拟衰减器可提供62dB的增益控制，同时可优化放大器驱动设计来提供高增益、高IP3、低噪声系数和低功耗指标。在对线性度要求不高的应用中，可通过调节外部电阻改变放大器的偏置电流，以进一步降低功耗。

可通过SPI兼容接口控制作为从机外设的数字衰减器；也允许以1dB步长通过并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择，直接将增益设置在4种选项(用户可通过SPI接口预先设置)的一种。2个控制引脚允许用户快速选择4种定制衰减的任何一个，无需SPI总线编程。利用外部电压或通过SPI接口控制片上8位DAC，实现衰减器的模拟调节。因为三级电路的每一级都具有RF输入和RF输出，通过适当配置可以优化NF (第1级为放大器)、OIP3 (最后一级为放大器)或在NF和OIP3之间进行折衷。该器件还包含具有22dB增益的放大器(放大器本身)，增益最大时NF为6.5dB (包括两个衰减器的插入损耗)，并提供+42dBm的高OIP3。这些特性使得MAX2065能够为众多接收器和发射器提供一个理想的VGA。

另外，MAX2065采用+5V单电源供电，提供功能完备的解决方案；工作在+3.3V时，性能指标略有降低，可调节偏置电流在电流损耗和线性度方面进行折衷。

模拟和5位数字衰减器控制

MAX2065集成了一个模拟衰减器和一个5位数字衰减器，用于实现高动态范围控制。该模拟衰减器具有31dB的动态范围，并可利用外部电压或通过3线串行外设接口(SPI)控制片上8位DAC实现衰减器调节。该数字衰减器具有31dB控制范围，1dB步长，并可通过3线SPI接口设置。请参考*应用信息*和表1所示衰减器设置，获得更多信息。这些衰减器可用于静态和动态功率控制。

驱动器放大器

MAX2065包括一个22dB固定增益的高性能驱动器。该驱动器放大器优化于50MHz至1000MHz频率范围的高线性度指标。

应用信息

SPI接口和衰减器设置

该数字衰减器可采用5位字节通过3线SPI/MICROWIRE™兼容串行接口进行控制。移入28位数据，MSB在前，并通过$\overline{CS}$打包。当$\overline{CS}$为低电平时，时钟有效，数据在时钟的上升沿移入。当$\overline{CS}$跳变到高电平时，数据被锁存，改变衰减器设置(图1)。表2给出了SPI数据格式的详细信息。

表1. 控制逻辑

VDAC_EN	SER/PAR	VREF_SELECT	ANALOG ATTENUATOR	DIGITAL ATTENUATOR	D/A CONVERTER
0	0	X	Controlled by external control voltage	Parallel controlled	Disabled
1	0	1	Controlled by on-chip DAC	Parallel controlled	Enabled (DAC uses on-chip voltage reference)
0	1	X	Controlled by external control voltage	SPI controlled	Disabled
1	1	0	Controlled by on-chip DAC	SPI controlled	Enabled (DAC uses external voltage reference)

X = 无关。

MICROWIRE是National Semiconductor Corp.的商标。

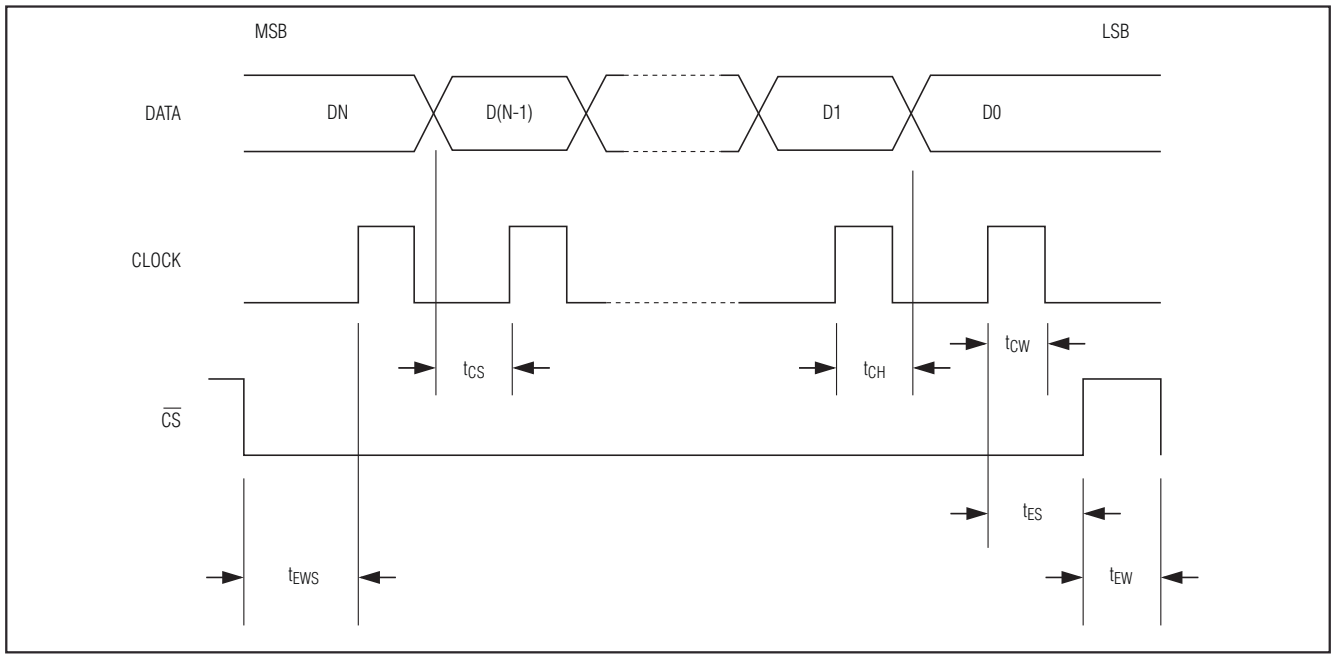


图1. MAX2065 SPI时序图

表2. SPI数据格式

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 4	D27 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step (LSB)
Digital Attenuator State 3	D22	5-bit word used to program the digital attenuator state 3 (see the description for digital attenuator state 4)
	D21	
	D20	
	D19	
	D18	
Digital Attenuator State 2	D17	5-bit word used to program the digital attenuator state 2 (see the description for digital attenuator state 4)
	D16	
	D15	
	D14	
	D13	
Digital Attenuator State 1	D12	5-bit word used to program the digital attenuator state 1 (see the description for digital attenuator state 4)
	D11	
	D10	
	D9	
	D8	

表2. SPI数据格式(续)

FUNCTION	BIT	DESCRIPTION
On-Chip DAC	D7	Bit 7 (MSB) of on-chip DAC used to program the analog attenuator
	D6	Bit 6 of DAC
	D5	Bit 5 of DAC
	D4	Bit 4 of DAC
	D3	Bit 3 of DAC
	D2	Bit 2 of DAC
	D1	Bit 1 of DAC
	D0 (LSB)	Bit 0 (LSB) of the on-chip DAC

衰减器和DAC操作

在ANALOG_VCTRL (第39引脚)施加一个外部控制电压或通过片上8位DAC控制模拟衰减器，也可以通过SPI兼容接口或并行总线控制数字衰减器。DAC使能/禁止逻辑输入引脚(VDAC_EN)、数字衰减器SPI或并行控制选择逻辑输入(SER/PAR)以及DAC基准电压选择逻辑输入引脚(VREF_SELECT)决定以何种方式控制这些衰减器。可以使能或禁止片上DAC，当DAC使能时，允许选择内部基准或外部基准。请参考表1所示衰减器和DAC工作真值表。

利用并行控制总线设置数字衰减器

为了达到25ns的快速切换能力，MAX2065提供一个辅助的5位并行控制接口。这些数字逻辑衰减器控制引脚(D0–D4)用于设置衰减器的工作状态(表3)。

直接访问5位总线可以使用户省去SPI接口的编程延时。任何SPI总线的速率都受限于指令逐位传递到外围器件的时间。通过直接访问5位并行接口，用户可以在“快速建立”自动增益控制(AGC)应用中实现数字衰减状态的迅速切换。

“速射”预编程衰减状态

MAX2065能够在4个预置衰减等级之间提供“速射”增益选择。与上述辅助5位总线类似，“速射”增益选择能够快速进入4个预先设定的数字衰减状态的任意一个，消除了通过SPI总线进行设置的相关延时。

这种方式的切换速度与采用辅助5位并行总线的速度相当。但这一特殊功能可以使衰减器的数字控制I/O降低5倍或2.5倍(5个控制位相比于1个或2个控制位)，具体取决于所要求的状态数。

表3. 数字衰减器设置(并行控制)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0	Disable 1dB attenuator, or when SPI is default programmer	Enable 1dB attenuator
D1	Disable 2dB attenuator, or when SPI is default programmer	Enable 2dB attenuator
D2	Disable 4dB attenuator, or when SPI is default programmer	Enable 4dB attenuator
D3	Disable 8dB attenuator, or when SPI is default programmer	Enable 8dB attenuator
D4	Disable 16dB attenuator, or when SPI is default programmer	Enable 16dB attenuator

50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

用户可通过STATE_A和STATE_B输入引脚设置所要求的状态(表4)。利用STATE_A引脚(1个控制位)可以得到2个预先设定的衰减状态，同时使用STATE_A和STATE_B引脚(2个控制位)，可以得到4个预先设定的衰减状态。

例如，假设AGC应用需要静态调节衰减器，以调整接收器增益。该AGC电路还需要对可能引起接收器灵敏度下降以及ADC过驱动的干扰信号进行动态衰减。该实例中，MAX2065可以预先设置(通过SPI总线) 2种衰减状态：一个状态用于处理静态增益调节，另一个状态用于处理干扰信号。用户只需要对一个I/O引脚(即STATE_A)进行控制，即可在静态和动态衰减控制之间快速切换。

表4. 预编程衰减状态设置

STATE_A	STATE_B	DIGITAL ATTENUATOR
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

需要时，用户还可以使用第二个I/O引脚，即STATE_B控制引脚，设置另外2个衰减状态。这两个附加的衰减设置非常适合软件定义的无线通信装置，这些装置往往需要多个静态增益设置，以满足不同工作频率的要求；也需要多个动态衰减设置以处理不同阻塞电平(由多个无线通信标准定义)。

串联OIP3

考虑到两个衰减器的有限IP3指标，当两个衰减器都设置在较高的衰减等级时，将会劣化串联OIP3。

外部偏置

驱动放大器偏置电流可通过外部电阻设置并进行优化。将电阻R1和R1A连接到RSET (引脚18)，可以设置放大器的偏置电流。增大外部偏置电阻可降低工作电流，代价是降低系统性能。

表5. 典型应用电路元件值(HC模式)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C11	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9, C10	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
C12, C13	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1, R1A	10Ω	0402	Panasonic Corp.	1%
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2065ETL+

表6. 典型应用电路元件值(LC模式)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C11	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9, C10	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
C12, C13	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitor
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1	24Ω	0402	Vishay	1%
R1A	0.01µF	0402	Murata Mfg. Co., Ltd.	X7R
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2065ETL+

+5V和+3.3V供电

MAX2065的另外一个供电选择是采用+3.3V供电，但在这种情况下系统的线性指标略有下降。

布局考虑

MAX2065经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。

MAX2065采用40引脚薄型QFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装MAX2065的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP**必须**直接或通过一系列过孔焊接到PCB的地层。

过冲幅度衰减

为降低数字衰减器状态变化时产生的过冲，需要在ATTEN2_OUT (引脚23)和地之间连接一个带通滤波器(并联LC)。工作在169MHz频率时，推荐使用L = 18nH，C = 47pF (图2)。关于其它工作频率的推荐元件，请与工厂联系。

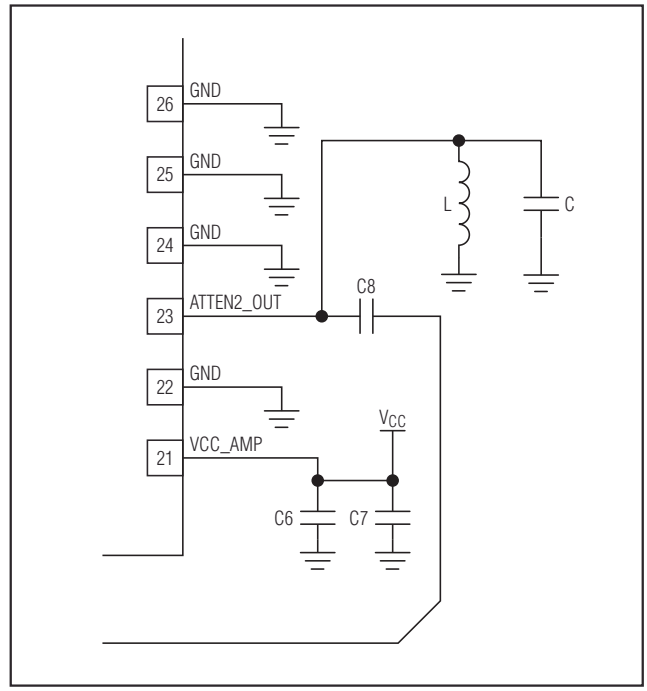
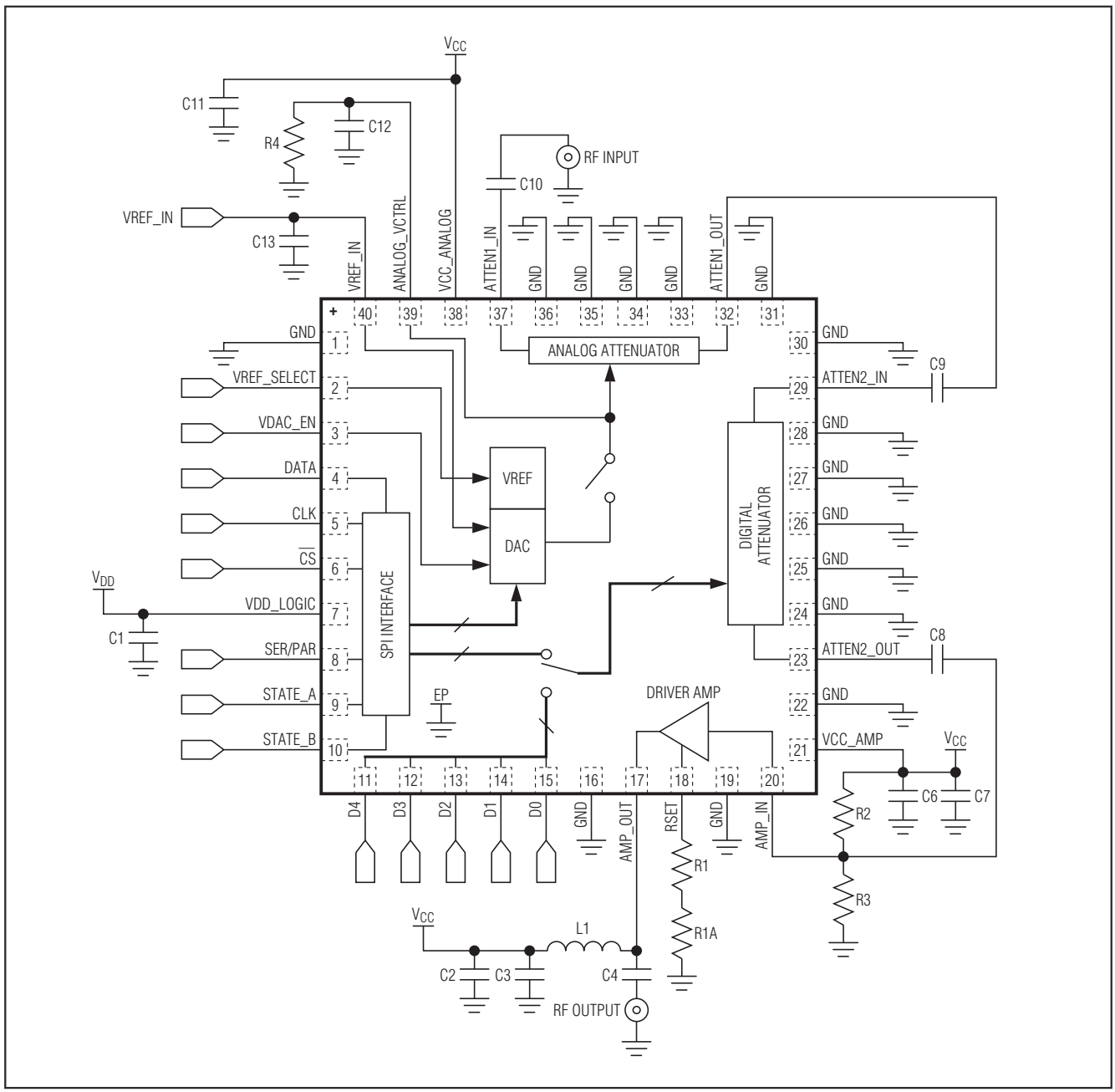
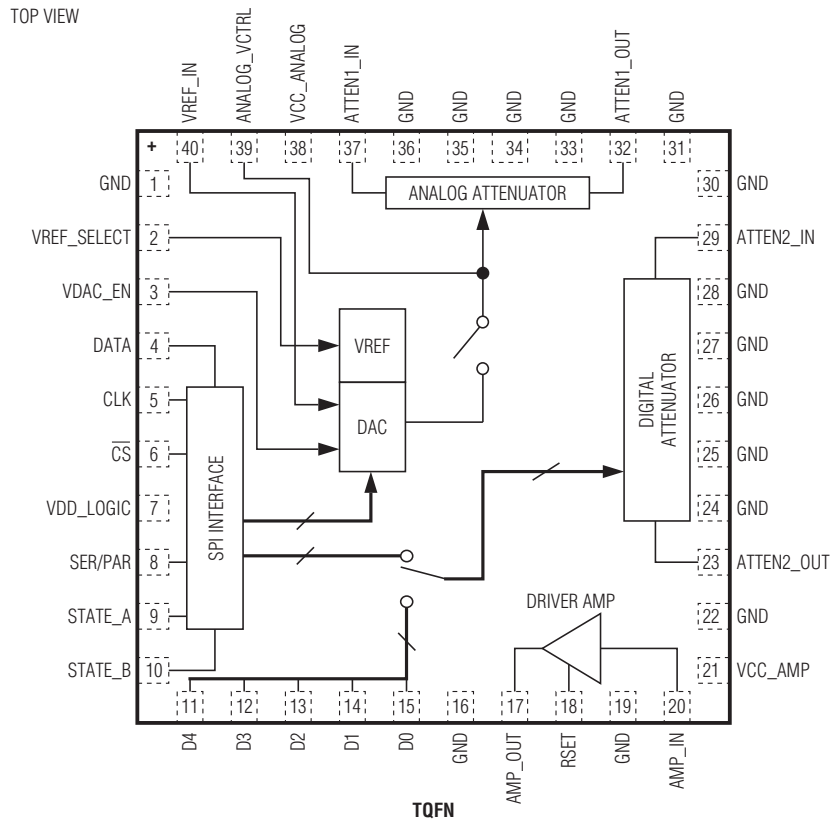


图2. 带通滤波器降低过冲幅度

典型应用电路


VCC
C11
R4
C12
RF INPUT
C10
VREF_IN
C13
VREF_IN
ANALOG_VCTRL
VCC_ANALOG
ATTEN1_IN
GND
GND
GND
GND
ATTEN1_OUT
GND
40
39
38
37
36
35
34
33
32
31
GND
1
ANALOG ATTENUATOR
30
GND
C9
VREF_SELECT
2
29
ATTEN2_IN
VDAC_EN
3
28
GND
DATA
4
VREF
27
GND
CLK
5
DAC
26
GND
CS
6
DIGITAL ATTENUATOR
25
GND
VDD
VDD_LOGIC
7
SPI INTERFACE
24
GND
C8
C1
SER/PAR
8
23
ATTEN2_OUT
STATE_A
9
EP
DRIVER AMP
22
GND
STATE_B
10
21
VCC_AMP
VCC
11
12
13
14
15
16
17
18
19
20
C6
C7
R2
D4
D3
D2
D1
D0
GND
AMP_OUT
RSET
GND
AMP_IN
R1
R3
VCC
L1
R1A
C2
C3
C4
RF OUTPUT

引脚配置/功能框图



芯片信息

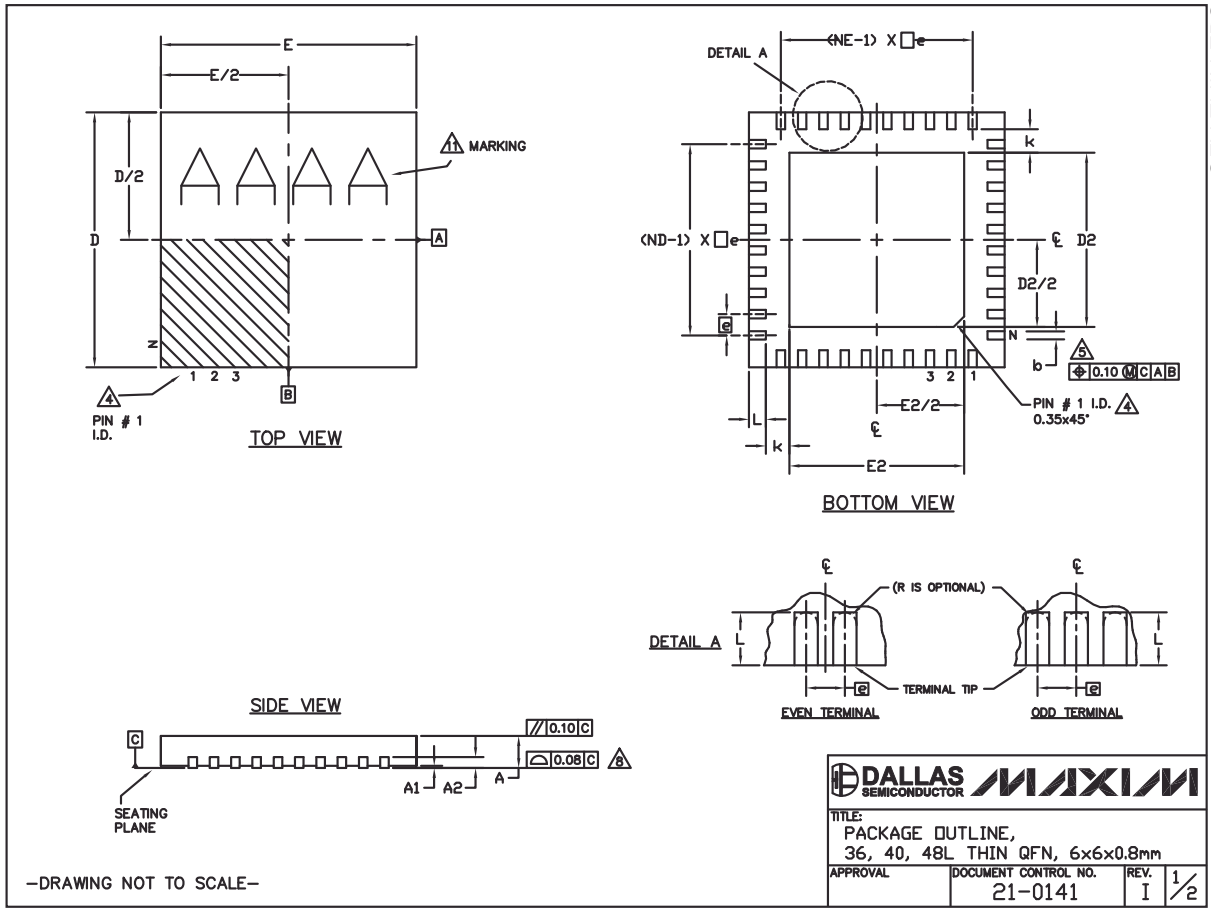
PROCESS: SiGe BiCMOS

50MHz至1000MHz高线性度、可串行/并行控制的模拟/数字VGA

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

QFN THIN.EPS



封装信息(续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	I	2/2

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