

Precision, High Speed, JFET Input Operational Amplifier

DESCRIPTION

The [RH1056A](#) JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/ μ s slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with off-set voltage of typically 50 μ V, 1.2 μ V/ $^{\circ}$ C drift, bias currents of 40pA at 70 $^{\circ}$ C.

The wafer lots are processed to LTC's in-house Class S flow to yield circuits usable in stringent military applications.

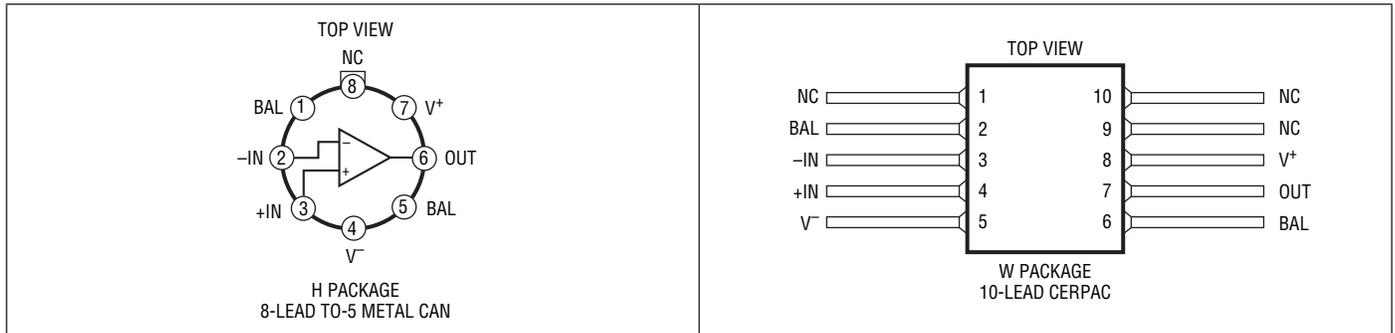
ABSOLUTE MAXIMUM RATINGS

(Note 1)

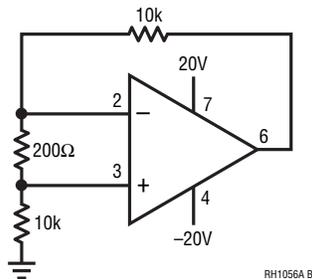
Supply Voltage	± 20 V
Differential Input Voltage	± 40 V
Input Voltage.....	± 20 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	-55° C to 125° C
Storage Temperature Range	-65° C to 150° C
Lead Temperature (Soldering, 10 sec).....	300° C

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PACKAGE INFORMATION



BURN-IN CIRCUIT



RH1056A BI

TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	RH1056AMW	2			300	4			900	2, 3	μV
		RH1056AMH				300				1100		μV
I_{OS}	Input Offset Current	Fully Warmed Up $T_A = 125^\circ\text{C}$	4 4			10	1			1.5	2	pA nA
I_B	Input Bias Current	Fully Warmed Up $T_A = 125^\circ\text{C}$	4			50	1			3.0	2	pA nA
R_{IN}	Input Resistance					10^{12}						Ω
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$		150			4	40			5,6	V/mV
		$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 1\text{k}$		130			4					V/mV
V_O	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 2\text{k}$				± 12	4	± 12			5,6	V
V_{CM}	Input Common Mode Voltage Range	$V_S = \pm 15\text{V}$				± 11	1	± 11			2,3	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$ $V_{CM} = \pm 10.5\text{V}$		86			1		85		2,3	dB
												dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$ $V_S = \pm 10\text{V}$ to $\pm 17\text{V}$		90			1		88		2,3	dB
												dB
I_S	Supply Current	$V_S = \pm 15\text{V}$				6.5	1					mA
SR	Slew Rate	$A_V = 1$, $V_S = \pm 15\text{V}$		10			7					$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product	$V_S = \pm 15\text{V}$				6.5						MHz
e_n	Input Noise Voltage Density	$V_S = \pm 15\text{V}$, $f = 10\text{Hz}$ $V_S = \pm 15\text{V}$, $f = 1\text{kHz}$				28						$\text{nV}/\sqrt{\text{Hz}}$
						14						$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$V_S = \pm 15\text{V}$, $f = 10\text{Hz}$ $V_S = \pm 15\text{V}$, $f = 1\text{kHz}$				1.8						$\text{fA}/\sqrt{\text{Hz}}$
						1.8						$\text{fA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance					4			4			pF

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si)		20KRAD (Si)		50KRAD (Si)		100KRAD (Si)		200KRAD (Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input Offset Voltage		2		300		300		370		570		870	μV
I_{OS}	Input Offset Current		4		± 10		± 50		± 150		± 250		± 350	pA
I_B	Input Bias Current		4		± 50		± 250		± 500		± 1000		± 2000	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10\text{V}$, $R_L \geq 2\text{k}$ $V_O = \pm 10\text{V}$, $R_L \geq 1\text{k}$		150		150		150		100		75		V/mV
				130		130		130		87		65		V/mV
V_O	Output Voltage Swing	$R_L \geq 2\text{k}$			± 12		± 12		± 12		± 12		± 12	V
V_{CM}	Input Common Mode Voltage Range	$V_S = \pm 15\text{V}$			± 11		± 11		± 11		± 11		± 11	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$		86		86		86		86		86		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$		90		90		90		90		90		dB
I_S	Supply Current			7		7		7		7		7		mA
SR	Slew Rate	$A_V = 1$, $V_S = \pm 15\text{V}$		10		10		9		9		9		$\text{V}/\mu\text{s}$
C_{IN}	Input Capacitance			3(Typ)		3(Typ)		3(Typ)		3(Typ)		3(Typ)		pF

TABLE 1A: ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage. Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power, (b) at $T_A = 25^\circ\text{C}$ only, with the chip heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 3: Unless otherwise stated, $V_S = \pm 15\text{V}$; and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0\text{V}$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + (\theta_{JA} \cdot P_D)$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 5: Unless otherwise stated, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ and $T_A = 25^\circ\text{C}$.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6, 7
Group A Test Requirements (Method 5005)	1,2,3,4,5,6, 7
Group B and D for Class S, and Class C and D for Class B** End Point Electrical Parameters (Method 5005)	1

*PDA applies to subgroup 1. See PDA Test Notes.

**For D3, D4, B5 and B6 V_{OS} Limit as follows

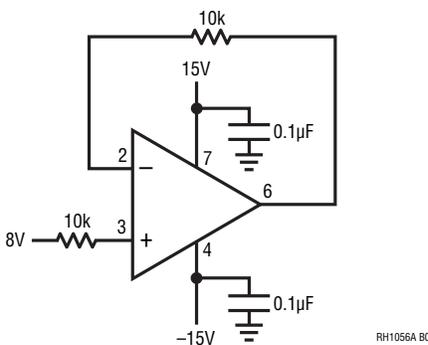
W Package	H Package
500 μV	700 μV

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT



REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	06/18	Corrected parametric units for input noise voltage density	All Pages

TYPICAL PERFORMANCE CHARACTERISTICS

