19-5511; Rev 1; 11/10

MAXIM

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

MAX2062

## 概述

MAX2062高线性度、双通道模拟/数字可变增益放大器(VGA)工作在50MHz至1000MHz频率范围，每通道带有两个独立的衰减器。可通过SPI™兼容接口控制作为从机外设的每路数字衰减器；也允许以1dB步长通过5位并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择功能，直接设置在4种增益选项的一种，用户可通过SPI兼容接口预先设置四种增益选项。2个独立的控制引脚允许用户快速选择4种定制衰减状态的任何一个，无需重新编程SPI总线。每路模拟衰减器采用外部电压或通过SPI兼容接口采用片内8位DAC进行控制。

由于每一级电路都具有各自的RF输入和RF输出，通过适当配置可以优化噪声系数(NF)（放大器配置为第一级）、OIP3(放大器配置为最后一级)或者在NF与OIP3之间进行折中。该器件具有24dB的放大器增益(放大器本身)，增益最大时NF为7.3dB（包括衰减器的插入损耗），并提供+41dBm的高OIP3。这些特性使得该器件成为多通道接收器和发射器应用理想的VGA选择。

此外，器件采用+5V单电源供电时具有最优的性能；工作在+3.3V单电源时，具有先进的省电模式，但性能指标略有降低。器件采用紧凑、带裸焊盘的48引脚TQFN封装(7mm x 7mm)，在扩展级温度范围($T_C$ = -40°C至+85°C)内确保电气特性。

## 应用

IF和RF增益级设计

温度补偿电路

GSM/EDGE基站

WCDMA、TD-SCDMA和cdma2000®基站

WiMAX™、LTE和TD-LTE基站及用户端设备

固定宽带无线接入

无线本地环路

军用系统

## 特性

- ♦ 两个通道可独立控制
- ♦ 50MHz至1000MHz RF频率范围
- ♦ 引脚兼容系列包括
  - MAX2063 (数字VGA)
  - MAX2064 (模拟VGA)
- ♦ 19.4dB (典型值)最大增益
- ♦ 100MHz带宽内保持0.34dB的增益平坦度
- ♦ 64dB增益范围(33dB模拟 + 31dB数字)
- ♦ 56dB通道隔离度(200MHz频率下)
- ♦ 内置8位DAC用于模拟衰减控制
- ♦ 支持4种“速射”预编程衰减状态
  - 快速设置4种定制衰减状态之一
  - 理想用于快速响应和大信号阻塞保护
  - 避免ADC过驱动
- ♦ 优异的线性特性(200MHz频率下，将放大器配置为最后一级)
  - +41dBm OIP3
  - +56dBm OIP2
  - 输出1dB压缩点为+19dBm
- ♦ 7.3dB典型噪声系数(200MHz频率下)
- ♦ 25ns快速数字切换时间
- ♦ 极低的数字VGA摆幅过冲/下冲
- ♦ +5V单电源供电(可选择+3.3V供电)
- ♦ 放大器关断模式支持TDD应用

## 定购信息

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX2062ETM+ | -40°C to +85°C | 48 TQFN-EP* |
| MAX2062ETM+T | -40°C to +85°C | 48 TQFN-EP* |

*+表示无铅(Pb)/符合RoHS标准的封装。*
**EP = 裸焊盘。*
*T = 卷带包装。*

*SPI是Motorola, Inc.的商标。*

*cdma2000是电信工业协会的注册商标。*

*WiMAX是WiMAX论坛的商标。*



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有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maxim-ic.com。

## ABSOLUTE MAXIMUM RATINGS

$V_{CC_AMP_1}$, $V_{CC_AMP_2}$, $V_{CC_RG}$ to GND .....-0.3V to +5.5V
STA_A_1, STA_A_2, STA_B_1, STA_B_2,
PD_1, PD_2, AMPSET to GND .....-0.3V to +3.6V
A_VCTL_1, A_VCTL_2 to GND .....-0.3V to +3.6V
DAT, $\overline{CS}$, CLK, AA_SP, DA_SP to GND .....-0.3V to +3.6V
D0_1, D1_1, D2_1, D3_1, D4_1, D0_2, D1_2,
D2_2, D3_2, D4_2 to GND .....-0.3V to +3.6V
AMP_IN_1, AMP_IN_2 to GND .....+0.95V to +1.2V
AMP_OUT_1, AMP_OUT_2 to GND .....-0.3V to +5.5V
D_ATT_IN_1, D_ATT_IN_2, D_ATT_OUT_1,
D_ATT_OUT_2 to GND .....0V to +3.6V
A_ATT_IN_1, A_ATT_IN_2, A_ATT_OUT_1,
A_ATT_OUT_2 to GND .....0V to +3.6V
REG_OUT to GND.....-0.3V to +3.6V
RF Input Power (D_ATT_IN_1, D_ATT_IN_2) ..... +20dBm
RF Input Power (A_ATT_IN_1, A_ATT_IN_2) ..... +20dBm
RF Input Power (AMP_IN_1, AMP_IN_2)..... +18dBm
$\theta_{JC}$ (Notes 1, 2)..... +12.3°C/W
$\theta_{JA}$ (Notes 2, 3)..... +38°C/W
Continuous Power Dissipation (Note 1) .....5.3W
Operating Case Temperature Range (Note 4) .. -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**Note 1:** Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

**Note 3:** Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

**Note 4:** $T_C$ is the temperature on the exposed pad of the package. $T_A$ is the ambient temperature of the device and PCB.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## 5.0V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = 4.75V to 5.25V, AMPSET = 0, PD_1 = PD_2 = 0, $T_C$ = -40°C to +85°C. Typical values are at $V_{CC_}$ = 5.0V and $T_C$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| Supply Current | $I_{DC}$ | | | 148 | 210 | mA |
| Power-Down Current | $I_{DCPD}$ | PD_1 = PD_2 = 1, $V_{IH}$ = 3.3V | | 5.3 | 8 | mA |
| Logic-Low Input Voltage | $V_{IL}$ | | | | 0.5 | V |
| Logic-High Input Voltage | $V_{IH}$ | | 1.7 | | 3.465 | V |
| Input Logic Current | $I_{IH}$, $I_{IL}$ | | -1 | | +1 | µA |

## 3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{CC_AMP_1} = V_{CC_AMP_2} = V_{CC_RG}$ = 3.135V to 3.465V, AMPSET = 1, PD_1 = PD_2 = 0, $T_C$ = -40°C to +85°C. Typical values are at $V_{CC_}$ = 3.3V and $T_C$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 3.135 | 3.3 | 3.465 | V |
| Supply Current | $I_{DC}$ | | | 87 | 145 | mA |
| Power-Down Current | $I_{DCPD}$ | PD_1 = PD_2 = 1, $V_{IH}$ = 3.3V | | 4.5 | 8 | mA |
| Logic-Low Input Voltage | $V_{IL}$ | | | 0.5 | | V |
| Logic-High Input Voltage | $V_{IH}$ | | | 1.7 | | V |

## RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| RF Frequency | $f_{RF}$ | (Note 5) | 50 | | 1000 | MHz |

## 5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted)

(*Typical Application Circuit*, $V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ $f_{RF}$ ≤ 500MHz, $T_C$ = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = 5.0V, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Small-Signal Gain | G | $f_{RF}$ = 50MHz | | 20.3 | | dB |
| | | $f_{RF}$ = 100MHz | | 19.9 | | |
| | | $f_{RF}$ = 200MHz | | 19.4 | | |
| | | $f_{RF}$ = 350MHz, $T_C$ = +25°C | 17.0 | 18.9 | 21.0 | |
| | | $f_{RF}$ = 450MHz | | 18.6 | | |
| | | $f_{RF}$ = 750MHz | | 17.8 | | |
| | | $f_{RF}$ = 900MHz | | 16.5 | | |
| Gain vs. Temperature | | | | -0.01 | | dB/°C |
| Gain Flatness vs. Frequency | | From 100MHz to 200MHz | | 0.5 | | dB |
| | | Any 100MHz frequency band from 200MHz to 500MHz | | 0.34 | | |
| Noise Figure | NF | $f_{RF}$ = 50MHz | | 6.4 | | dB |
| | | $f_{RF}$ = 100MHz | | 6.8 | | |
| | | $f_{RF}$ = 200MHz | | 7.3 | | |
| | | $f_{RF}$ = 350MHz | | 7.6 | | |
| | | $f_{RF}$ = 450MHz | | 7.8 | | |
| | | $f_{RF}$ = 750MHz | | 8.7 | | |
| | | $f_{RF}$ = 900MHz | | 9.0 | | |
| Total Attenuation Range | | Analog and digital combined | | 64.1 | | dB |
| Output Second-Order Intercept Point | OIP2 | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$ | | 52.1 | | dBm |
| Path Isolation | | RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω | | 48.6 | | dB |
| | | RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω | | 47.7 | | |
| Output Third-Order Intercept Point | OIP3 | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 50MHz | | 47.5 | | dBm |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 100MHz | | 43.4 | | |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 200MHz | | 41.3 | | |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 350MHz | | 37.4 | | |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 450MHz | | 35.1 | | |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 750MHz | | 28.8 | | |
| | | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz, $f_{RF}$ = 900MHz | | 25.8 | | |
| Output -1dB Compression Point | $P_{1dB}$ | $f_{RF}$ = 350MHz, $T_C$ = +25°C (Note 7) | 17 | 18.8 | | dBm |

## 5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted) (continued)

(*Typical Application Circuit*, $V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ $f_{RF}$ ≤ 500MHz, $T_C$ = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = 5.0V, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Second Harmonic | | $P_{OUT}$ = +3dBm | | | -55.0 | | dBc |
| Third Harmonic | | $P_{OUT}$ = +3dBm | | | -72.7 | | dBc |
| Group Delay | | Includes EV kit PCB delays | | | 1.03 | | ns |
| Amplifier Power-Down Time | | PD_1 or PD_2 from 0 to 1, amplifier DC supply current settles to within 0.1mA | | | 0.5 | | µs |
| Amplifier Power-Up Time | | PD_1 or PD_2 from 1 to 0, amplifier DC supply current settles to within 1% | | | 0.5 | | µs |
| Input Return Loss | $RL_{IN}$ | 50Ω source | | | 16.1 | | dB |
| Output Return Loss | $RL_{OUT}$ | 50Ω load | | | 30.8 | | dB |
| **DIGITAL ATTENUATOR (Each Path, Unless Otherwise Noted)** | | | | | | | |
| Insertion Loss | | | | | 3.0 | | dB |
| Input Second-Order Intercept Point | | $P_{IN1}$ = 0dBm, $P_{IN2}$ = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$ | | | 53.6 | | dBm |
| Input Third-Order Intercept Point | | $P_{IN1}$ = 0dBm, $P_{IN2}$ = 0dBm (minimum attenuation), Δf = 1MHz | | | 41.5 | | dBm |
| Attenuation Range | | $f_{RF}$ = 350MHz, $T_C$ = +25°C, $V_{CC}$ = 5.0V | | 29.5 | 30.9 | | dB |
| Step Size | | | | | 1 | | dB |
| Relative Attenuation Accuracy | | | | | 0.13 | | dB |
| Absolute Attenuation Accuracy | | | | | 0.14 | | dB |
| Insertion Phase Step | | $f_{RF}$ = 170MHz | 0dB to 16dB | | 0 | | Degrees |
| | | | 0dB to 24dB | | 1.1 | | |
| | | | 0dB to 31dB | | 1.2 | | |
| Amplitude Overshoot/Undershoot | | Between any two states | Elapsed time = 15ns | | 1.0 | | dB |
| | | | Elapsed time = 40ns | | 0.05 | | |
| Switching Speed | | RF settled to within ±0.1dB | 31dB to 0dB | | 25 | | ns |
| | | | 0dB to 31dB | | 21 | | |
| Input Return Loss | | 50Ω source | | | 22.0 | | dB |
| Output Return Loss | | 50Ω load | | | 21.9 | | dB |
| **ANALOG ATTENUATOR (Each Path, Unless Otherwise Noted)** | | | | | | | |
| Insertion Loss | | | | | 2.2 | | dB |
| Input Second-Order Intercept Point | | $P_{IN1}$ = 0dBm, $P_{IN2}$ = 0dBm (minimum attenuation), Δf = 1MHz, $f_1 + f_2$ | | | 61.9 | | dBm |
| Input Third-Order Intercept Point | | $P_{IN1}$ = 0dBm, $P_{IN2}$ = 0dBm (minimum attenuation), Δf = 1MHz | | | 37.0 | | dBm |

## 5.0V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted) (continued)

(*Typical Application Circuit*, $V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 4.75V to 5.25V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, 100MHz ≤ $f_{RF}$ ≤ 500MHz, $T_C$ = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = 5.0V, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Attenuation Range | | $f_{RF}$ = 350MHz, $T_C$ = +25°C, $V_{CC}$ = 5.0V | | 29.5 | 33.2 | | dB |
| Gain Control Slope | | Analog control input | | | -13.3 | | dB/V |
| Maximum Gain Control Slope | | Over analog control input range | | | -35.2 | | dB/V |
| Insertion Phase Change | | Over analog control input range | | | 17.6 | | Deg |
| Attenuator Response Time | | RF settled to within ±0.5dB | AA_SP = 0, $V_{A_VCTL__}$ from 2.75V to 0.25V | | 500 | | ns |
| | | | AA_SP = 1, DAC code from 11111111 to 00000000, from $\overline{CS}$ rising edge | | 500 | | |
| | | | AA_SP = 0, $V_{A_VCTL__}$ from 0.25V to 2.75V | | 500 | | |
| | | | AA_SP = 1, DAC code from 00000000 to 11111111, from $\overline{CS}$ rising edge | | 500 | | |
| Group Delay vs. Control Voltage | | Over analog control input from 0.25V to 2.75V | | | -0.34 | | ns |
| Analog Control Input Range | | | | 0.25 | | 2.75 | V |
| Analog Control Input Impedance | | | | | 19.2 | | kΩ |
| Input Return Loss | | 50Ω source | | | 16.1 | | dB |
| Output Return Loss | | 50Ω load | | | 16.8 | | dB |
| **D/A CONVERTER** | | | | | | | |
| Number of Bits | | | | | 8 | | Bits |
| Output Voltage | | DAC code = 00000000 | | | | 0.35 | V |
| | | DAC code = 11111111 | | 2.7 | | | |
| **SERIAL PERIPHERAL INTERFACE (SPI)** | | | | | | | |
| Maximum Clock Speed | | | | | 20 | | MHz |
| Data-to-Clock Setup Time | $t_{CS}$ | | | | 2 | | ns |
| Data-to-Clock Hold Time | $t_{CH}$ | | | | 2.5 | | ns |
| Clock-to-$\overline{CS}$ Setup Time | $t_{ES}$ | | | | 3 | | ns |
| $\overline{CS}$ Positive Pulse Width | $t_{EW}$ | | | | 7 | | ns |
| $\overline{CS}$ Setup Time | $t_{EWS}$ | | | | 3.5 | | ns |
| Clock Pulse Width | $t_{CW}$ | | | | 5 | | ns |

## 3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS (Each Path, Unless Otherwise Noted)

(*Typical Application Circuit*, $V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 3.135V to 3.465V, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, 100MHz ≤ $f_{RF}$ ≤ 500MHz, $T_C$ = -40°C to +85°C. Typical values are at maximum gain setting, $V_{CC_}$ = 3.3V, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Small-Signal Gain | | | | 18.8 | | dB |
| Output Third-Order Intercept Point | OIP3 | $P_{OUT}$ = 0dBm/tone | | 29.4 | | dBm |
| Noise Figure | | | | 7.8 | | dB |
| Total Attenuation Range | | | | 64.1 | | dB |
| Path Isolation | | RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to 50Ω | | 49.1 | | dB |
| | | RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to 50Ω | | 48.0 | | |
| Output -1dB Compression Point | $P_{1dB}$ | (Note 7) | | 13.4 | | dBm |

**Note 5:** Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics* section.

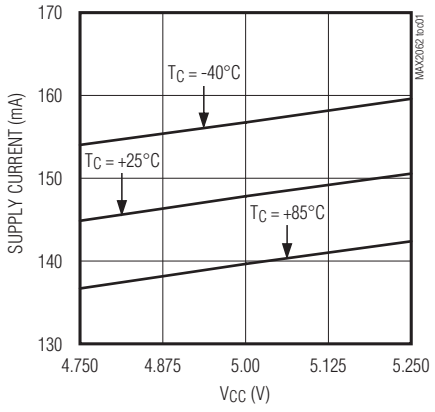
**Note 6:** All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

**Note 7:** It is advisable not to continuously operate the RF input 1 or RF input 2 above +15dBm.

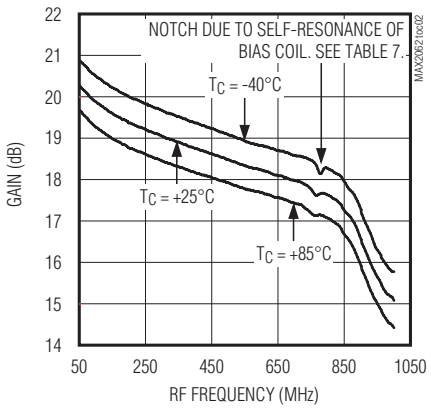
## 典型工作特性

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

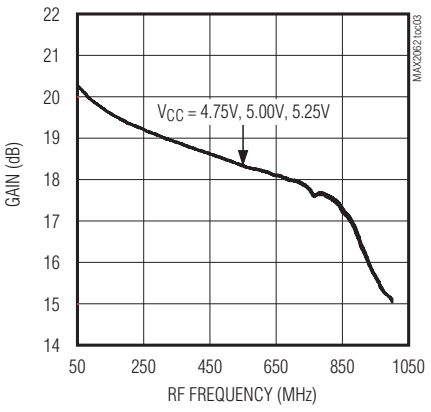
**SUPPLY CURRENT vs. $V_{CC}$**




**GAIN vs. RF FREQUENCY**



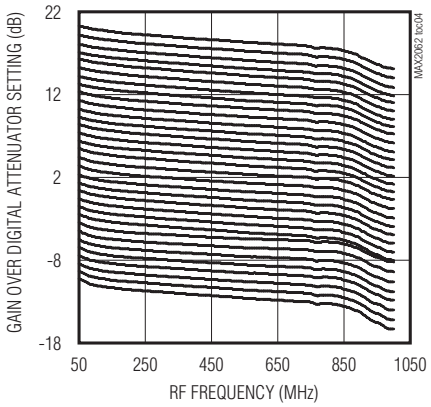

**GAIN vs. RF FREQUENCY**



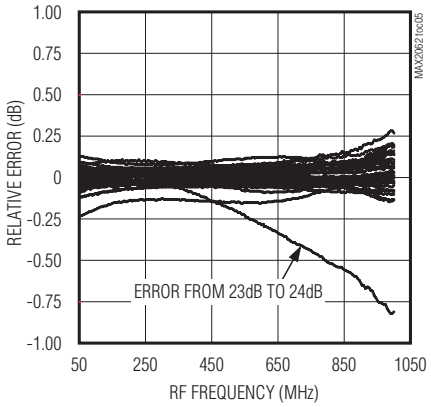
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

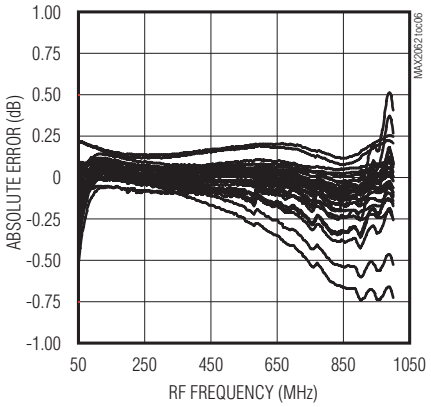
**GAIN OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**



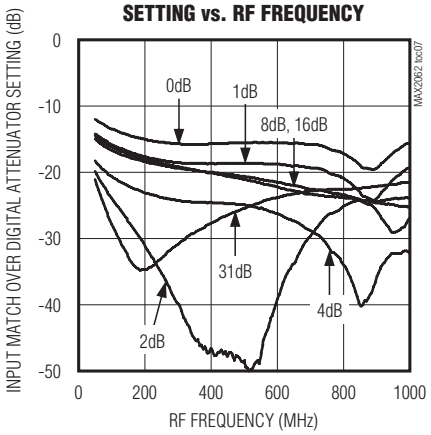

**DIGITAL ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY**



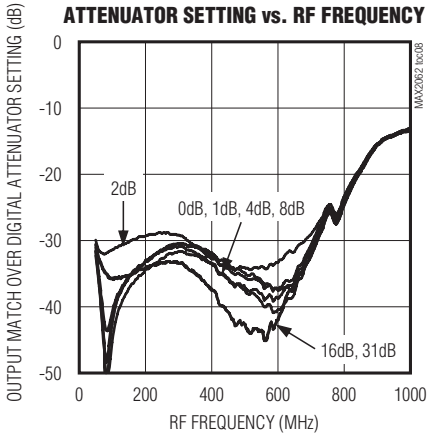

**DIGITAL ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY**



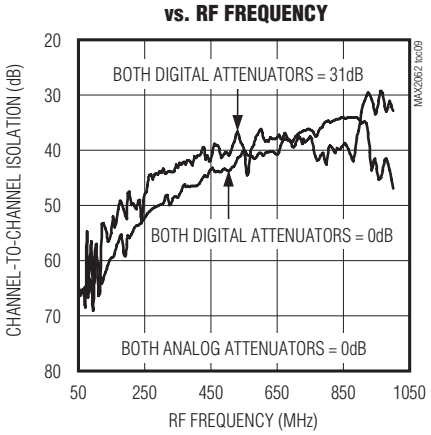

**INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**



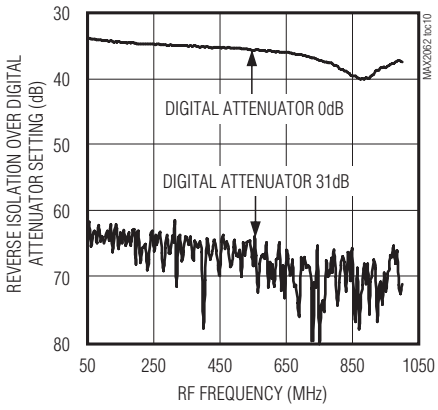

**OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**



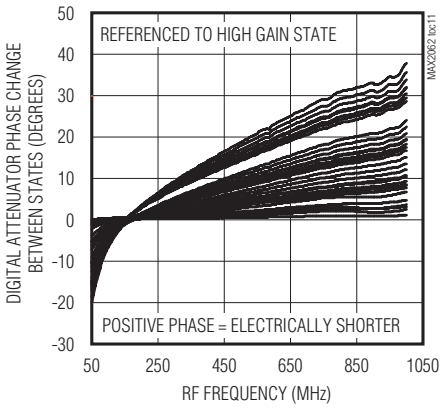

**CHANNEL-TO-CHANNEL ISOLATION vs. RF FREQUENCY**



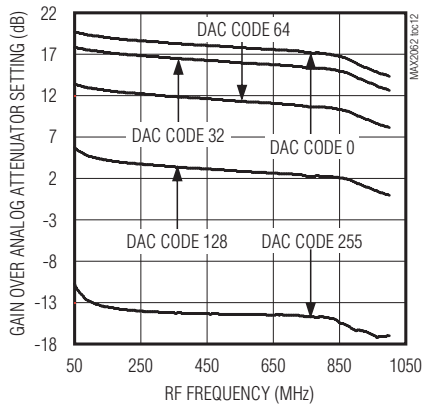

**REVERSE ISOLATION OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**




**DIGITAL ATTENUATOR PHASE CHANGE BETWEEN STATES vs. RF FREQUENCY**




**GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY**

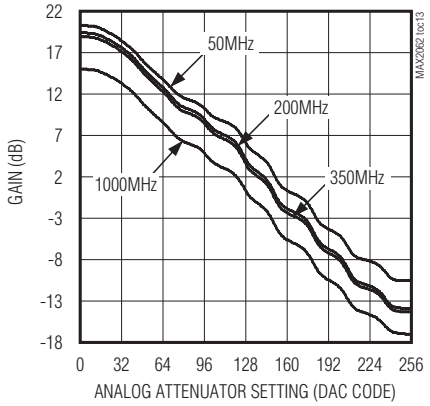


# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

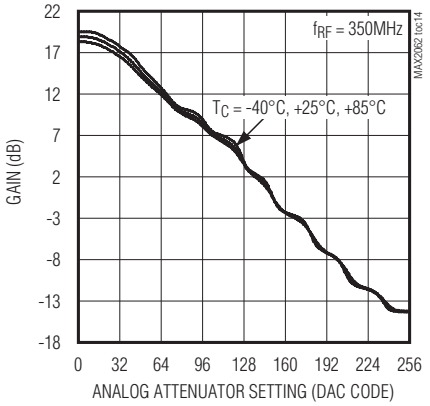
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

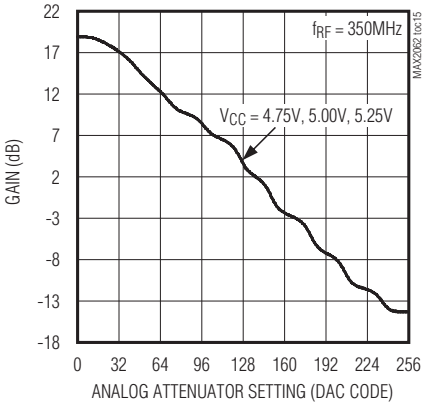
**GAIN vs. ANALOG ATTENUATOR SETTING**



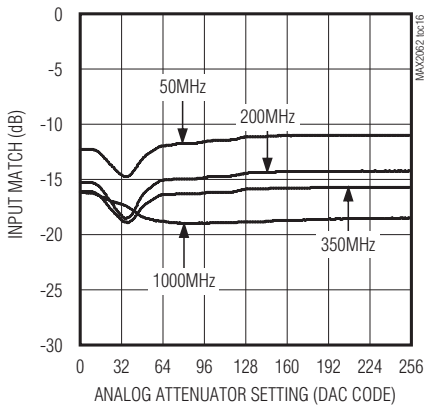

**GAIN vs. ANALOG ATTENUATOR SETTING**



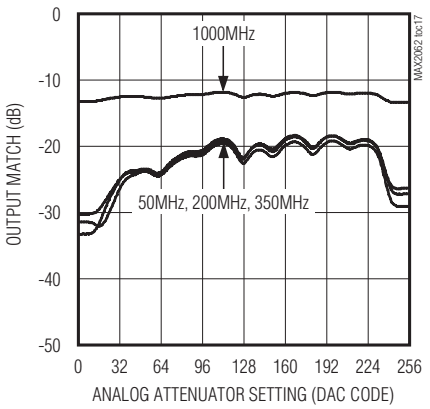

**GAIN vs. ANALOG ATTENUATOR SETTING**



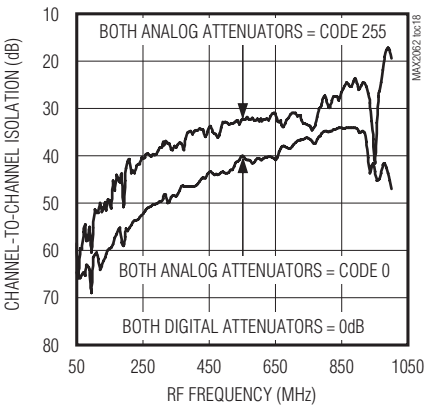

**INPUT MATCH vs. ANALOG ATTENUATOR SETTING**



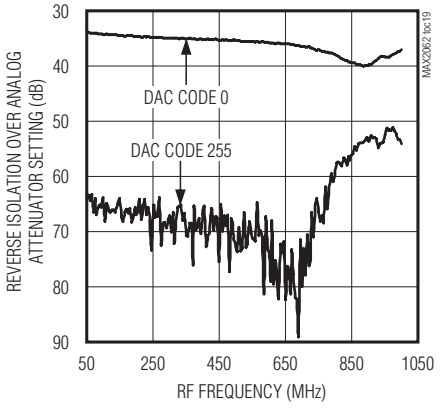

**OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING**



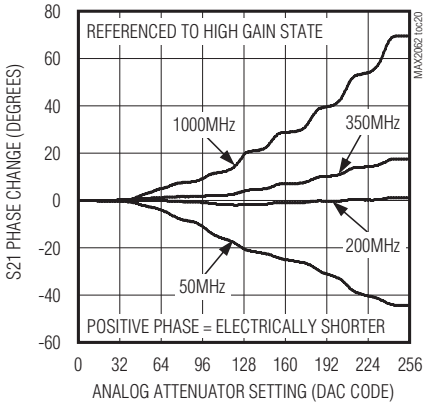

**CHANNEL-TO-CHANNEL ISOLATION vs. RF FREQUENCY**



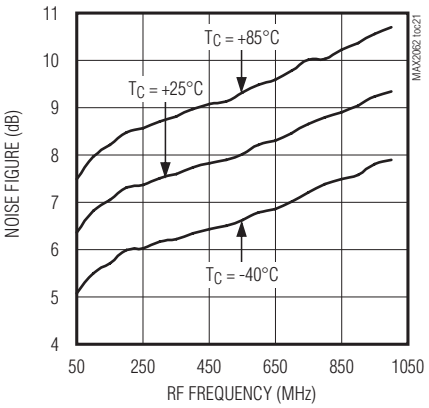

**REVERSE ISOLATION OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY**




**S21 PHASE CHANGE vs. ANALOG ATTENUATOR SETTING**




**NOISE FIGURE vs. RF FREQUENCY**



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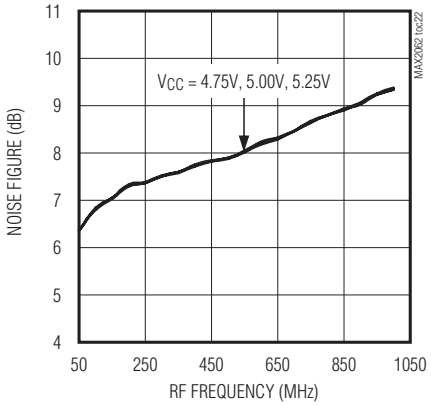
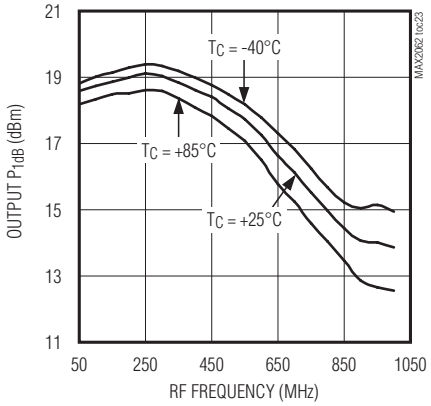
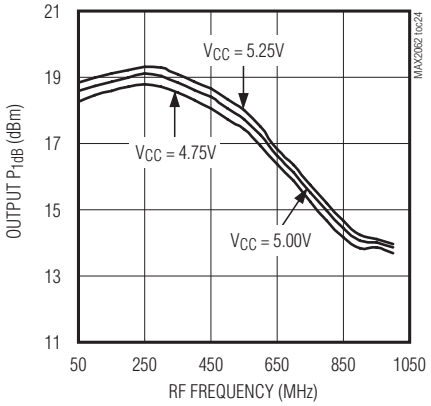
**NOISE FIGURE vs. RF FREQUENCY**



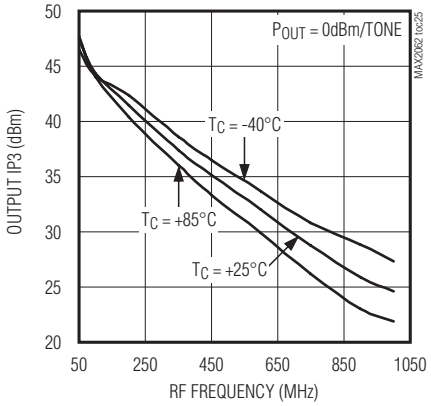

**OUTPUT $P_{1dB}$ vs. RF FREQUENCY**



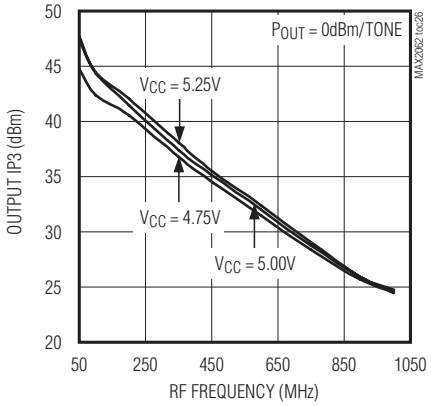

**OUTPUT $P_{1dB}$ vs. RF FREQUENCY**



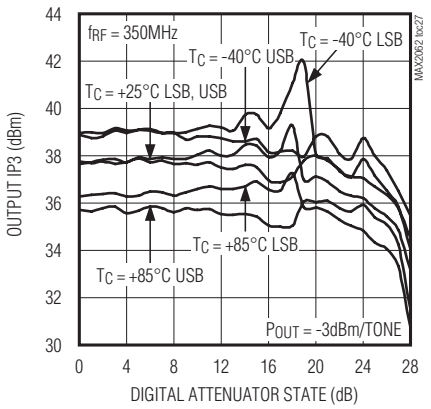

**OUTPUT IP3 vs. RF FREQUENCY**



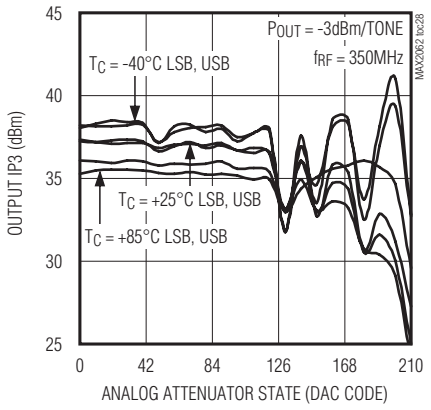

**OUTPUT IP3 vs. RF FREQUENCY**



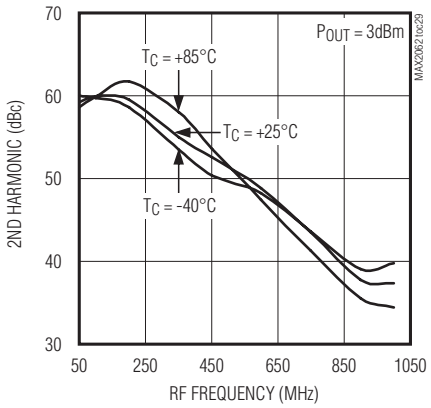

**OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE**



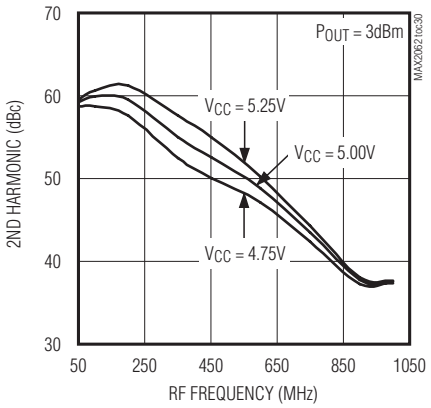

**OUTPUT IP3 vs. ANALOG ATTENUATOR STATE**




**2ND HARMONIC vs. RF FREQUENCY**




**2ND HARMONIC vs. RF FREQUENCY**

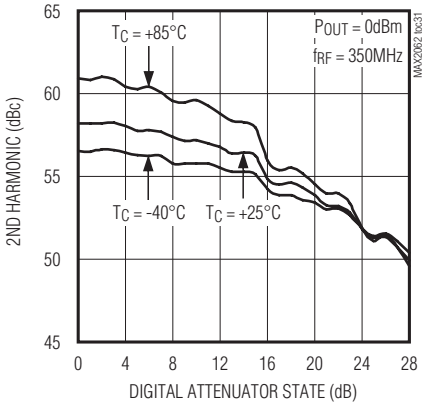


# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

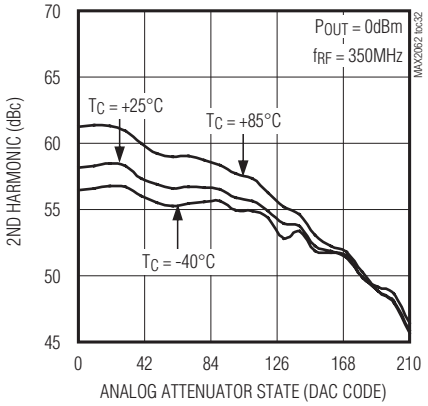
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 5.0V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 0, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

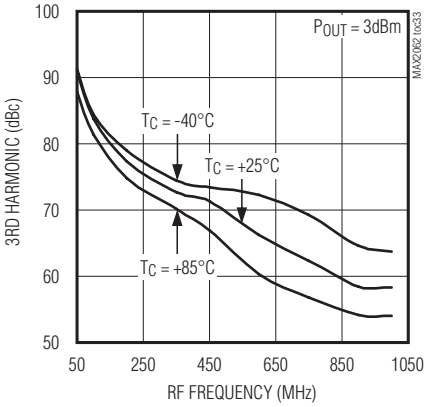
**2ND HARMONIC vs. DIGITAL ATTENUATOR STATE**



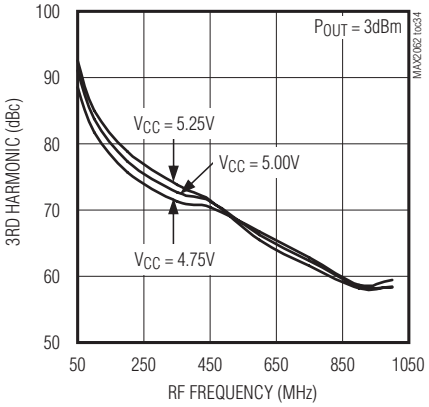

**2ND HARMONIC vs. ANALOG ATTENUATOR STATE**



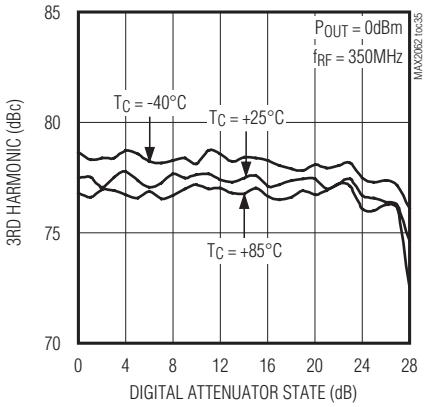

**3RD HARMONIC vs. RF FREQUENCY**



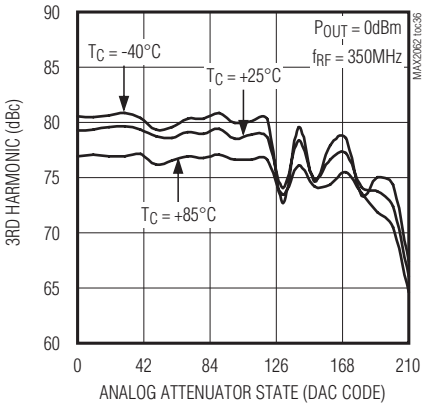

**3RD HARMONIC vs. RF FREQUENCY**



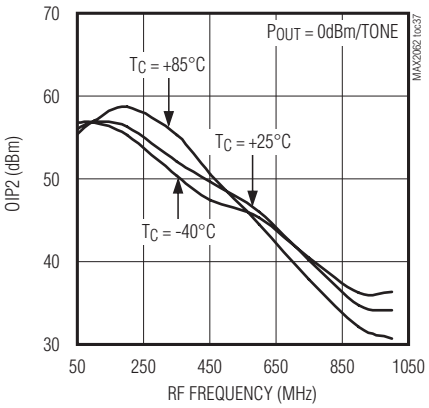

**3RD HARMONIC vs. DIGITAL ATTENUATOR STATE**



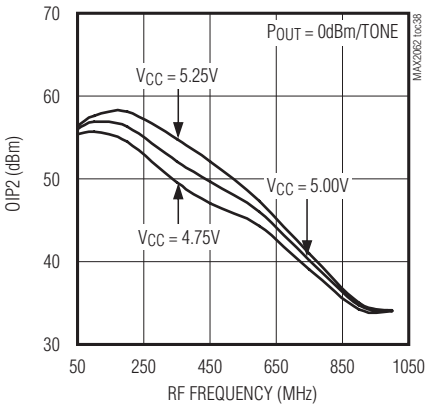

**3RD HARMONIC vs. ANALOG ATTENUATOR STATE**



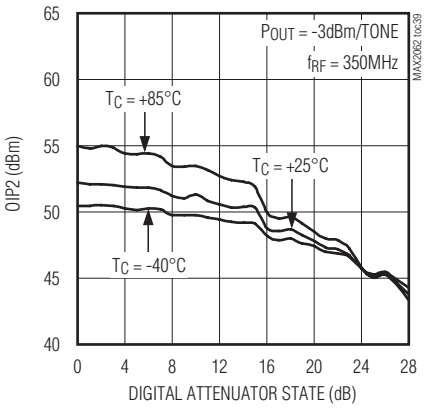

**OIP2 vs. RF FREQUENCY**




**OIP2 vs. RF FREQUENCY**




**OIP2 vs. DIGITAL ATTENUATOR STATE**



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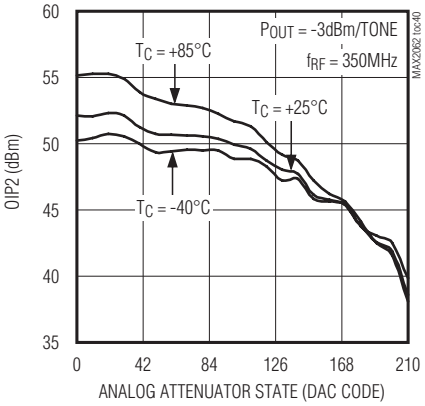
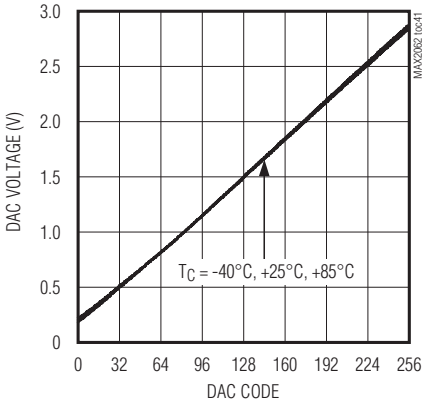
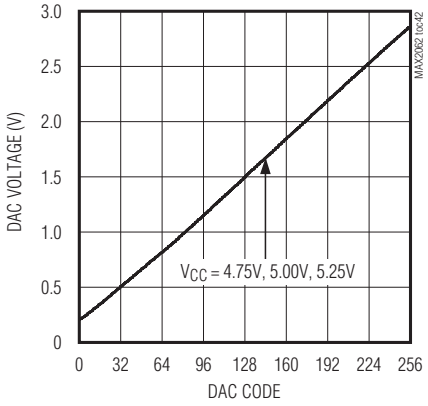
**OIP2 vs. ANALOG ATTENUATOR STATE**



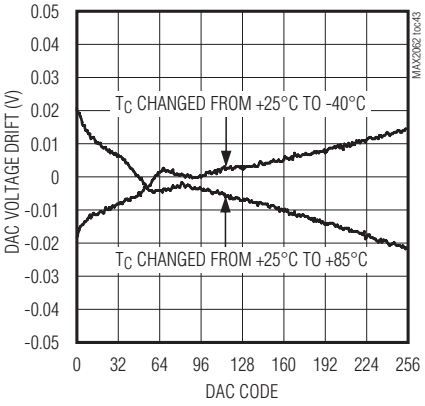

**DAC VOLTAGE vs. DAC CODE**



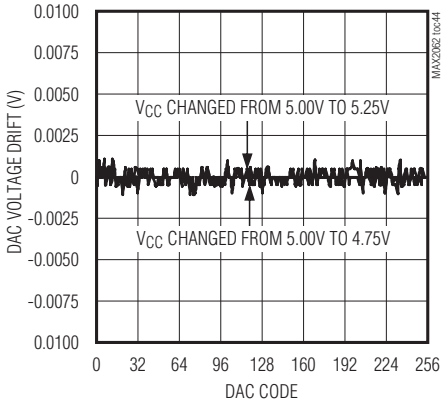

**DAC VOLTAGE vs. DAC CODE**



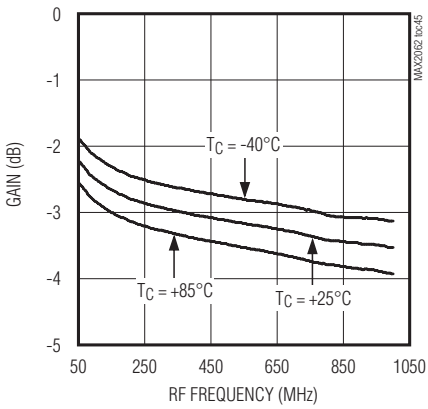

**DAC VOLTAGE DRIFT vs. DAC CODE**



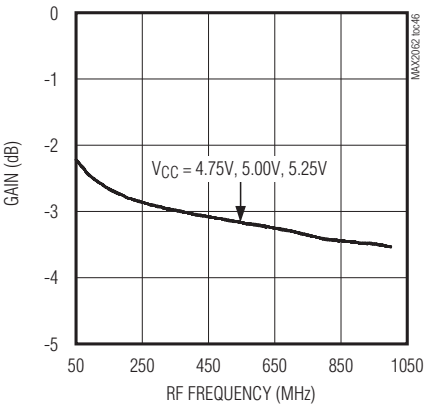

**DAC VOLTAGE DRIFT vs. DAC CODE**



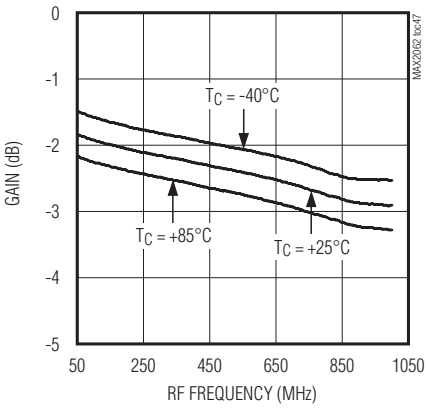

**GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)**



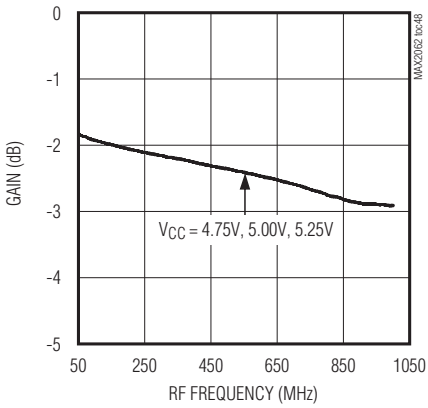

**GAIN vs. RF FREQUENCY (DIGITAL ATTENUATOR ONLY)**




**GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)**




**GAIN vs. RF FREQUENCY (ANALOG ATTENUATOR ONLY)**



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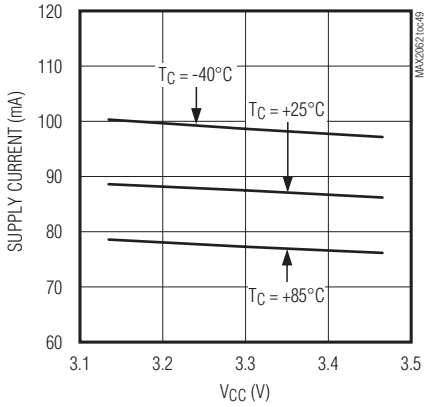
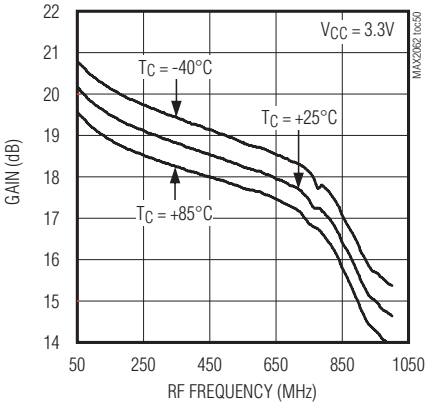
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

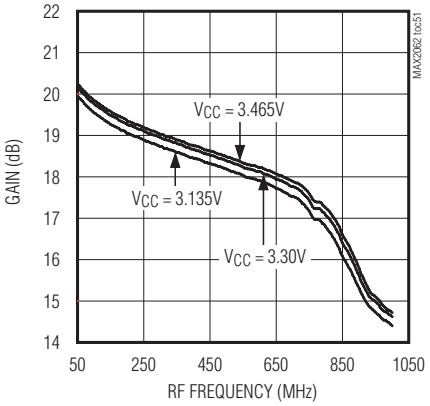
**SUPPLY CURRENT vs. $V_{CC}$**



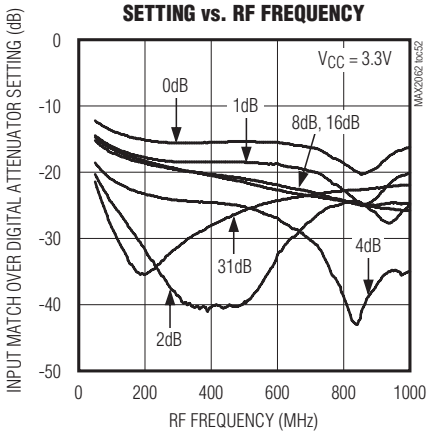

**GAIN vs. RF FREQUENCY**



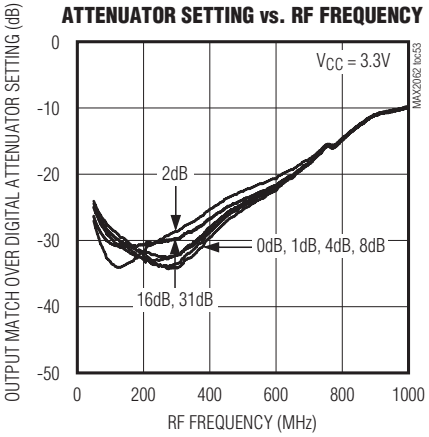

**GAIN vs. RF FREQUENCY**



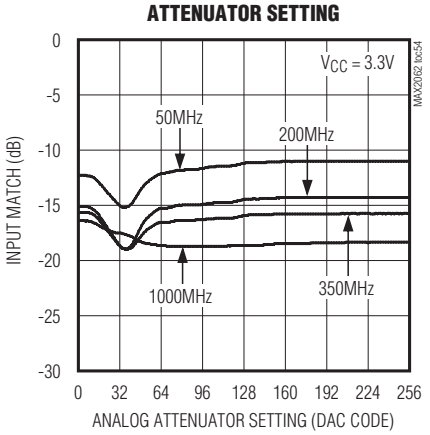

**INPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**



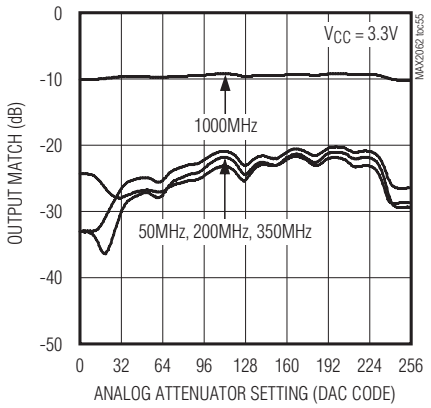

**OUTPUT MATCH OVER DIGITAL ATTENUATOR SETTING vs. RF FREQUENCY**



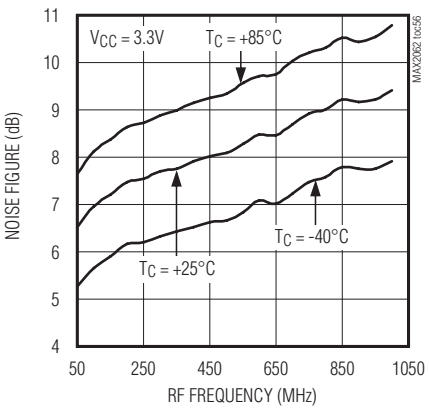

**INPUT MATCH vs. ANALOG ATTENUATOR SETTING**



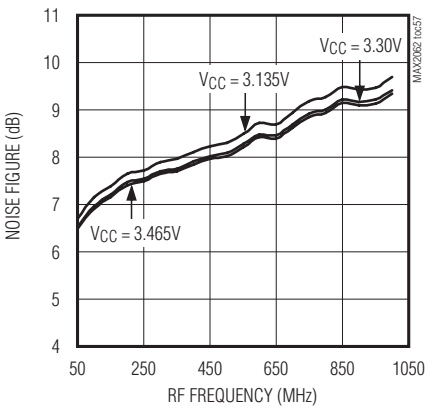

**OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING**




**NOISE FIGURE vs. RF FREQUENCY**



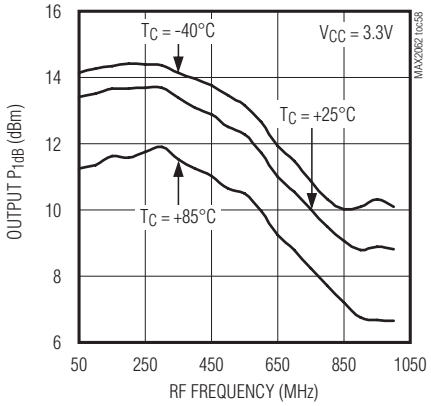

**NOISE FIGURE vs. RF FREQUENCY**



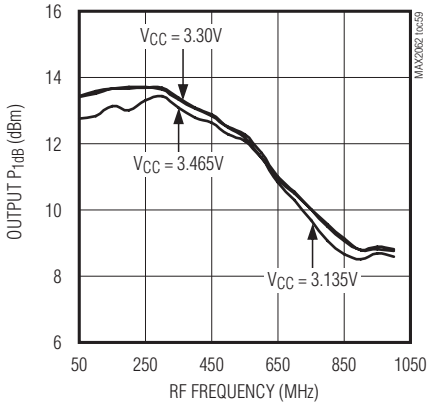
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

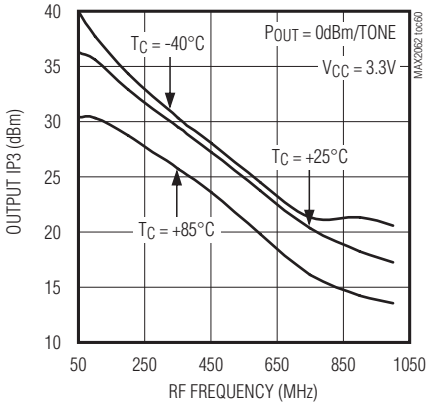
**OUTPUT $P_{1dB}$ vs. RF FREQUENCY**



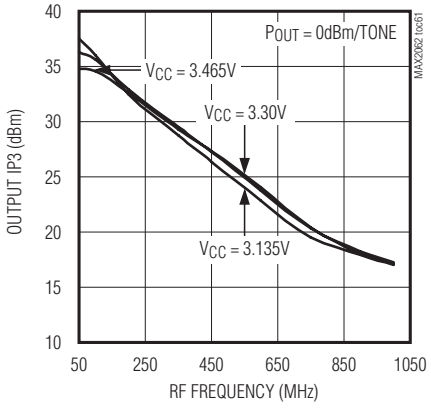

**OUTPUT $P_{1dB}$ vs. RF FREQUENCY**



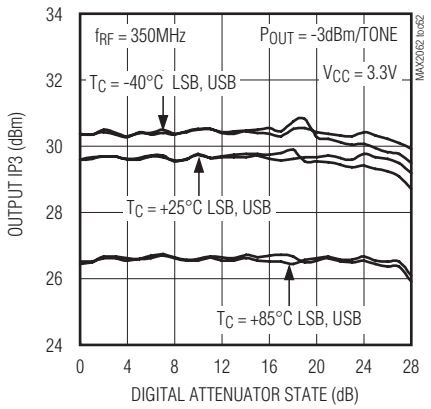

**OUTPUT IP3 vs. RF FREQUENCY**



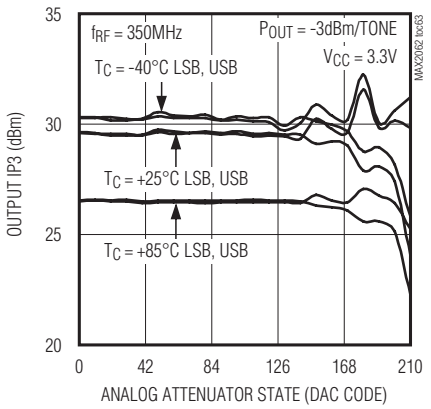

**OUTPUT IP3 vs. RF FREQUENCY**



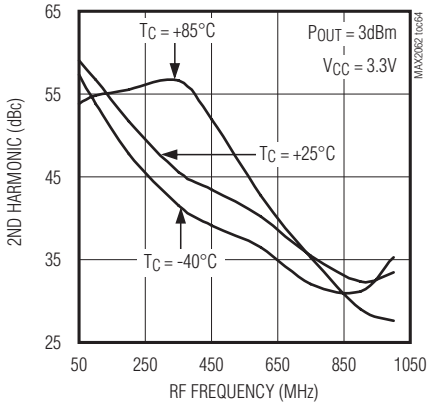

**OUTPUT IP3 vs. DIGITAL ATTENUATOR STATE**



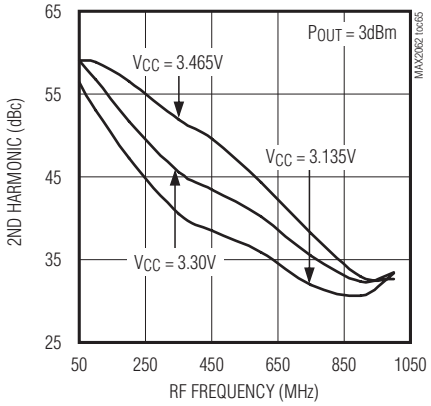

**OUTPUT IP3 vs. ANALOG ATTENUATOR STATE**



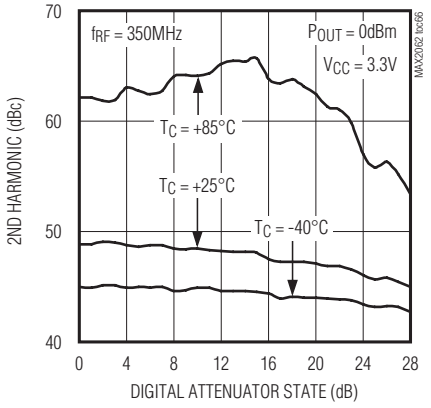

**2ND HARMONIC vs. RF FREQUENCY**




**2ND HARMONIC vs. RF FREQUENCY**




**2ND HARMONIC vs. DIGITAL ATTENUATOR STATE**

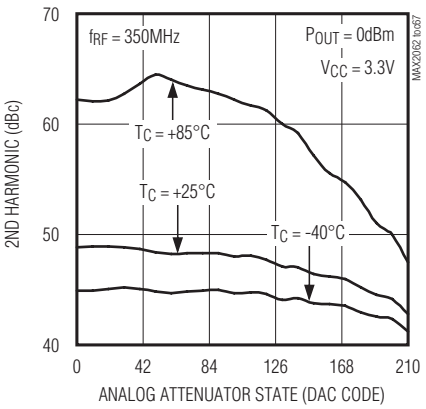


# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

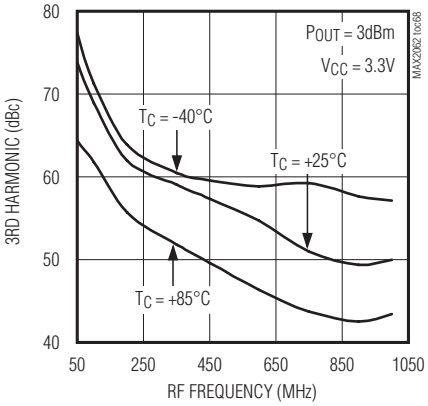
## 典型工作特性(续)

(*Typical Application Circuit*, **$V_{CC}$ = $V_{CC_AMP_1}$ = $V_{CC_AMP_2}$ = $V_{CC_RG}$ = 3.3V**, attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD_1 = PD_2 = 0, $P_{IN}$ = -20dBm, $f_{RF}$ = 350MHz, and $T_C$ = +25°C, unless otherwise noted.)

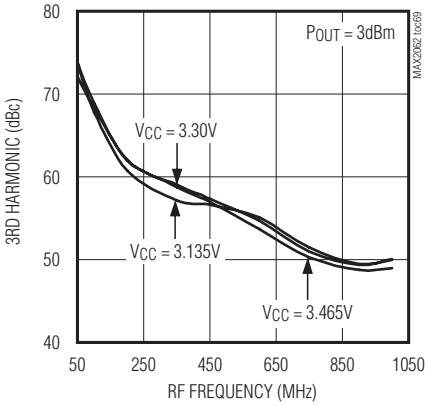
**2ND HARMONIC vs. ANALOG ATTENUATOR STATE**



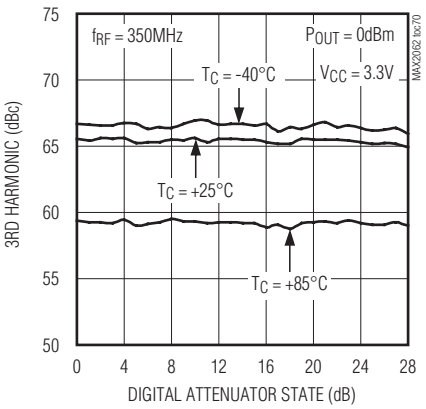

**3RD HARMONIC vs. RF FREQUENCY**



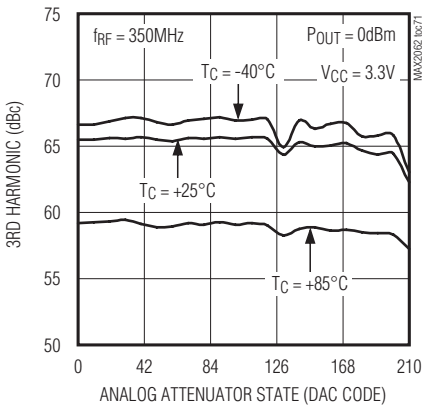

**3RD HARMONIC vs. RF FREQUENCY**



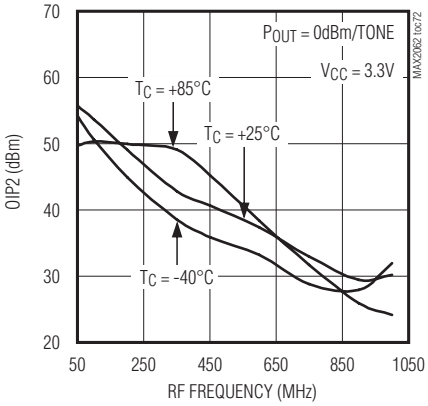

**3RD HARMONIC vs. DIGITAL ATTENUATOR STATE**



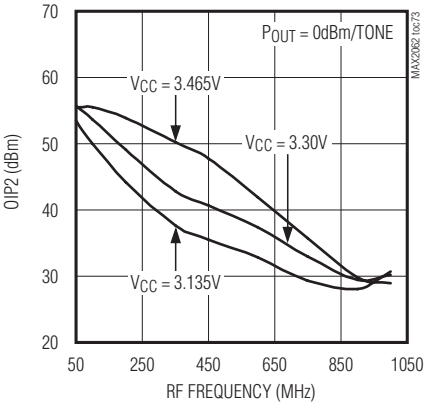

**3RD HARMONIC vs. ANALOG ATTENUATOR STATE**



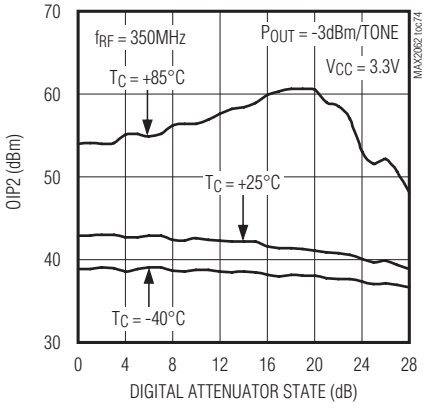

**OIP2 vs. RF FREQUENCY**



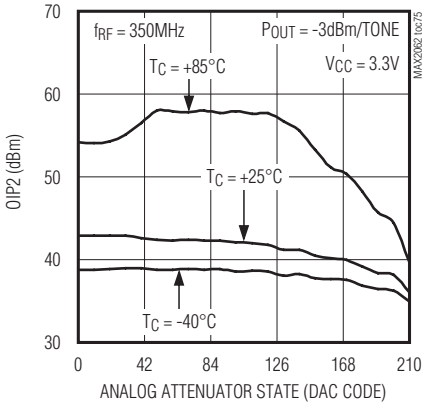

**OIP2 vs. RF FREQUENCY**



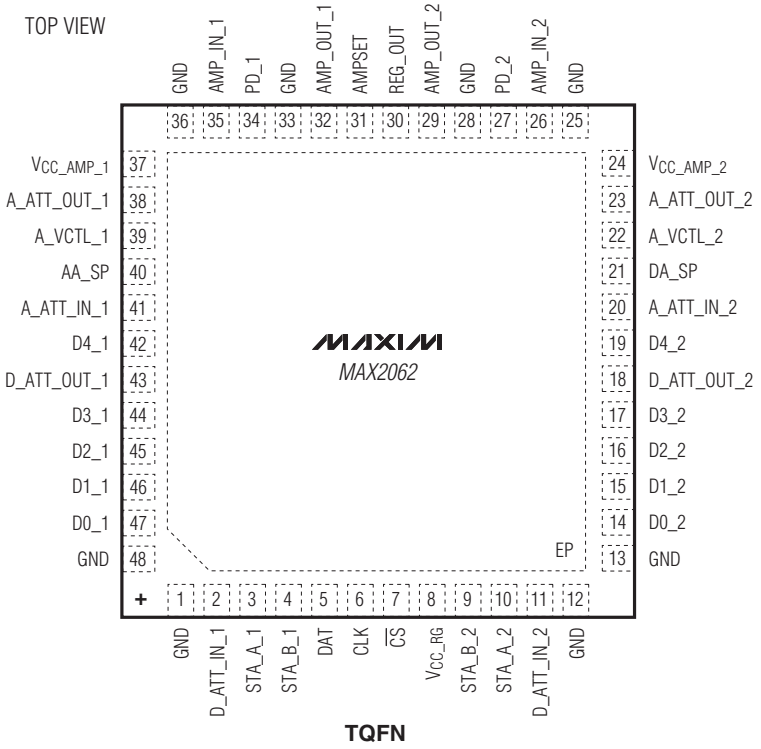

**OIP2 vs. DIGITAL ATTENUATOR STATE**




**OIP2 vs. ANALOG ATTENUATOR STATE**



## 引脚配置




## 引脚说明

| 引脚 | 名称 | 功能 |
|---|---|---|
| 1, 12, 13, 25, 28, 33, 36, 48 | GND | 地。 |
| 2 | D_ATT_IN_1 | 5位数字衰减器输入(50Ω)，通道1。需要外接隔直流电容。 |
| 3 | STA_A_1 | 数字衰减器预编程衰减状态逻辑输入，通道1。<br>**状态A　状态B　数字衰减器**<br>逻辑电平 = 0　逻辑电平 = 0　预编程状态1<br>逻辑电平 = 1　逻辑电平 = 0　预编程状态2<br>逻辑电平 = 0　逻辑电平 = 1　预编程状态3<br>逻辑电平 = 1　逻辑电平 = 1　预编程状态4 |
| 4 | STA_B_1 | |
| 5 | DAT | SPI数据输入。 |
| 6 | CLK | SPI时钟输入。 |
| 7 | $\overline{CS}$ | SPI片选输入。 |
| 8 | $V_{CC_RG}$ | 稳压电源输入，连接到3.3V或5V外部电源。$V_{CC_RG}$为驱动放大器以外的所有电路供电，在尽可能靠近该引脚的位置安装10nF旁路电容。 |

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

## 引脚说明(续)

| 引脚 | 名称 | 功能 |
|---|---|---|
| 9 | STA_B_2 | 数字衰减器预编程衰减状态逻辑输入，通道2。<br>**状态A　状态B　数字衰减器**<br>逻辑电平 = 0　逻辑电平 = 0　预编程状态1<br>逻辑电平 = 1　逻辑电平 = 0　预编程状态2<br>逻辑电平 = 0　逻辑电平 = 1　预编程状态3<br>逻辑电平 = 1　逻辑电平 = 1　预编程状态4 |
| 10 | STA_A_2 | |
| 11 | D_ATT_IN_2 | 5位数字衰减器输入(50Ω)，通道2。需要外接隔直流电容。 |
| 14 | D0_2 | 1dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。 |
| 15 | D1_2 | 2dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。 |
| 16 | D2_2 | 4dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。 |
| 17 | D3_2 | 8dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。 |
| 18 | D_ATT_OUT_2 | 5位数字衰减器输出(50Ω)，通道2。需要外接隔直流电容，通过1000pF电容连接到A_ATT_IN_2。 |
| 19 | D4_2 | 16dB衰减器逻辑输入，通道2。逻辑0 = 关闭；逻辑1 = 使能。 |
| 20 | A_ATT_IN_2 | 模拟衰减器输入(50Ω)，通道2。需要外接隔直流电容，通过1000pF电容连接到D_ATT_OUT_2。 |
| 21 | DA_SP | 数字衰减器串行/并行控制选择输入。将DA_SP设置为逻辑1，选择串行控制；将DA_SP设置为逻辑0，选择并行控制。 |
| 22 | A_VCTL_2 | 模拟衰减器电压控制输入，通道2。如果使用片上DAC（AA_SP = 1），则通过150pF电容将该引脚旁路至地。 |
| 23 | A_ATT_OUT_2 | 模拟衰减器输出(50Ω)，通道2。需要外接隔直流电容，通过1000pF电容连接到AMP_IN_2。 |
| 24 | $V_{CC_AMP_2}$ | 驱动放大器电源电压输入，通道2。在尽可能靠近该引脚的位置安装10nF旁路电容。 |
| 26 | AMP_IN_2 | 驱动放大器输入(50Ω)，通道2。需要外接隔直流电容，通过1000pF电容连接到A_ATT_OUT_2。 |
| 27 | PD_2 | 关断控制，通道2。详细操作请参考表2。 |
| 29 | AMP_OUT_2 | 驱动放大器输出(50Ω)，通道2。在AMP_OUT_2与$V_{CC_}$之间连接上拉电感。 |
| 30 | REG_OUT | 稳压器输出，通过1µF电容旁路。 |
| 31 | AMPSET | 3.3V供电时，驱动放大器的偏置设置。$V_{CC_AMP_1}$和$V_{CC_AMP_2}$采用3.3V供电时，该引脚置为逻辑1；5V供电时，置为逻辑0。 |
| 32 | AMP_OUT_1 | 驱动放大器输出(50Ω)，通道1。在AMP_OUT_1与$V_{CC_}$之间连接上拉电感。 |
| 34 | PD_1 | 关断控制，通道1。详细操作请参考表2。 |
| 35 | AMP_IN_1 | 驱动放大器输入(50Ω)，通道1。需要外接隔直流电容，通过1000pF电容连接到A_ATT_OUT_1。 |
| 37 | $V_{CC_AMP_1}$ | 驱动放大器电源电压输入，通道1。在尽可能靠近该引脚的位置安装10nF旁路电容。 |
| 38 | A_ATT_OUT_1 | 模拟衰减器输出(50Ω)，通道1。需要外接隔直流电容，通过1000pF电容连接到AMP_IN_1。 |
| 39 | A_VCTL_1 | 模拟衰减器电压控制输入，通道1。如果使用片上DAC（AA_SP = 1），则通过150pF电容将该引脚旁路至地。 |

## 引脚说明(续)

| 引脚 | 名称 | 功能 |
|---|---|---|
| 40 | AA_SP | 模拟衰减器的DAC使能/禁用逻辑输入。AA_SP置为逻辑1时，使能片上DAC电路和数字SPI控制；AA_SP置为逻辑0时，禁用片上DAC电路和数字SPI控制。AA_SP = 0时，使用模拟控制线(A_VCTL_1和A_VCTL_2)。 |
| 41 | A_ATT_IN_1 | 模拟衰减器输入(50Ω)，通道1。需要外接隔直流电容，通过1000pF电容连接到D_ATT_OUT_1。 |
| 42 | D4_1 | 16dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。 |
| 43 | D_ATT_OUT_1 | 5位数字衰减器输出(50Ω)，通道1。需要外接隔直流电容，通过1000pF电容连接到A_ATT_IN_1。 |
| 44 | D3_1 | 8dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。 |
| 45 | D2_1 | 4dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。 |
| 46 | D1_1 | 2dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。 |
| 47 | D0_1 | 1dB衰减器逻辑输入，通道1。逻辑0 = 关闭；逻辑1 = 使能。 |
| — | EP | 裸焊盘，内部连接到GND。将其连接到GND，以改善RF性能、增强散热。 |

## 详细说明

MAX2062高线性度模拟/数字VGA是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω接口的应用而设计。

器件的每个通道集成了一个数字衰减器和一个模拟衰减器，可提供64dB的总增益控制，同时可优化放大器驱动设计以提供高增益、高IP3、低NF和低功耗指标。

可通过SPI兼容接口控制作为从机外设的每个数字衰减器；也允许以1dB步长通过5位并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择，可直接设置在4种增益选项的一种，用户可通过SPI兼容接口预先设置四种增益选项。2个独立的控制引脚允许用户快速选择4种定制衰减状态的任何一个，无需对SPI总线重新编程。每路模拟衰减器采用外部电压或通过SPI兼容接口采用片内8位DAC进行控制。衰减器编程的详细信息，请参见*应用信息*部分。

由于每个信号通道的三级电路中的每一级都具有各自的RF输入和RF输出，通过适当配置可以优化噪声系数(NF)（放大器配置为第一级)、OIP3（放大器配置为最后一级)或者在NF与OIP3之间进行折中。该器件具有24dB的放大器增益(放大器本身)，增益最大时NF为7.3dB（包括衰减器的插入损耗)，并提供+41dBm的高OIP3。这些特性使得该器件成为多通道接收器和发射器应用理想的VGA选择。

此外，器件采用+5V单电源供电时具有最优的性能；工作在+3.3V单电源时，具有先进的省电模式，但性能指标略有降低。器件采用紧凑、带裸焊盘的48引脚TQFN封装(7mm x 7mm)，在扩展级温度范围($T_C$ = -40°C至+85°C)内确保电气特性。

### 模拟和5位数字衰减器控制

器件集成了两个模拟衰减器和两个5位数字衰减器，用于实现高动态范围控制。每个模拟衰减器具有33dB增益范围，采用外部电压或通过3线SPI接口采用片内8位DAC进行控制。每个数字衰减器具有31dB控制范围、1dB步长，通过3线SPI接口或独立的5位并行总线进行设置。衰减器编程的详细信息，请参见*应用信息*部分和表1。这些衰减器可用于静态和动态功率控制。

需要注意的是，当采用DAC通过SPI总线控制模拟衰减器时，DAC输出电压送入A_VCTL_1和A_VCTL_2引脚(分别为39和22引脚)。因此，SPI模式下，A_VCTL_1和A_VCTL_2引脚必须连接到接地电阻和电容，如*典型应用电路*所示。

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

表1. 控制逻辑

| AA_SP | ANALOG ATTENUATOR | D/A CONVERTER |
|---|---|---|
| 0 | Controlled by external control voltage | Disabled |
| 1 | Controlled by on-chip DAC | Enabled (DAC output voltage shows on A_VCTL__ pins); DAC uses on-chip voltage reference |
| **DA_SP** | **DIGITAL ATTENUATOR** | |
| 0 | Parallel controlled | |
| 1 | SPI controlled (control voltages show up on the parallel control pins) | |

### 驱动放大器

器件的每个通道都包括一个24dB固定增益的高性能驱动器。驱动放大器电路优化于50MHz至1000MHz频率范围的高线性度指标。

## 应用信息

### 工作模式

器件可以选择工作在+3.3V电源电压，但会降低线性指标。AMPSET引脚需要在不同模式下进行适当偏置，如表2所示。此外，还可对驱动放大器进行独立的关断控制，以降低直流电源的功耗，详细信息请参考表2所示的偏置配置。

### SPI接口和衰减器设置

数字衰减器可采用5位字长通过3线SPI/MICROWIRE®兼容串行接口进行控制。移入56位数据，MSB在前，并通过$\overline{CS}$打包成帧。前28位数据用于设置第一路衰减器，后续28位数据用于设置第二路衰减器。当$\overline{CS}$为低电平时，时钟有效，数据在时钟的上升沿移入。当$\overline{CS}$跳变到高电平时，数据被锁存，改变衰减器设置(图1)。表3给出了SPI数据格式的详细信息。

表2. 工作模式

| RESULT | VCC (V) | AMPSET | PD_1 | PD_2 |
|---|---|---|---|---|
| All on | 5 | 0 | 0 | 0 |
| | 3.3 | 1 | 0 | 0 |
| AMP1 off AMP2 on | 5 | 0 | 1 | 0 |
| | 3.3 | 1 | 1 | 0 |
| AMP1 on AMP2 off | 5 | 0 | 0 | 1 |
| | 3.3 | 1 | 0 | 1 |
| All off | 5 | 0 | 1 | 1 |
| | 3.3 | 1 | 1 | 1 |

### 通道1 DAC和数字衰减器编程

D0:D7　发送至DAC寄存器
D0 = LSB，D7 = MSB

D8:D12　预编程衰减状态1
D8 = 1dB位，D9 = 2dB位，D10 = 4dB位，D11 = 8dB位，D12 = 16dB位

D13:D17　预编程衰减状态2
D13 = 1dB位，D14 = 2dB位，D15 = 4dB位，D16 = 8dB位，D17 = 16dB位

D18:D22　预编程衰减状态3
D18 = 1dB位，D19 = 2dB位，D20 = 4dB位，D21 = 8dB位，D22 = 16dB位

D23:D27　预编程衰减状态4
D23 = 1dB位，D24 = 2dB位，D25 = 4dB位，D26 = 8dB位，D27 = 16dB位

### 通道2 DAC和数字衰减器编程

D28:D35　发送至DAC寄存器
D28 = LSB，D35 = MSB

D36:D40　预编程衰减状态1
D36 = 1dB位，D37 = 2dB位，D38 = 4dB位，D39 = 8dB位，D40 = 16dB位

D41:D45　预编程衰减状态2
D41 = 1dB位，D42 = 2dB位，D43 = 4dB位，D44 = 8dB位，D45 = 16dB位

D46:D50　预编程衰减状态3
D46 = 1dB位，D47 = 2dB位，D48 = 4dB位，D49 = 8dB位，D50 = 16dB位

D51:D55　预编程衰减状态4
D51 = 1dB位，D52 = 2dB位，D53 = 4dB位，D54 = 8dB位，D55 = 16dB位

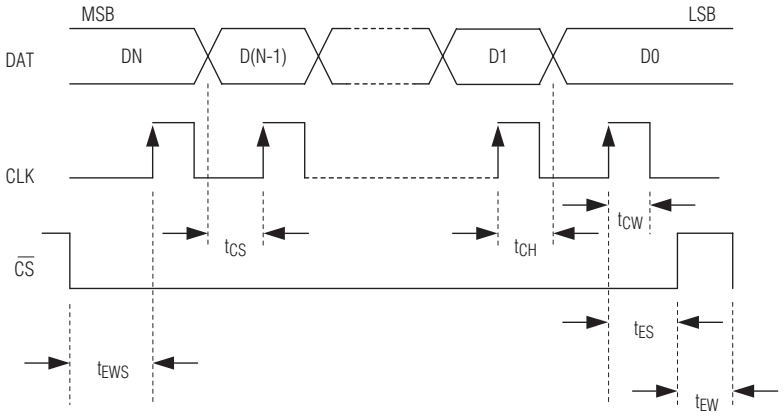
*MICROWIRE是National Semiconductor Corporation的注册商标。*

表3. SPI数据格式

| FUNCTION | BIT | DESCRIPTION |
|---|---|---|
| Digital Attenuator State 4 (Path 2) | D55 (MSB) | 16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 4) |
| | D54 | 8dB step |
| | D53 | 4dB step |
| | D52 | 2dB step |
| | D51 | 1dB step |
| Digital Attenuator State 3 (Path 2) | D50 | 16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 3) |
| | D49 | 8dB step |
| | D48 | 4dB step |
| | D47 | 2dB step |
| | D46 | 1dB step |
| Digital Attenuator State 2 (Path 2) | D45 | 16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 2) |
| | D44 | 8dB step |
| | D43 | 4dB step |
| | D42 | 2dB step |
| | D41 | 1dB step |
| Digital Attenuator State 1 (Path 2) | D40 | 16dB step (MSB of the 5-bit word used to program the Path 2 digital attenuator state 1) |
| | D39 | 8dB step |
| | D38 | 4dB step |
| | D37 | 2dB step |
| | D36 | 1dB step |
| On-Chip DAC (Path 2) | D35 | Bit 7 (MSB) of on-chip DAC used to program the Path 2 analog attenuator |
| | D34 | Bit 6 of DAC |
| | D33 | Bit 5 of DAC |
| | D32 | Bit 4 of DAC |
| | D31 | Bit 3 of DAC |
| | D30 | Bit 2 of DAC |
| | D29 | Bit 1 of DAC |
| | D28 | Bit 0 (LSB) of DAC |
| Digital Attenuator State 4 (Path 1) | D27 | 16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 4) |
| | D26 | 8dB step |
| | D25 | 4dB step |
| | D24 | 2dB step |
| | D23 | 1dB step |
| Digital Attenuator State 3 (Path 1) | D22 | 16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 3) |
| | D21 | 8dB step |
| | D20 | 4dB step |
| | D19 | 2dB step |
| | D18 | 1dB step |

表3. SPI数据格式(续)

| FUNCTION | BIT | DESCRIPTION |
|---|---|---|
| Digital Attenuator State 2 (Path 1) | D17 | 16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 2) |
| | D16 | 8dB step |
| | D15 | 4dB step |
| | D14 | 2dB step |
| | D13 | 1dB step |
| Digital Attenuator State 1 (Path 1) | D12 | 16dB step (MSB of the 5-bit word used to program the Path 1 digital attenuator state 1) |
| | D11 | 8dB step |
| | D10 | 4dB step |
| | D9 | 2dB step |
| | D8 | 1dB step |
| On-Chip DAC (Path 1) | D7 | Bit 7 (MSB) of on-chip DAC used to program the Path 1 analog attenuator |
| | D6 | Bit 6 of DAC |
| | D5 | Bit 5 of DAC |
| | D4 | Bit 4 of DAC |
| | D3 | Bit 3 of DAC |
| | D2 | Bit 2 of DAC |
| | D1 | Bit 1 of DAC |
| | D0 (LSB) | Bit 0 (LSB) of DAC |




**NOTES**: DATA ENTERED ON CLOCK RISING EDGE.
ATTENUATOR REGISTER STATE CHANGE ON $\overline{CS}$ RISING EDGE.
N = NUMBER OF DATA BITS.

*图1. SPI时序图*

### *衰减器和DAC操作*

通过A_VCTL_1和A_VCTL_2 (引脚39和22)上的外部控制电压或片内8位DAC对两路模拟衰减器进行控制，而数字衰减器则通过SPI兼容接口或两个独立的5位并行总线进行控制。DAC使能/禁用逻辑输入引脚(AA_SP)和数字衰减器SPI/并行控制选择逻辑输入引脚(DA_SP)决定了衰减器的控制方式。

### *利用并行控制总线设置数字衰减器*

为了达到25ns的快速切换能力，器件提供一个辅助的5位并行控制接口。数字逻辑衰减器控制引脚(D0_至D4_)用于设置衰减器的各级电路(参考表3和表4)。

直接访问5位总线可以使用户省去SPI接口的编程延时。任何SPI总线的速率都受限于指令逐位传递到外围器件的时间。通过直接访问5位并行接口，用户可以在“快速建立”自动增益控制(AGC)应用中实现数字衰减状态的迅速切换。

需要注意的是，当数字衰减器由SPI总线控制时，每个数字衰减器的控制电压由五个并行控制引脚设置(引脚14至17和引脚19控制数字衰减器2，引脚42和引脚44至47控制数字衰减器1)。**当数字衰减器处于SPI控制模式时，并行控制引脚必须开路。**

### *“速射”预编程衰减状态*

器件能够在4个预编程衰减等级之间进行“速射”增益选择。与上述辅助5位总线类似，“速射”增益选择使用户能够快速进入4个预先设定的数字衰减状态的任意一个，消除了通过SPI总线重新编程的相关延时。

这种方式的切换速度与采用辅助5位并行总线的速度相当。但这一特殊功能可以使数字衰减器的I/O降低5倍或2.5倍(5个控制位与1个或2个控制位)，具体取决于所要求的状态数。

用户可通过STA_A_1和STA_B_1 (数字衰减器2对应于STA_A_2和STA_B_2)逻辑输入引脚设置所要求的各级状态(参考表5和表6)。利用STA_A_1引脚(1个控制位)可以得到2个预先设定的衰减状态，同时使用STA_A_1和STA_B_1引脚(2个控制位)，可以得到4个预先设定的衰减状态。

## 表4. 数字衰减器设置(并行控制，DA_SP = 0)

| INPUT | LOGIC = 0 (OR GROUND) | LOGIC = 1 |
|---|---|---|
| D0 | Disable 1dB attenuator | Enable 1dB attenuator |
| D1 | Disable 2dB attenuator | Enable 2dB attenuator |
| D2 | Disable 4dB attenuator | Enable 4dB attenuator |
| D3 | Disable 8dB attenuator | Enable 8dB attenuator |
| D4 | Disable 16dB attenuator | Enable 16dB attenuator |

## 表5. 衰减器1的可编程衰减状态设置 (DA_SP = 1)

| STA_A_1 | STA_B_1 | SETTING FOR DIGITAL ATTENUATOR 1* |
|---|---|---|
| 0 | 0 | Preprogrammed attenuation state 1 |
| 1 | 0 | Preprogrammed attenuation state 2 |
| 0 | 1 | Preprogrammed attenuation state 3 |
| 1 | 1 | Preprogrammed attenuation state 4 |

**由SPI编程位D8:D27定义(详细信息请参考表3)。*

## 表6. 衰减器2的可编程衰减状态设置 (DA_SP = 1)

| STA_A_2 | STA_B_2 | SETTING FOR DIGITAL ATTENUATOR 2** |
|---|---|---|
| 0 | 0 | Preprogrammed attenuation state 1 |
| 1 | 0 | Preprogrammed attenuation state 2 |
| 0 | 1 | Preprogrammed attenuation state 3 |
| 1 | 1 | Preprogrammed attenuation state 4 |

***由SPI编程位D36:D55定义(详细信息请参考表3)。*

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

例如，假设AGC应用需要静态调节衰减器，以解决接收器增益不一致的问题。该AGC电路还需要对可能引起接收器灵敏度下降以及ADC过驱动的干扰信号进行动态衰减。该实例中，器件可以预先设置(通过SPI总线) 2种定制衰减状态: 一个状态用于处理静态增益调节，另一个状态用于处理干扰信号。

用户只需要对一个I/O引脚(即STA_A_1控制位)进行控制，即可在静态和动态衰减设置之间快速切换。

需要时，用户还可以使用第二个I/O引脚(即STA_B_1控制位)设置另外两个衰减状态。这两个附加的衰减设置非常适合软件定义的无线通信装置，这些装置往往需要多个静态增益设置，以满足不同工作频率的要求；也适合需要多个动态衰减设置以处理不同阻塞电平(按照多个无线通信标准的定义)的应用。

### *供电顺序*

所采用的供电顺序为:

1) 电源

2) 控制信号

### *布局考虑*

器件经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。器件采用48引脚TQFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装器件的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP**必须**直接或通过一系列电镀过孔焊接到PCB的地层。PCB布局在顶层应提供适当的屏蔽地线，对放大器的输入和输出进行隔离。在这两条通路(输入和输出)之间加入屏蔽地线对于实现通道间隔离十分重要。

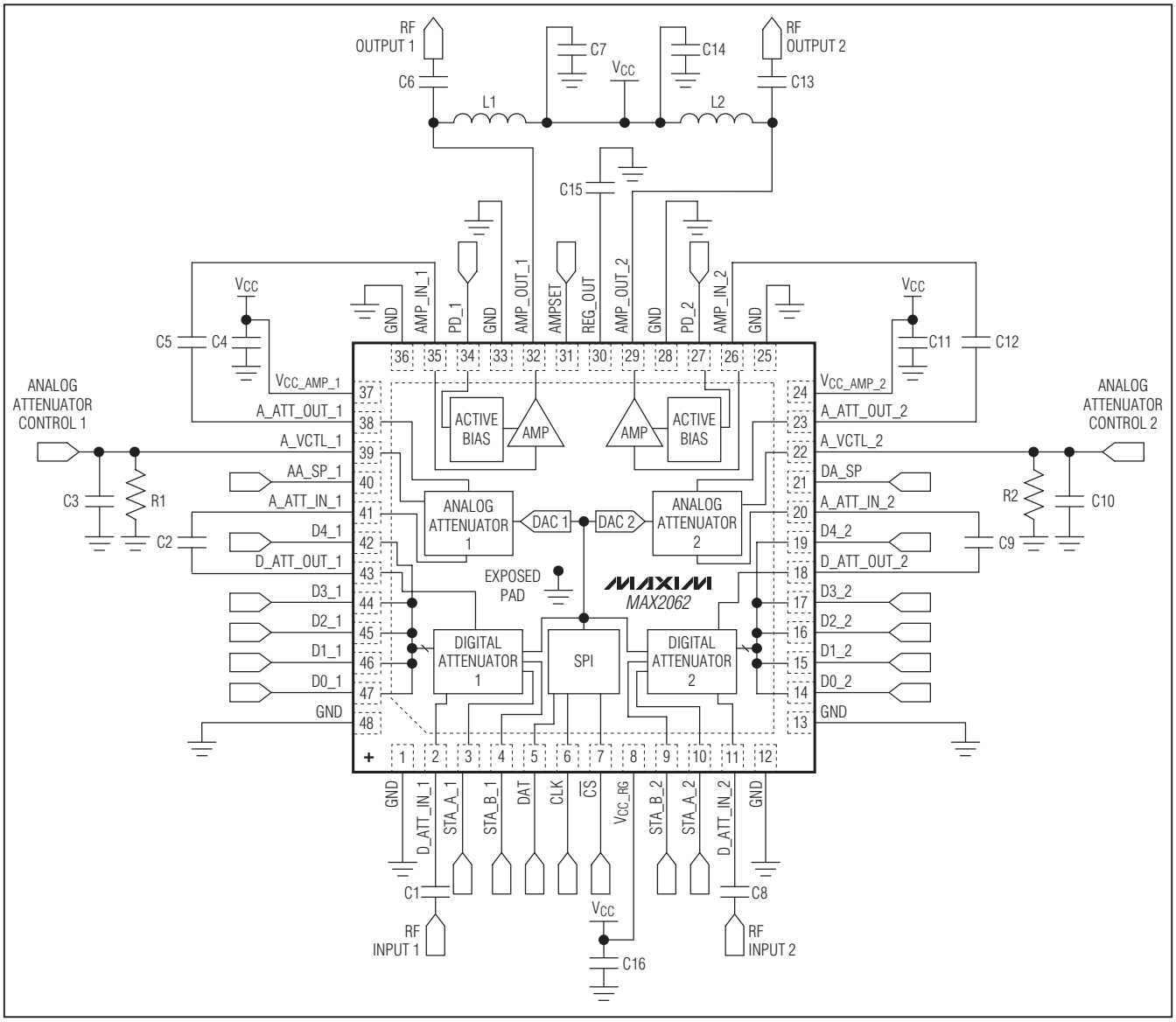
## 表7. 典型应用电路的元件值

| DESIGNATION | QTY | DESCRIPTION | COMPONENT SUPPLIER |
|---|---|---|---|
| C1, C2, C5, C6, C8, C9, C12, C13 | 8 | 1000pF ceramic capacitors (0402) GRM1555C1H102J | Murata Electronics North America, Inc. |
| C3, C10 | 2 | 150pF ceramic capacitors (0402) GRM1555C1H151J | Murata Electronics North America, Inc. |
| C4, C7, C11, C14, C16 | 5 | 10nF ceramic capacitors (0402) GRM155R71E103K | Murata Electronics North America, Inc. |
| C15 | 1 | 1µF ceramic capacitor (0603) GRM188R71C105K | Murata Electronics North America, Inc. |
| L1, L2* | 2 | 820nH inductors (1008) Coilcraft 1008CS-821XJLC | Coilcraft, Inc. |
| R1, R2 | 2 | 47.5kΩ resistors (0402) | — |
| U1 | 1 | 48 TQFN-EP (7mm x 7mm) Maxim MAX2062ETM | Maxim Integrated Products, Inc. |

**适当选择电感值，确保电感的自激频率位于工作频带之外。*

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

## 典型应用电路




## 芯片信息

PROCESS: SiGe BiCMOS

## 封装信息

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

| 封装类型 | 封装编码 | 外形编号 | 焊盘布局编号 |
|---|---|---|---|
| 48 TQFN-EP | T4877+7 | 21-0144 | 90-0133 |

# 50MHz至1000MHz、高线性度、可串行/并行控制的双通道模拟/数字VGA

## 修订历史

| 修订号 | 修订日期 | 说明 | 修改页 |
|---|---|---|---|
| 0 | 9/10 | 最初版本。 | — |
| 1 | 11/10 | 更新了*输出电压*指标。 | 5 |

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