

MAX14950A

PCIe均衡器/转接驱动器

概述

MAX14950A为双通道均衡器/转接驱动器，通过可编程输入均衡提高PCI Express® (PCIe)信号完整性。器件用于降低确定性抖动，由转接驱动电路重新建立去加重，以补偿电路板的高频损耗。器件有助于优化PCIe关键部件的布局，支持更长的带状线、微带线或电缆传输。

器件内置两个相同通道，用于均衡PCIe Gen III (8GT/s)、Gen II (5GT/s)和Gen I (2.5GT/s)信号，每个通道都具有信号空闲和接收检测功能。

MAX14950A采用小尺寸、40引脚、5.0mm x 5.0mm TQFN封装，提供顺畅的电路板引线，以优化布局并减小占用空间。器件工作在0°C至+70°C商业级温度范围。

应用

服务器
工业PC
测试设备
计算机
外置图形卡应用
通信交换机
存储局域网

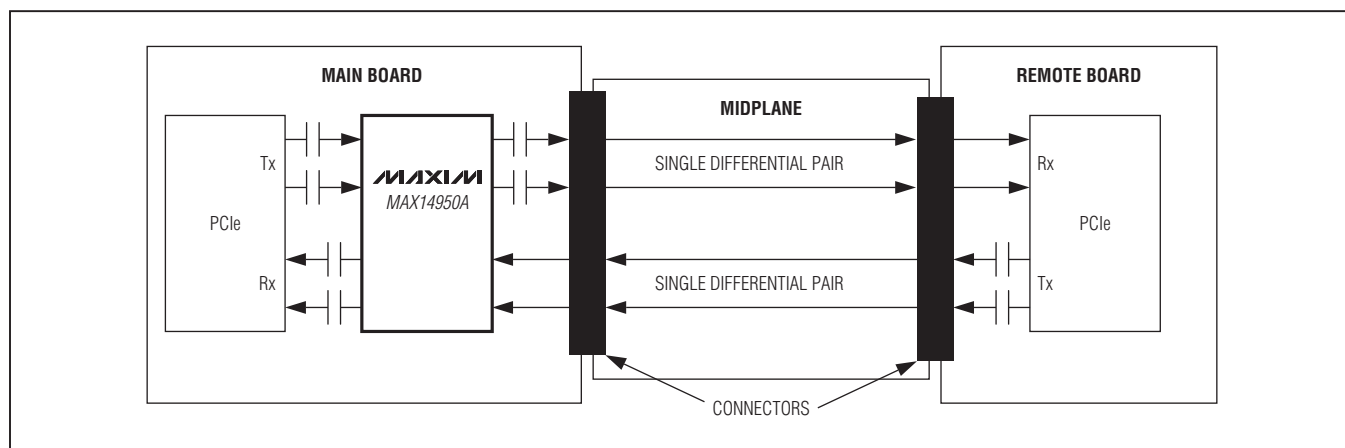
优势和特性

- ◆ 创新设计降低外部元件成本
 - ◇ +3.3V单电源供电
- ◆ 向下兼容，提高设计灵活性
 - ◇ 优化支持PCIe Gen III (8GT/s)和Gen II (5GT/s)信号，兼容于Gen I (2.5GT/s)信号
- ◆ 高度集成改善系统性能
 - ◇ 超低延迟：160ps (典型值)传输延迟
 - ◇ 输入/输出回波损耗满足PCIe Gen III (8GT/s)需求
 - ◇ 四电平可编程输入均衡
 - ◇ 八电平可编程输出去加重
 - ◇ 电路空闲状态检测
 - ◇ 接收检测允许全透明传输
- ◆ 理想用于空间敏感应用
 - ◇ 片上50Ω输入/输出端接
 - ◇ 40引脚、5.0mm x 5.0mm、TQFN封装

订购信息在数据资料的最后给出。

相关型号以及配合该器件使用的推荐产品，请参见：china.maxim-ic.com/MAX14950A.related

典型工作电路



PCI Express是PCI-SIG组织的注册服务标志。

PCIe均衡器/转接驱动器

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V_{CC}	-0.3V to +4.0V
All Other Pins (Note 1)	-0.3V to ($V_{CC} + 0.3V$)
Continuous Current I_{IN_P} , I_{IN_M} , I_{OUT_P} , I_{OUT_M}	$\pm 30mA$
Peak Current I_{IN_P} , I_{IN_M} , I_{OUT_P} , I_{OUT_M} (pulsed for 1 μs , 1% duty cycle).....	$\pm 100mA$

Continuous Power Dissipation ($T_A = +70^{\circ}C$)

TQFN (derate 35.7mW/ $^{\circ}C$ above $+70^{\circ}C$).....	2857mW
Operating Temperature Range.....	$0^{\circ}C$ to $+70^{\circ}C$
Junction Temperature Range.....	$-40^{\circ}C$ to $+150^{\circ}C$
Storage Temperature Range.....	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$
Soldering Temperature (reflow)	$+260^{\circ}C$

Note 1: All I/O pins are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	$28^{\circ}C/W$
Junction-to-Case Thermal Resistance (θ_{JC})	$2^{\circ}C/W$

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to china.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $C_{CL} = 200nF$ coupling capacitor on each output, $R_L = 50\Omega$ on each output, $T_A = 0^{\circ}C$ to $+70^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V _{CC}			3.0	3.3	3.6	V
Supply Current	I _{CC}	EN = V _{CC}	OEQ_2 = OEQ_1 = OEQ_0 = GND	102		135	mA
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V _{CC}	106		140	
			OEQ_2 = OEQ_0 = GND, OEQ_1 = V _{CC}	107		140	
			OEQ_2 = GND, OEQ_1 = OEQ_0 = V _{CC}	125		160	
			OEQ_2 = V _{CC} , OEQ_1 = OEQ_0 = GND	106		140	
			OEQ_2 = OEQ_0 = V _{CC} , OEQ_1 = GND	132		170	
			OEQ_2 = OEQ_1 = V _{CC} , OEQ_0 = GND	140		180	
			OEQ_2 = OEQ_1 = OEQ_0 = V _{CC}	165		210	

PCIe均衡器/转接驱动器

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $C_{CL} = 200nF$ coupling capacitor on each output, $R_L = 50\Omega$ on each output, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{STBY}	EN = GND	OEQ_2 = OEQ_1 = OEQ_0 = GND	57	80	mA
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V_{CC}	61	85	
			OEQ_2 = OEQ_0 = GND, OEQ_1 = V_{CC}	62	85	
			OEQ_2 = GND, OEQ_1 = OEQ_0 = V_{CC}	75	100	
			OEQ_2 = V_{CC} , OEQ_1 = OEQ_0 = GND	62	80	
			OEQ_2 = OEQ_0 = V_{CC} , OEQ_1 = GND	85	110	
			OEQ_2 = OEQ_1 = V_{CC} , OEQ_0 = GND	92	120	
			OEQ_2 = OEQ_1 = OEQ_0 = V_{CC}	120	150	
Differential Input Impedance	$Z_{RX-DIFF-DC}$	DC	80	100	120	Ω
Differential Output Impedance	$Z_{TX-DIFF-DC}$	DC	80	100	120	Ω
Common-Mode Resistance to GND, Input Termination Not Powered	$Z_{RX-HIGH-IMP-DC}$	$-150mV \leq V_{IN_CM} \leq +200mV$	50			$k\Omega$
Common-Mode Resistance to GND, Input Termination Powered	Z_{RX-DC}		20	25	30	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended (Note 4)			90	mA
Common-Mode Delta, Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$				100	mV
DC Output Offset, During Active State	$V_{TX-ACTIVE-DIFF-DC}$	$ V_{OUT_P} - V_{OUT_M} $			50	mV
DC Output Offset, During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	$ V_{OUT_P} - V_{OUT_M} $			50	mV

PCIe均衡器/转接驱动器

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $C_{CL} = 200nF$ coupling capacitor on each output, $R_L = 50\Omega$ on each output, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE (Note 4)						
Input Return Loss, Differential	RL _{RX-DIFF}	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	5			dB
Input Return Loss, Common Mode	RL _{RX-CM}	f = 0.05GHz to 2.5GHz	6			dB
		f = 2.5GHz to 4GHz	4			dB
Output Return Loss, Differential	RL _{TX-DIFF}	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	4			dB
Output Return Loss, Common Mode	RL _{TX-CM}	f = 0.05GHz to 2.5GHz	6			dB
		f = 2.5GHz to 4GHz	4			dB
Redriver-Operation Differential Input-Signal Range	V _{RX-DIFF-PP}		100		1200	mV _{P-P}
Full-Swing Differential Output Voltage (No Deemphasis)	V _{TX-DIFF-PP}	$2 \times I(V_{OUT_P} - V_{OUT_M})$, OEQ_2 = OEQ_1 = OEQ_0 = GND	800	1000	1300	mV _{P-P}
Output Deemphasis Ratio, 0dB	V _{TX-DE-RATIO-0dB}	OEQ_2 = OEQ_1 = OEQ_0 = GND, Figure 1		0		dB
Output Deemphasis Ratio, 3.5dB	V _{TX-DE-RATIO-3.5dB}	OEQ_2 = OEQ_1 = GND, OEQ_0 = V _{CC} , Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB	V _{TX-DE-RATIO-6dB}	OEQ_2 = OEQ_0 = GND, OEQ_1 = V _{CC} , Figure 1		6		dB
Output Deemphasis Ratio, 6dB with Higher Amplitude	V _{TX-DE-HA-RATIO-6dB}	OEQ_2 = GND, OEQ_1 = OEQ_0 = V _{CC} , Figure 1		6		dB
Output Deemphasis Ratio, 3.5dB with Preshoot	V _{TX-DE-PS-RATIO-3.5dB}	OEQ_2 = V _{CC} , OEQ_1 = OEQ_0 = GND, Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB with Preshoot	V _{TX-DE-PS-RATIO-6dB}	OEQ_2 = OEQ_0 = V _{CC} , OEQ_1 = GND, Figure 1		6		dB
Output Deemphasis Ratio, 9dB with Preshoot	V _{TX-DE-PS-RATIO-9dB}	OEQ_2 = OEQ_1 = V _{CC} , OEQ_0 = GND, Figure 1		9		dB
Output Deemphasis Ratio, 9dB with Preshoot and Higher Amplitude	V _{TX-DE-PS-HA-RATIO-9dB}	OEQ_2 = OEQ_1 = OEQ_0 = V _{CC} , Figure 1		9		dB
Input Equalization, 3dB	V _{RX-EQ-3dB}	INEQ_1 = INEQ_0 = GND (Note 5)		3		dB

PCIe均衡器/转接驱动器

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $C_{CL} = 200nF$ coupling capacitor on each output, $R_L = 50\Omega$ on each output, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Equalization, 5dB	$V_{RX-EQ-5dB}$	$INEQ_1 = GND$, $INEQ_0 = V_{CC}$ (Note 5)		5		dB
Input Equalization, 7dB	$V_{RX-EQ-7dB}$	$INEQ_1 = V_{CC}$, $INEQ_0 = GND$ (Note 5)		7		dB
Input Equalization, 9dB	$V_{RX-EQ-9dB}$	$INEQ_1 = INEQ_0 = V_{CC}$ (Note 5)		9		dB
Output Common-Mode Voltage	$V_{TX-CM-AC-PP}$	$MAX(V_{OUT_P} + V_{OUT_M})/2 - MIN(V_{OUT_P} + V_{OUT_M})/2$			100	mV _{P-P}
Propagation Delay	t_{PD}		120	160	240	ps
Rise/Fall Time	$t_{TX-RISE-FALL}$	(Note 6)	20			ps
Rise/Fall Time Mismatch	$t_{TX-RF-MISMATCH}$	(Note 6)			3	ps
Output Skew Same Pair	t_{SK}				5	ps
Deterministic Jitter	$t_{TX-DJ-DD}$	K28.5 pattern, AC-coupled, $R_L = 50\Omega$, no deemphasis, no preshoot, data rate = 8GT/s		10.5	23.5	ps _{P-P}
Random Jitter	$t_{TX-RJ-DD}$	D10.2 pattern, no deemphasis, no preshoot, data rate = 8GT/s			1.5	ps _{RMS}
Electrical Idle Entry Delay	$t_{TX-IDLE-SET-TO-IDLE}$	From input to output, D10.2 pattern, data rate = 1GT/s		5		ns
Electrical Idle Exit Delay	$t_{TX-IDLE-TO-DIFF-DATA}$	From input to output, D10.2 pattern, data rate = 1GT/s		5		ns
Electrical Idle Detect Threshold (Note 7)	$V_{TX-IDLE-THRESH}$	$EIL_L = EIH_H = EIH_L = GND$	65		175	mV _{P-P}
		$EIL_L = EIH_L = GND$, $EIH_H = V_{CC}$	85		215	
		$EIL_L = EIH_H = GND$, $EIH_L = V_{CC}$	25		155	
		$EIL_L = V_{CC}$, $EIH_H = EIH_L = GND$	V_{IH}	50	175	
			V_{IL}	20	165	
		$EIL_L = EIH_H = V_{CC}$, $EIH_L = GND$	V_{IH}	80	205	
			V_{IL}	50	195	
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	$I(V_{OUT_P} - V_{OUT_M})$			20	mV _{P-P}
Receiver-Detect Pulse Amplitude	$V_{TX-RCV-DETECT}$	Voltage change in positive direction			600	mV
Receiver-Detect Pulse Width				100		ns
Receiver-Detect Retry Period				200		ns

PCIe均衡器/转接驱动器

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL LOGIC						
Input-Logic Level Low	V _{IL}				0.6	V
Input-Logic Level High	V _{IH}		1.4			V
Input-Logic Hysteresis	V _{HYST}			0.1		V
Input Pulldown Resistance	R _{PD}		200	375		kΩ
ESD PROTECTION						
ESD Voltage		Human Body Model (HBM)		±4		kV

- Note 3:** All devices are 100% production tested at T_A = +70°C. Specifications over operating temperature range are guaranteed by design.
- Note 4:** Guaranteed by design, unless otherwise noted.
- Note 5:** Equivalent to same amount of deemphasis driving the input.
- Note 6:** Rise and fall times are measured using 20% and 80% levels.
- Note 7:** Electrical idle detect threshold is measured using D10.2 pattern and data rate = 1GT/s.

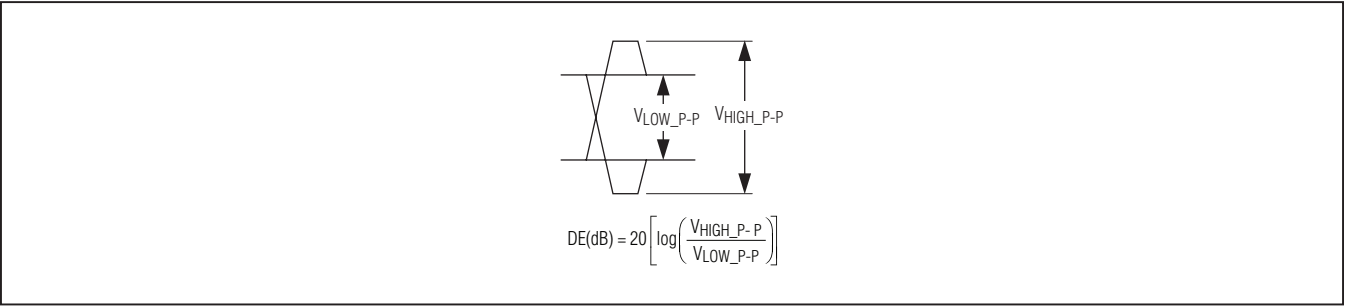


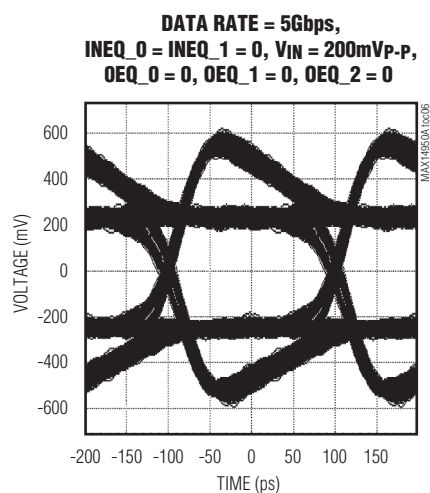
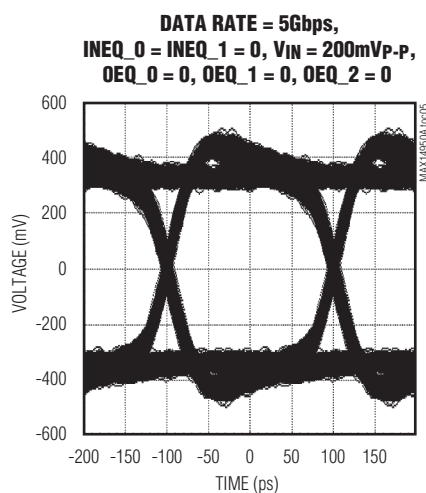
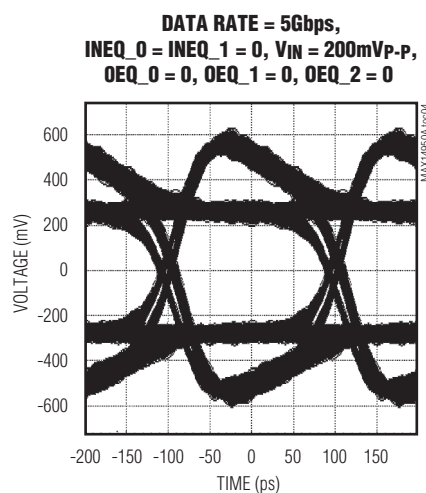
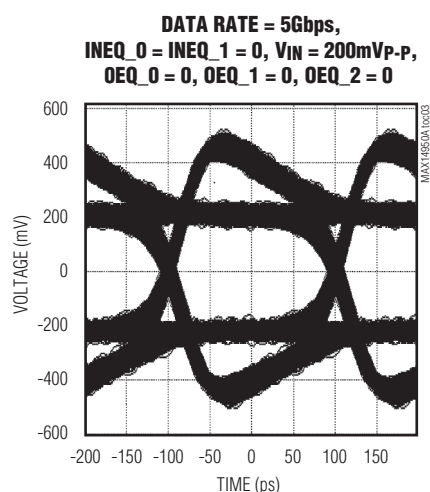
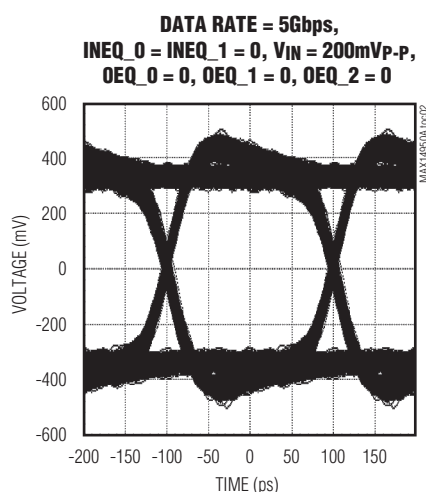
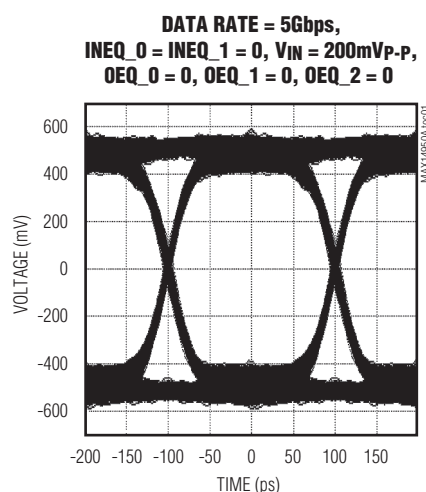
图1. 输出去加重

MAX14950A

PCIe均衡器/转接驱动器

典型工作特性

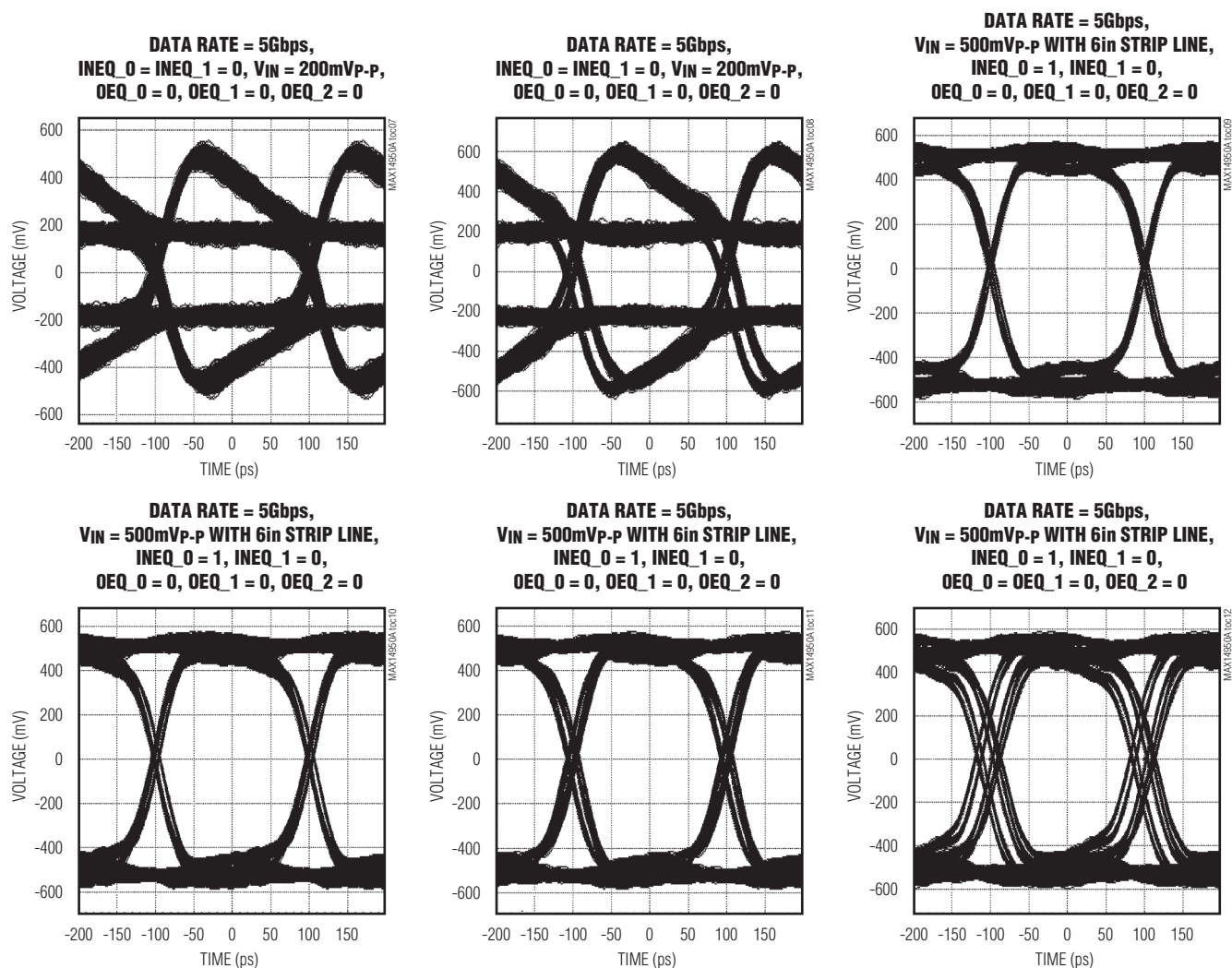
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



PCIe均衡器/转接驱动器

典型工作特性(续)

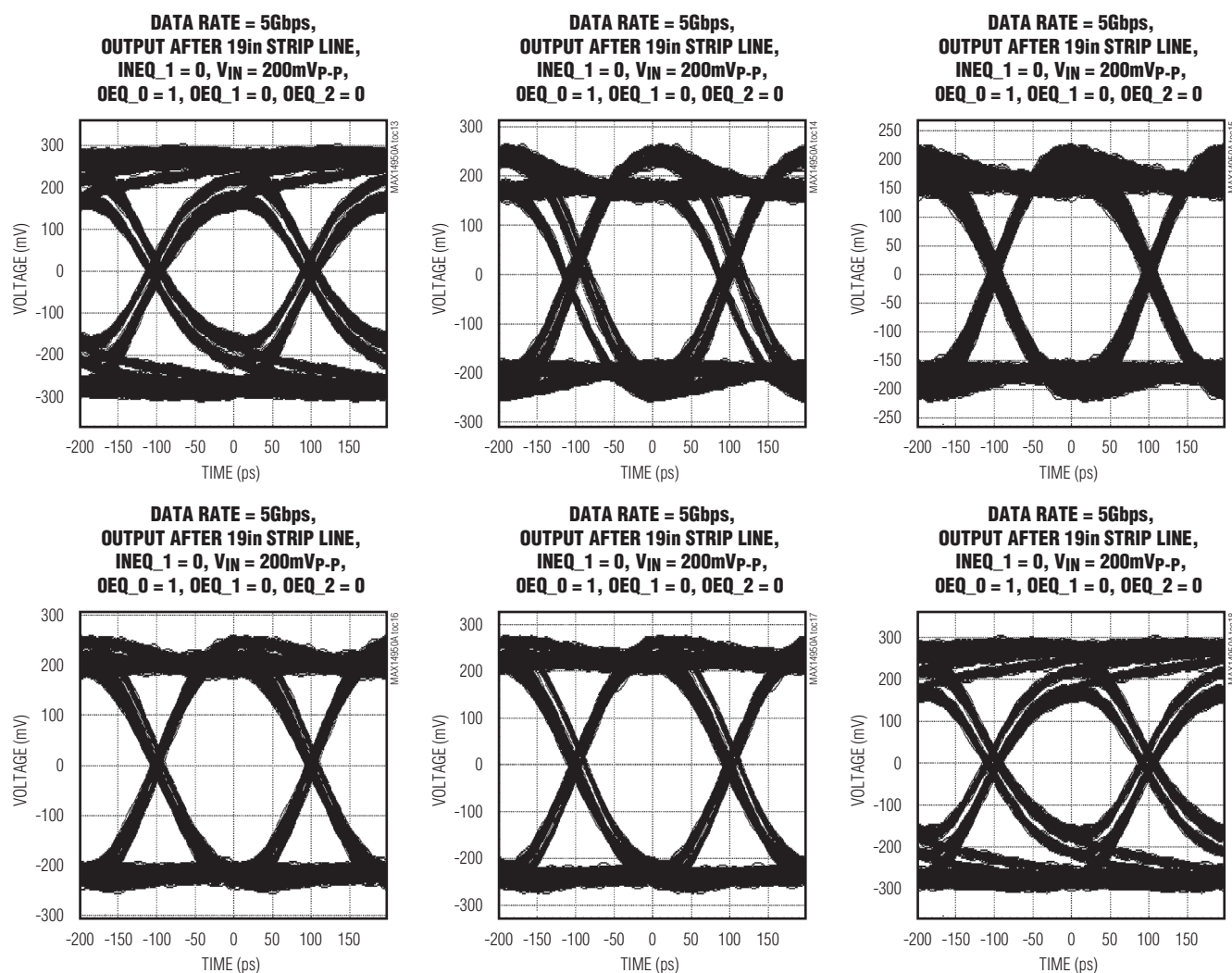
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



PCIe均衡器/转接驱动器

典型工作特性(续)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

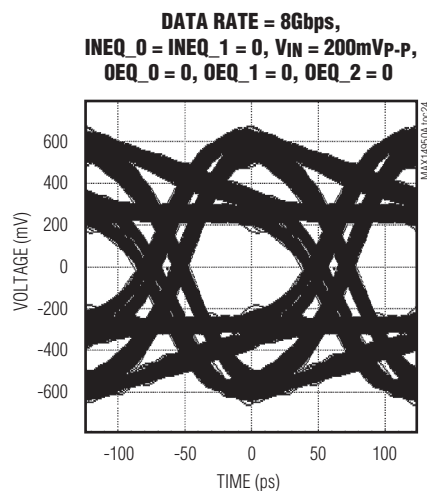
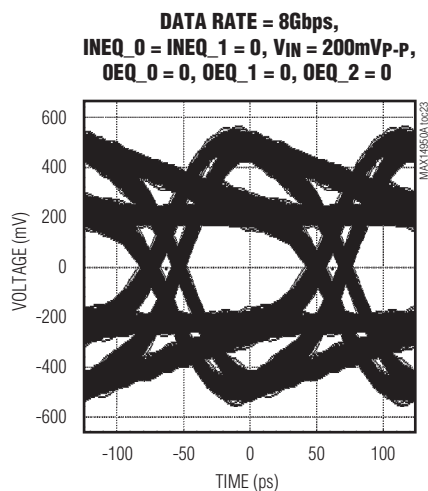
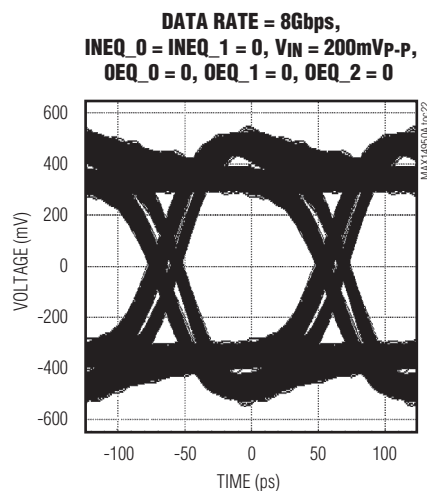
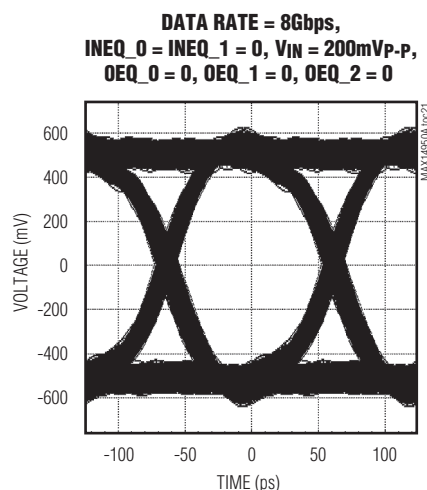
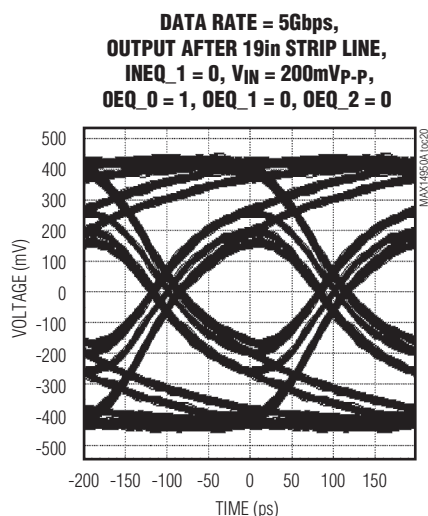
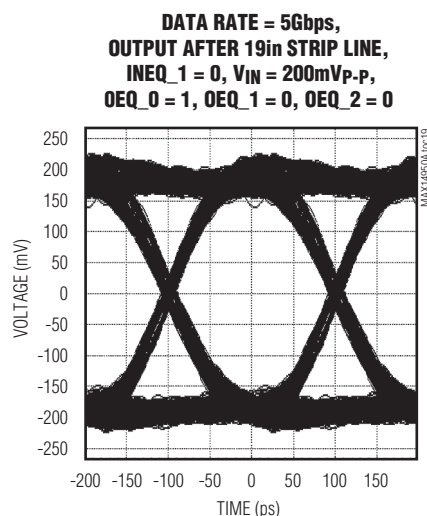


MAX14950A

PCIe均衡器/转接驱动器

典型工作特性(续)

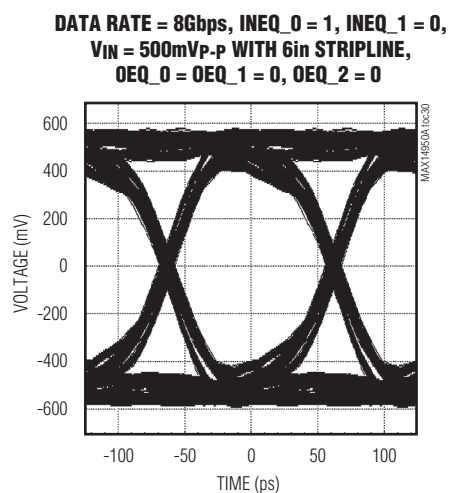
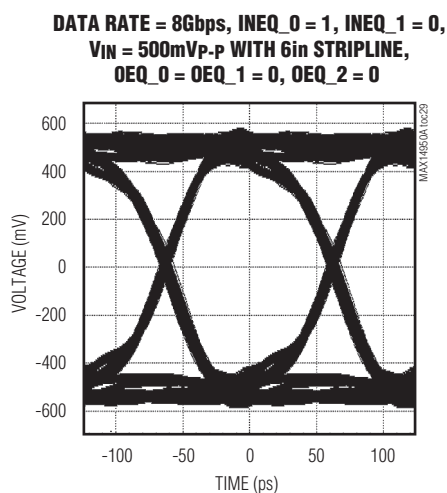
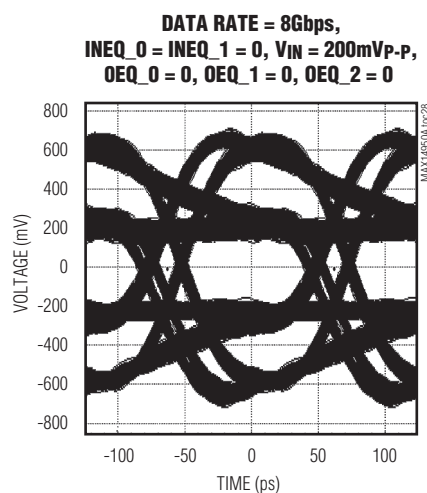
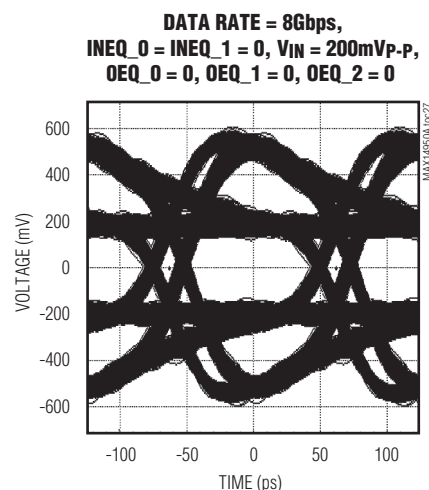
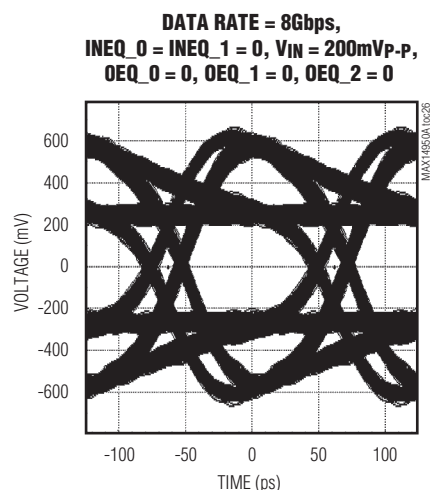
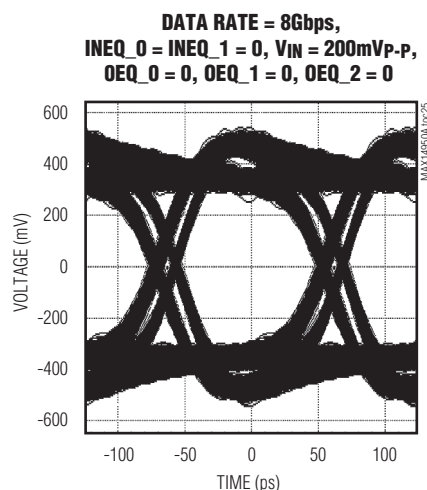
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



PCIe均衡器/转接驱动器

典型工作特性(续)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

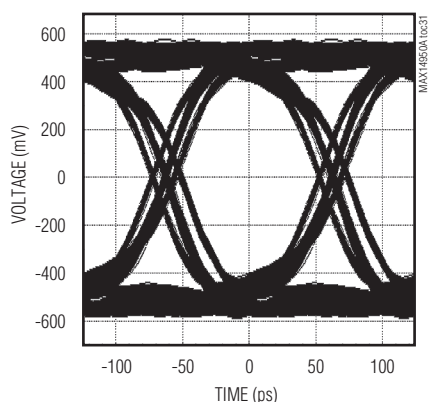


PCIe均衡器/转接驱动器

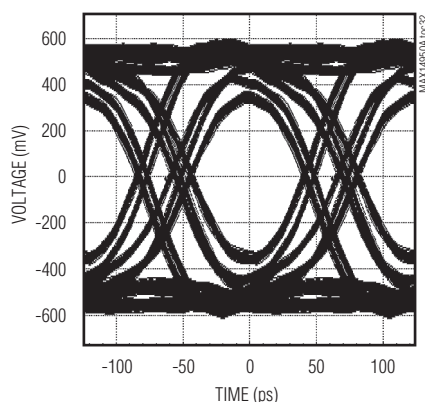
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

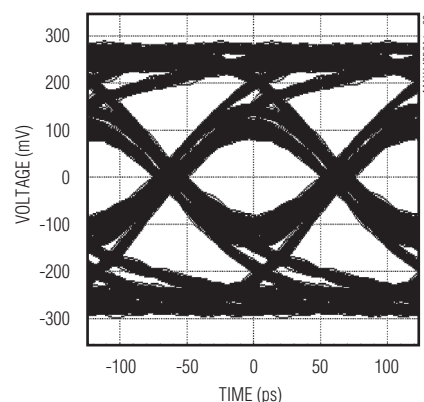
DATA RATE = 8Gbps, INEQ_0 = 1, INEQ_1 = 0,
V_{IN} = 500mVp-p WITH 6in STRIPLINE,
OEQ_0 = OEQ_1 = 0, OEQ_2 = 0



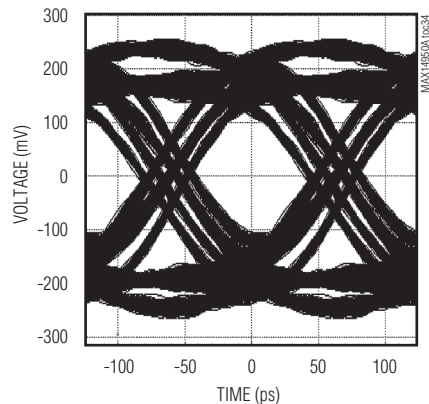
DATA RATE = 8Gbps, INEQ_0 = 1, INEQ_1 = 0,
V_{IN} = 500mVp-p WITH 6in STRIPLINE,
OEQ_0 = OEQ_1 = 0, OEQ_2 = 0



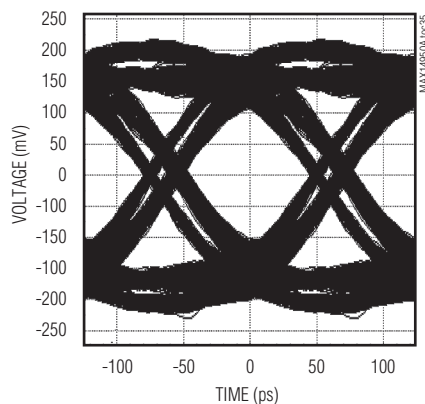
DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
V_{IN} = 200mVp-p,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0



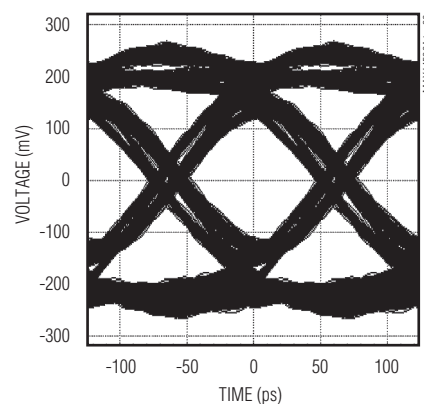
DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
V_{IN} = 200mVp-p,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0



DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
V_{IN} = 200mVp-p,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0



DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
V_{IN} = 200mVp-p,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0

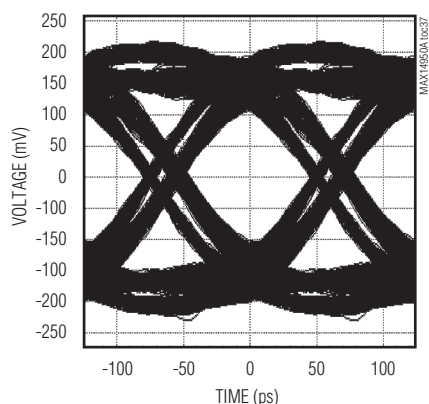


PCIe均衡器/转接驱动器

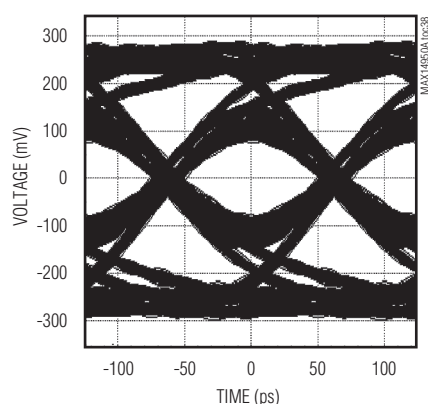
典型工作特性(续)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

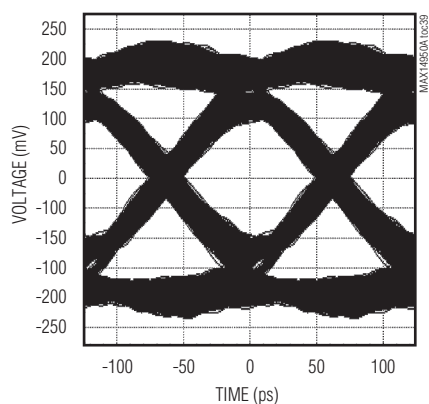
**DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
 $V_{IN} = 200mVp-p$,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0**



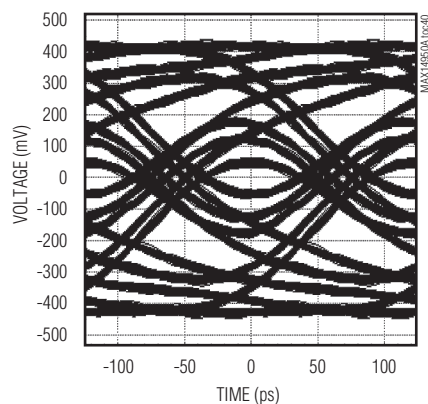
**DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
 $V_{IN} = 200mVp-p$,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0**



**DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
 $V_{IN} = 200mVp-p$,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0**



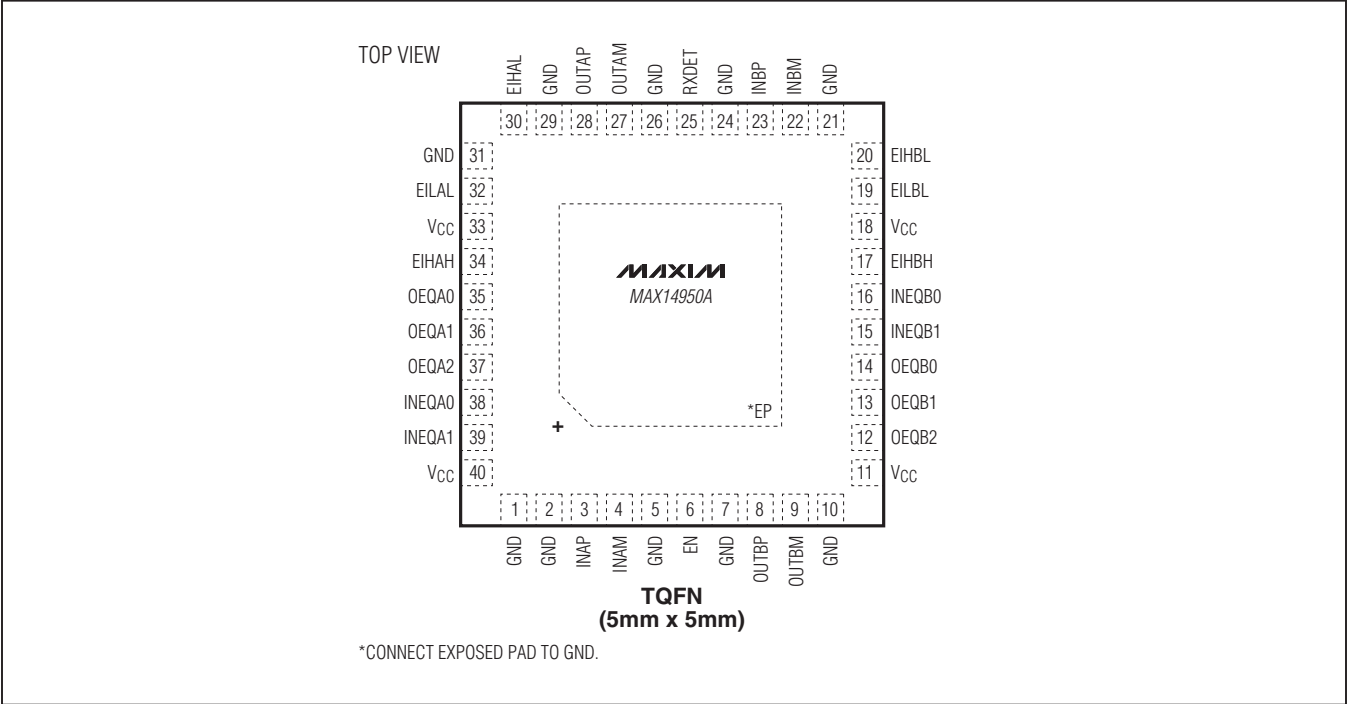
**DATA RATE = 8Gbps, OUTPUT AFTER
19in STRIPLINE, INEQ_0 = INEQ_1 = 0,
 $V_{IN} = 200mVp-p$,
OEQ_0 = 1, OEQ_1 = 0, OEQ_2 = 0**



MAX14950A

PCIe均衡器/转接驱动器

引脚配置



引脚说明

引脚	名称	功能
1, 2, 5, 7, 10, 21, 24, 26, 29, 31	GND	地。
3	INAP	同相输入，通道A。
4	INAM	反相输入，通道A。
6	EN	使能输入，EN为低电平时，器件处于待机模式；EN为高电平时，器件处于正常工作模式。EN具有375kΩ (典型值)内部下拉电阻。
8	OUTBP	同相输出，通道B。
9	OUTBM	反相输出，通道B。
11, 18, 33, 40	V _{CC}	电源输入，利用0.1μF和0.01μF并联电容将V _{CC} 旁路至GND，电容尽量靠近器件放置。
12	OEQB2	输出去加重控制MSB，通道B。OEQB2具有375kΩ (典型值)内部下拉电阻。
13	OEQB1	输出去加重第1位，通道B。OEQB1具有375kΩ (典型值)内部下拉电阻。
14	OEQB0	输出去加重控制LSB，通道B。OEQB0具有375kΩ (典型值)内部下拉电阻。
15	INEQB1	输入均衡控制MSB，通道B。INEQB1具有375kΩ (典型值)内部下拉电阻。
16	INEQB0	输入均衡控制LSB，通道B。INEQB0具有375kΩ (典型值)内部下拉电阻。

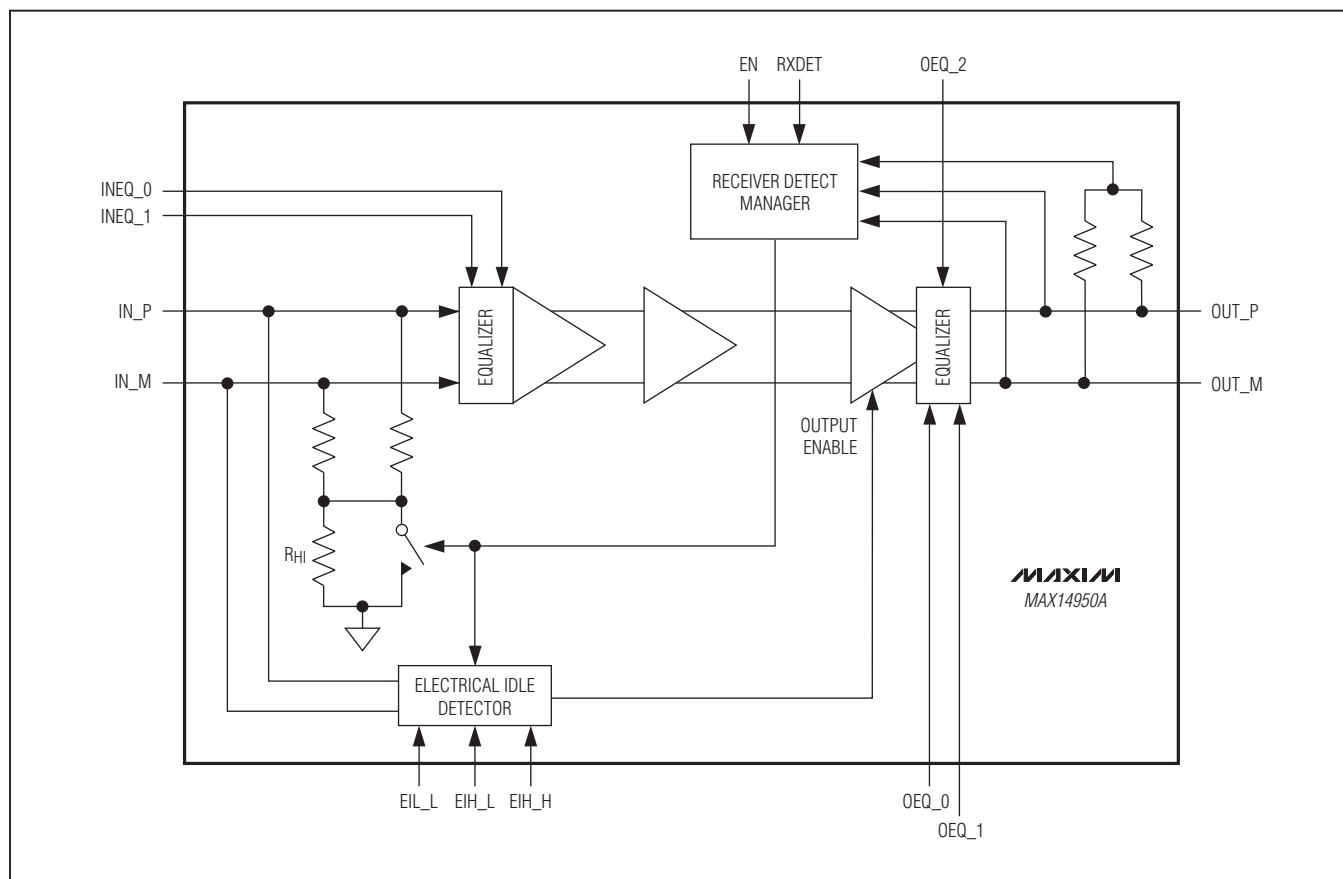
PCIe均衡器/转接驱动器

引脚说明(续)

引脚	名称	功能
17	EIHBH	空闲状态检测上限递增控制位，通道B。EIHBH具有375k Ω (典型值)内部下拉电阻。
19	EILBL	空闲状态检测下限递减控制位，通道B。EILBL具有375k Ω (典型值)内部下拉电阻。
20	EIHL	空闲状态检测上限递减控制位，通道B。EIHL具有375k Ω (典型值)内部下拉电阻。
22	INBM	反相输入，通道B。
23	INBP	同相输入，通道B。
25	RXDET	接收器检测控制位。触发RXDET，以启动接收检测功能。RXDET具有375k Ω (典型值)内部下拉电阻。
27	OUTAM	反相输出，通道A。
28	OUTAP	同相输出，通道A。
30	EIHAL	空闲状态检测上限递减控制位，通道A。EIHAL具有375k Ω (典型值)内部下拉电阻。
32	EILAL	空闲状态检测下限递减控制位，通道A。EILAL具有375k Ω (典型值)内部下拉电阻。
34	EIHAH	空闲状态检测上限递增控制位，通道A。EIHAH具有375k Ω (典型值)内部下拉电阻。
35	OEQA0	输出去加重控制LSB，通道A。OEQA0具有375k Ω (典型值)内部下拉电阻。
36	OEQA1	输出去加重控制第1位，通道A。OEQA1具有375k Ω (典型值)内部下拉电阻。
37	OEQA2	输出去加重控制MSB，通道A。OEQA2具有375k Ω (典型值)内部下拉电阻。
38	INEQA0	输入均衡控制LSB，通道A。INEQA0具有375k Ω (典型值)内部下拉电阻。
39	INEQA1	输入均衡控制MSB，通道A。INEQA1具有375k Ω (典型值)内部下拉电阻。
—	EP	裸焊盘，内部连接至GND。将EP连接至较大的接地区域，以改善散热和对地的热传导性。不要将EP作为唯一的GND连接点。

PCIe均衡器/转接驱动器

功能框图



详细说明

MAX14950A双通道均衡器/转接驱动器支持Gen III (8GT/s)、Gen II (5GT/s)和Gen I (2.5GT/s) PCIe数据率。器件含有两路相同的驱动器，每个通道都具有空闲/接收检测功能，以及均衡/去加重/预冲，用以补偿电路板损耗。可编程输入均衡电路降低确定性抖动，改善信号完整性。器件具有可编程输出去加重/预冲功能，优化关键PCIe元件布局，支持更长的带状线、微带线或电缆传输。

可编程输入均衡

通道A的可编程输入均衡由INEQA1和INEQA0位控制，通道B的可编程输入均衡由INEQB1和INEQB0位控制(表1)。

表1. 输入均衡

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	0	3
0	1	5
1	0	7
1	1	9

PCIe均衡器/转接驱动器

表2. 输出去加重/预冲

OEQ_2	OEQ_1	OEQ_0	OUTPUT DEEMPHASIS RATIO (dB)	PRESHOOT
0	0	0	0 ¹	No
0	0	1	3.5 ¹	No
0	1	0	6 ¹	No
0	1	1	6 ²	No
1	0	0	3.5 ¹	Yes
1	0	1	6 ¹	Yes
1	1	0	9 ³	Yes
1	1	1	9 ¹	Yes

¹ 峰-峰摆幅为1.0V_o。² 峰-峰摆幅为1.2V_o。³ 峰-峰摆幅为0.9V_o。

表3. 接收器检测输入功能

RXDET	EN	DESCRIPTION
X	0	Receiver detection is inactive
X	1	Following a rising edge of EN signal, indefinite retry until a receiver is detected for at least one channel. Retries stop a few times after any channel is detected.
Rising/Falling Edge	1	Initiate receiver detection

X = 无关。

表4. 空闲状态检测门限设置

EIL_L	EIH_H	EIH_L	THRESHOLD LOW LIMIT (typ) (mV)	THRESHOLD HIGH LIMIT (typ) (mV)
0	0	0	118	120
0	0	1	88	90
0	1	0	148	150
0	1	1	Not Valid	Not Valid
1	0	0	92	107
1	0	1	Not Valid	Not Valid
1	1	0	125	135
1	1	1	Not Valid	Not Valid

可编程输出去加重

通道A的可编程输出去加重/预冲由OEQA2、OEQA1、OEQA0三位控制，通道B的可编程输出去加重/预冲由OEQB2、OEQB1、OEQB0三位控制(表2)。

接收器检测

器件在每个通道都具有接收器检测功能。初始上电时，如果EN为高电平，启动接收器检测功能。EN为高电平时，可在RXDET输入的上升或下降沿启动接收器检测功能。在此期间，器件保持低功耗待机模式，即使EN为高电平也将禁止输出。连续监测每个通道的接收器，直到检测到通道接收的有效信号。如果一个通道检测到接收信号，将限制另一通道的重试次数。接收器检测功能使能后，使能输入共模匹配电阻和空闲状态检测(表3)。

空闲状态检测

器件具有空闲状态检测功能，避免把噪声信号转接驱动到输出端。当差分输入下降到空闲状态检测门限的下限时，禁止输出。差分输入信号高于空闲状态门限的上限时，器件打开输出并转接驱动信号。每个通道的空闲状态检测门限可独立设置。如表4所示，驱动通道A的EIH_{AL}、EIL_{AL}和EIH_{AH}及通道B的EIH_{BL}、EIL_{BL}和EIH_{BH}，分别设置空闲门限的上限和下限。空闲状态和转接驱动模式之间的输出共模电压略有差异。

PCIe均衡器/转接驱动器

应用信息

布局

电路板布局和设计对器件性能的影响非常显著。采用良好的高频设计技术，包括尽可能降低接地电感，采用阻抗受控的数据信号传输线等。电源去耦电容须尽量靠近VCC安装，VCC必须始终连接到电源区域。建议在不同电路板层布置接收器和发送器，使串扰降至最小。

裸焊盘封装

带裸焊盘的40引脚TQFN封装为IC散热提供了极低的热阻通路。器件的裸焊盘必须焊接至电路板接地区域，以改善散热。关于裸焊盘封装的更多信息，请参考Maxim应用笔记HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

电源排序

注意：请勿超出绝对最大额定值，如果工作条件超出器件的额定值，将会造成器件永久损坏。

建议对所有器件提供适当的供电顺序。任何情况下，需要先施加GND和VCC，然后再施加信号，特别是在信号没有限流的条件下。

订购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX14950ACTL+	0°C to +70°C	40 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。

*EP = 裸焊盘。

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询china.maxim-ic.com/packages。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
40 TQFN-EP	T4055+2	21-0140	90-0002

MAX14950A

PCIe均衡器/转接驱动器

修订历史

修订号	修订日期	说明	修改页
0	6/11	最初版本。	—

Maxim北京办事处

北京8328信箱 邮政编码100083

免费电话：800 810 0310

电话：010-6211 5199

传真：010-6211 5299

Maxim不对Maxim产品以外的任何电路使用负责，也不提供其专利许可。Maxim保留在任何时间、没有任何通报的前提下修改产品资料和规格的权利。

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 _____ **19**

© 2011 Maxim Integrated Products

Maxim是Maxim Integrated Products, Inc.的注册商标。