19-6188; Rev 0; 7/12
备有评估板

MAX2091

50MHz至500MHz模拟VGA、1735MHz至1935MHz上变频混频器，带镜频滤波、门限报警电路和用于电平控制的误差放大器

概述

MAX2091单芯片SiGeBiCMOS上变频器IC集成了模拟可变增益放大器(VGA)、上变频混频器器和镜频滤波器。器件对250MHz至450MHz IF信号进行放大，然后与LO信号混频，并为所产生的1735MHz至1935MHz上变频信号提供片上滤波，作为信号处理的最后一级。如需不含镜频滤波器的器件，请参考MAX2091B。

模拟衰减器由外部模拟电压控制，器件具有23dB增益(无衰减)、5.4dB NF(无衰减，包括衰减器插入损耗)和+24.5dBm OIP3。所有这些特性都使MAX2091成为各种发射器系统的理想上变频器选择。与MAX2092 RF VGA配对使用时，构成完备的2芯片IF–RF信号调理方案，用于微波点对点发射设备。

MAX2091采用5V单电源供电，提供紧凑的20引脚TQFN封装(5mm x 5mm)，带有裸焊盘。在TC = -40°C至+95°C扩展级温度范围内确保电气性能。

应用

微波点对点发射器

IF可变增益放大器

温补电路

蜂窝系统

WiMAX®应用

LTE应用

固定宽带无线接入

无线本地环路

军用设备

优势和特性

- 单芯片IC实现完备的上变频
  - ✧ 50MHz至500MHz模拟VGA
  - ✧ 1735MHz至1935MHz上变频混频器
  - ✧ 片上LO缓冲器
  - ✧ 镜频滤波
- 高线性度
  - ✧ +24.5dBm OIP3
  - ✧ +12dBm输出-1dB压缩点
- 23dB增益
- 37dB IF衰减器控制范围
- 5.4dB噪声系数(包括衰减器插入损耗)
- 整个100MHz带宽内增益波动仅为0.25dB
- 模拟衰减器，由外部电压控制
- 可调门限报警
- 20dB镜频抑制，抑制1135MHz RF频率
- 单+5V供电，电源电压范围可扩展至：+4.75V至+5.8V
- 无铅封装
- 关断功能

定购信息在数据资料的最后给出。

相关型号以及配合该器件使用的推荐产品，请参见：china.maximintegrated.com/MAX2091.related。

WiMAX是WiMAX Forum. 注册的认证及服务商标。

ABSOLUTE MAXIMUM RATINGS

V_{CC_A}, V_{CC_IF}, V_{CC_LO}, V_{CC_RF} ..... -0.3V to +6V
IF_IN, MIX_IN, IF_OUT, LO+, RF_OUT ..... -0.3V to V_{CC} + 0.3V
ALM, R_BIAS, DET_VIN, AMP_OUT, LO- ..... -0.3V to +3.6V
ALM_THRES, PLVLSET,
CTRL1, CTRL2 ..... -0.3V to MINIMUM (V_{CC} + 0.3V, +3.6V)
IF_IN, MIX_IN Input Power ..... +15dBm
Continuous Power Dissipation (Note 1) 2.5W

Operating Case Temperature
Range (Note 2) ..... -40°C to +95°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering 10s) ..... 300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

Junction-to-Ambient Thermal Resistance (θ_{JA})
(Notes 3, 4) ..... +29°C/W

Junction-to-Case Thermal Resistance (θ_{JC})
(Notes 1, 4) ..... +7°C/W

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.8V, V_{GND} = 0V, P_{LO} = -10dBm to -4dBm, and T_C = -40°C to +95°C. Typical values are at V_{CC} = 5.5V, P_{LO} = -7dBm, and T_C= +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.5	5.8	V
Total Supply Current	I_{DC}	CTRL1 = 1, CTRL2 = 1		264	290	mA
		CTRL1 = 1, CTRL2 = 0		254		
		CTRL1 = 0, CTRL2 = 0		8.5	15	
CTRL1/CTRL2 Logic-Low Input Voltage	V_{IL}				0.8	V
CTRL1/CTRL2 Logic-High Input Voltage	V_{IH}		2.2			V
CTRL1/CTRL2 Input Logic Current	I_{IH}/I_{IL}		-10		10	µA
PLVLSET Input Resistance	R_{IN}		650			kΩ
PLVLSET Input Voltage Range			0		2.5	V
PLVLSET Minimum Control Voltage			0	0.1	0.2	V
PLVLSET Maximum Control Voltage			2.3	2.4	2.5	V
DET_IN Input Voltage Range	V_{IN}		0		2.5	V
ALM_THRES Input Resistance			90	135		kΩ
Alarm Output Logic 1			3.135	3.3	3.465	V
Alarm Output Logic 0					0.4	V
DET_VIN Input Resistance			175	235	295	kΩ

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF Frequency	f_{RF}	(Note 6)	1685		1985	MHz
LO Frequency	f_{LO}	(Note 6)	1185	1485	2485	MHz
IF_IN Frequency	f_{IF_IN}	(Note 6)	50		500	MHz
MIX_IN Frequency	f_{MIX_IN}	(Note 6)	100		500	MHz
LO Power	P_{LO}		-10		-4	dBm

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit* with analog attenuator set to maximum gain, V_{CC} = 4.75V to 5.8V, f_{RF} = 1835MHz, f_{LO} = 1485MHz, f_{IF} = 350MHz, $f_{RF} = f_{LO} + f_{IF}$, P_{LO} = -10dBm to -4dBm, T_C = -40°C to +95°C, and IF_IN, LO+, and RF_OUT ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{LO} = -7dBm, P_{IF} = -25dBm, $V_{PLVLSET}$ = 2.5V, CTRL1 = logic 1, CTRL2 = logic 0. Min/max specifications apply over supply, process, and temperature, unless otherwise noted. (Notes 5, 7, 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VGA + 2.5dB PAD + MIXER CASCADE						
Small-Signal Gain	G		20	23	26	dB
Gain vs. Temperature				-0.016		dB/C
Gain Variation vs. Frequency (Note 9)		1835MHz ± 50MHz		0.25		dB
		1835MHz ± 80MHz		0.4		
		1835MHz ± 100MHz		0.6		
Noise Figure	NF			5.4		dB
Total Attenuation Range		$V_{PLVLSET}$ = 0.2V to 2.5V	35	37		dB
Group-Delay Variation		Within ±50MHz		133		ps
		Within ±80MHz		220		
		Within ±100MHz		285		
Spurious Response		LO + 2IF, P_{RF_OUT} = -2dBm		60		dBc
		LO - 2IF, P_{RF_OUT} = -2dBm		70		
		LO + 3IF, P_{RF_OUT} = -2dBm		67		
		LO - 3IF, P_{RF_OUT} = -2dBm		77		
Output Third-Order Intercept Point	OIP3	P_{RF_OUT} = -2dBm/tone, $f_{RF2} - f_{RF1}$ = 1MHz		24.5		dBm
Output -1dB Compression Point	P_{1dB}			12		dBm
LO Leakage at IF_IN				-60		dBm
IF_IN Return Loss				21		dB
		f_{IF} = 140MHz		17.5		
LO+ Port Return Loss				24		dB
RF_OUT Return Loss				19.6		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit* with analog attenuator set to maximum gain, V_{CC} = 4.75V to 5.8V, f_{RF} = 1835MHz, f_{LO} = 1485MHz, f_{IF} = 350MHz, $f_{RF} = f_{LO} + f_{IF}$, P_{LO} = -10dBm to -4dBm, T_C = -40°C to +95°C, and IF_IN, LO+, and RF_OUT ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{LO} = -7dBm, P_{IF} = -25dBm, $V_{PLVLSET}$ = 2.5V, CTRL1 = logic 1, CTRL2 = logic 0. Min/max specifications apply over supply, process, and temperature, unless otherwise noted. (Notes 5, 7, 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IF VGA (ATTENUATOR + AMPLIFIER)						
Small-Signal Gain			23.5	26	27.5	dB
Noise Figure				4.0		dB
Output Third-Order Intercept Point	OIP3	Up to 30dB attenuation, P_{IF_OUT} = 0dBm/tone, $f_{RF2} - f_{RF1}$ = 1MHz		38.8		dBm
Output Second-Order Intercept Point	OIP2	P_{IF_OUT} = 0dBm/tone, $f_{RF2} - f_{RF1}$ = 1MHz		57.4		dBm
Output Second Harmonic		P_{IF_OUT} = 0dBm		64.5		dBc
Output Third Harmonic		P_{IF_OUT} = 0dBm		80.0		dBc
Output -1dB Compression Point	P_{1dB}			17.6		dBm
Average Gain-Control Slope		$V_{PLVLSET}$ = 0.5V to 2.0V	16.5	19.5	23.0	dB/V
Maximum Gain-Control Slope		$V_{PLVLSET}$ = 0V to 2.5V		25		dB/V
VGA Reverse Isolation				35		dB
Attenuator Response Time		P_{IF_IN} = -15dBm, $V_{PLVLSET}$ = 2.5V to 1.2V, output settled to within ±0.5dB of final value		330		ns
		P_{IF_IN} = -15dBm, $V_{PLVLSET}$ = 1.2V to 2.5V, output settled to within ±0.5dB of final value		220		
Insertion Phase Change		$V_{PLVLSET}$ = 2.5V to 0V		11.4		Degrees
MIXER WITH IMAGE REJECT FILTER						
Conversion Gain	G		-2.2	-0.5	1.5	dB
SSB Noise Figure	NF			17.1		dB
Output Third-Order Intercept Point	OIP3			24.7		dBm
Output -1dB Compression Point	P_{1dB}			12.2		dBm
Image Rejection		f_{IF} = 350MHz ± 50MHz	15	20		dB
LO Leakage at RF_OUT				-41		dBm
2LO Leakage at RF_OUT				-35		dBm
Second Harmonic	HD2	P_{RF_OUT} = -2dBm		65		dBc
Third Harmonic	HD3	P_{RF_OUT} = -2dBm		77.5		dBc
3LO + IF Spur		P_{RF_OUT} = -2dBm		33		dBc
MIX_IN Return Loss				22		dB
LO+ Port Return Loss				24		dB
RF_OUT Return Loss				20		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit* with analog attenuator set to maximum gain, V_{CC} = 4.75V to 5.8V, f_{RF} = 1835MHz, f_{LO} = 1485MHz, f_{IF} = 350MHz, f_{RF} = f_{LO} + f_{IF}, P_{LO} = -10dBm to -4dBm, T_C = -40°C to +95°C, and IF_IN, LO+, and RF_OUT ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{LO} = -7dBm, P_{IF} = -25dBm, $V_{PLVLSET}$ = 2.5V, CTRL1 = logic 1, CTRL2 = logic 0. Min/max specifications apply over supply, process, and temperature, unless otherwise noted. (Notes 5, 7, 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER AND ALARM CIRCUIT (CTRL1 = CTRL2 = LOGIC 1)						
Maximum AMP_OUT Capacitance to GND		(Note 6)			20	pF
ALM Threshold		Input = DET_VIN		1.35		V

Note 5: Min and max limits are production tested, and guaranteed at T_C = +95°C for worst-case supply voltage and frequency.

Note 6: Recommended functional range, not production tested. Operation outside this range is possible, but with degraded performance of some parameters.

Note 7: All limits include external component and PCB losses. Output measurements taken at the RF port of the *Typical Application Circuit*.

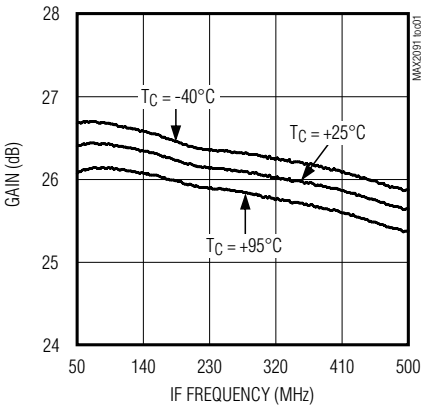
Note 8: It is advisable not to continuously operate the VGA IF_IN and MIX_IN above +11dBm.

Note 9: Gain variation after slope compensation with external equalizer in position R2–R4 in the *Typical Application Circuit*.

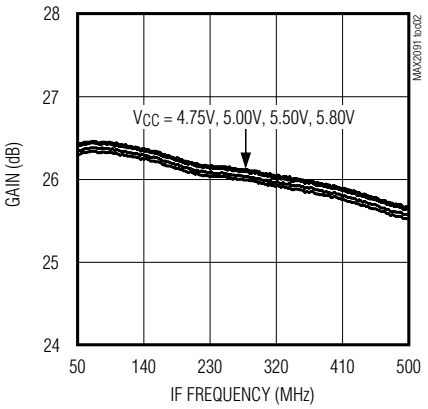
典型工作特性

(*Typical Application Circuit* **configured for AGC amp only (IF_IN to IF_OUT)**, analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

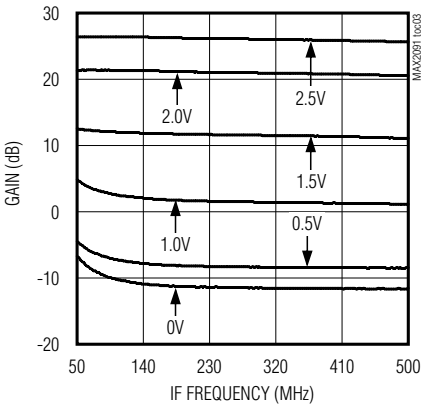
GAIN vs. IF FREQUENCY



GAIN vs. IF FREQUENCY



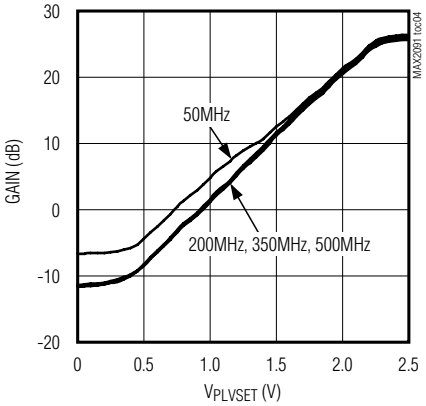
GAIN OVER PLVSET SETTING vs. IF FREQUENCY



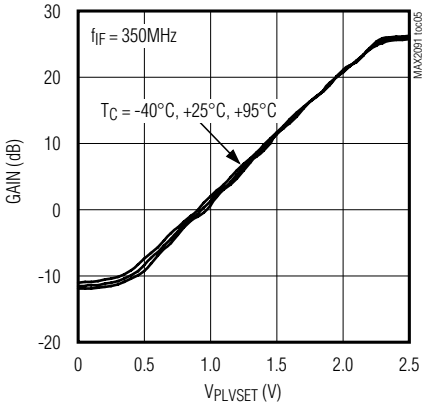
典型工作特性(续)

(*Typical Application Circuit* **configured for AGC amp only (IF_IN to IF_OUT)**, analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

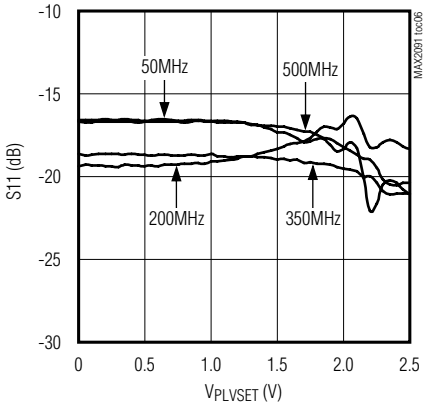
GAIN vs. V_{PLVSET} SETTING



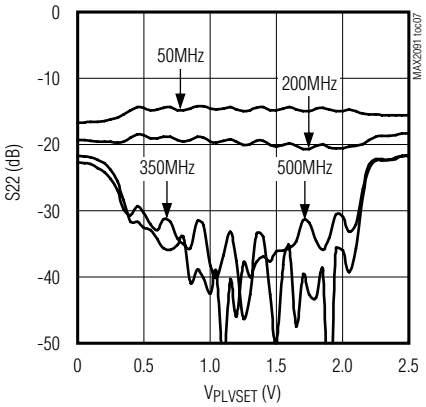
GAIN vs. V_{PLVSET} SETTING



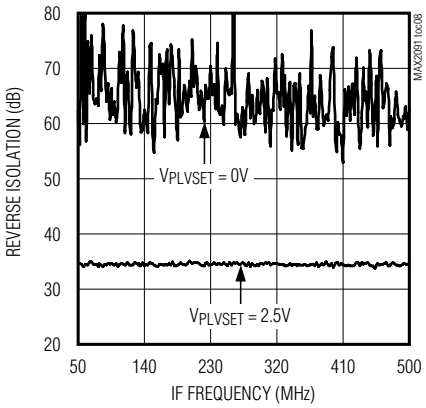
INPUT MATCH vs. V_{PLVSET} SETTING



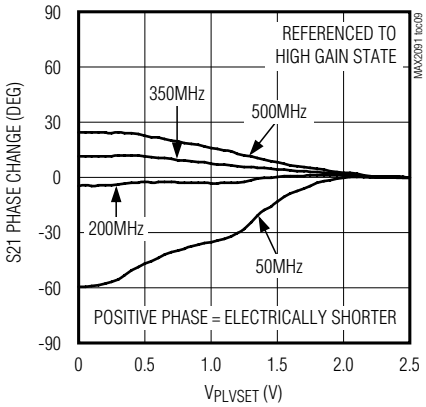
OUTPUT MATCH vs. V_{PLVSET} SETTING



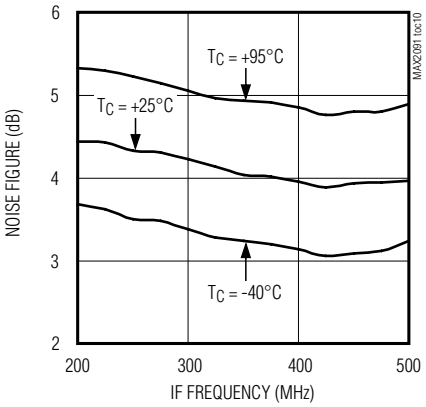
REVERSE ISOLATION OVER V_{PLVSET} SETTING vs. IF FREQUENCY



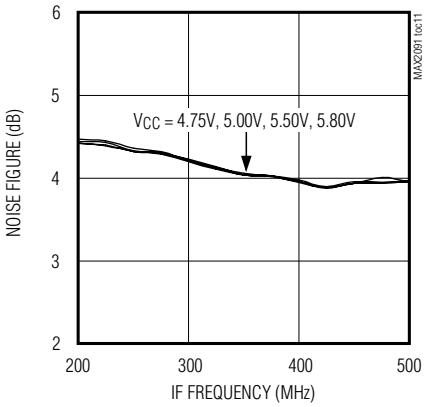
S21 PHASE CHANGE vs. V_{PLVSET} SETTING



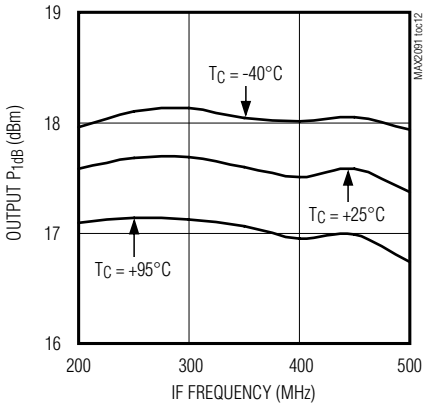
NOISE FIGURE vs. IF FREQUENCY



NOISE FIGURE vs. IF FREQUENCY



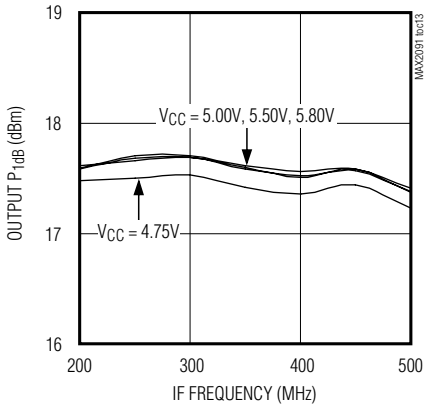
OUTPUT P_{1dB} vs. IF FREQUENCY



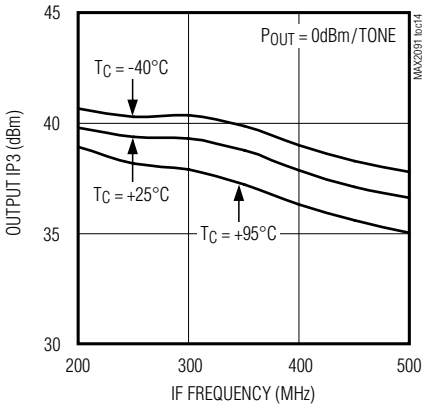
典型工作特性(续)

(*Typical Application Circuit* **configured for AGC amp only (IF_IN to IF_OUT)**, analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

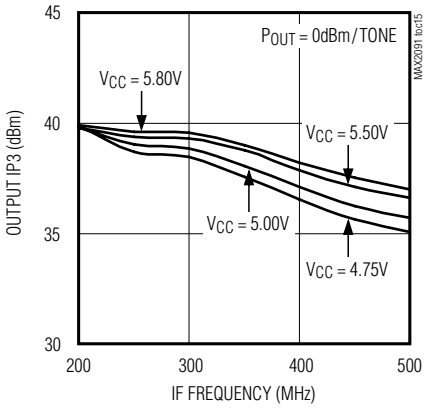
OUTPUT P_{1dB} vs. IF FREQUENCY



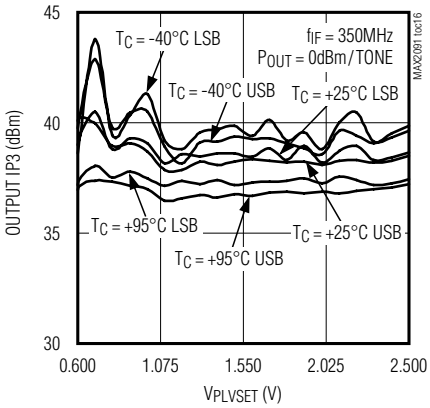
OUTPUT IP3 vs. IF FREQUENCY



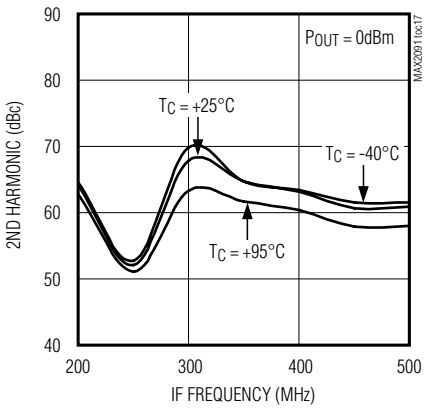
OUTPUT IP3 vs. IF FREQUENCY



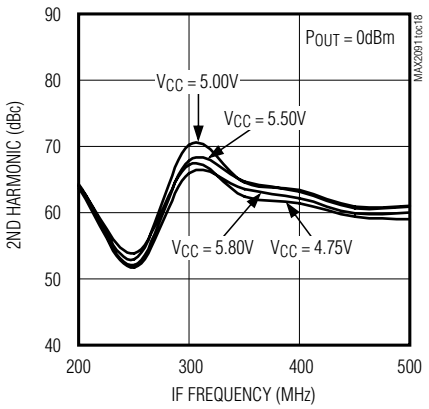
OUTPUT IP3 vs. V_{PLVSET} SETTING



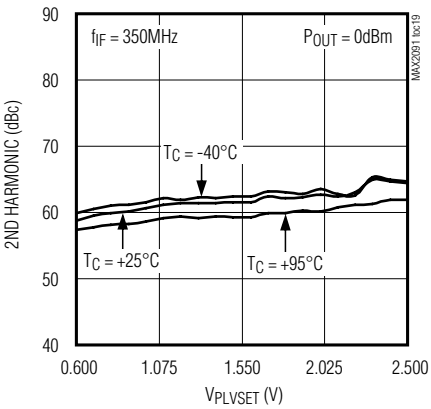
2ND HARMONIC vs. IF FREQUENCY



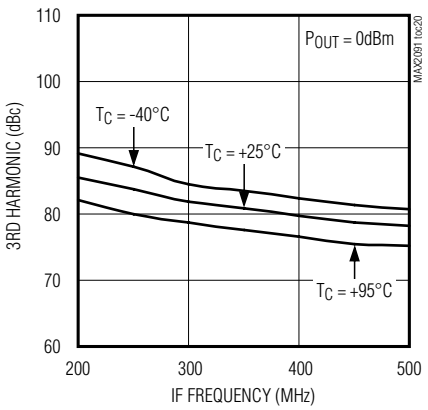
2ND HARMONIC vs. IF FREQUENCY



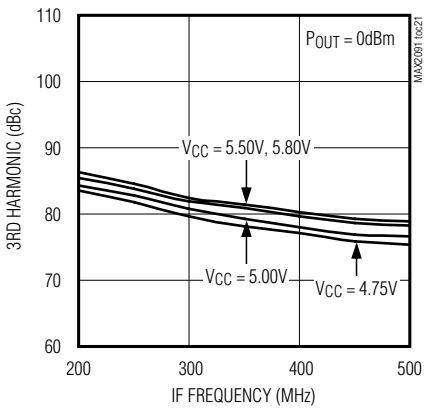
2ND HARMONIC vs. V_{PLVSET} SETTING



3RD HARMONIC vs. IF FREQUENCY



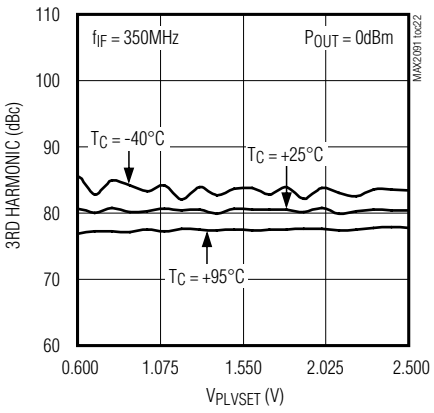
3RD HARMONIC vs. IF FREQUENCY



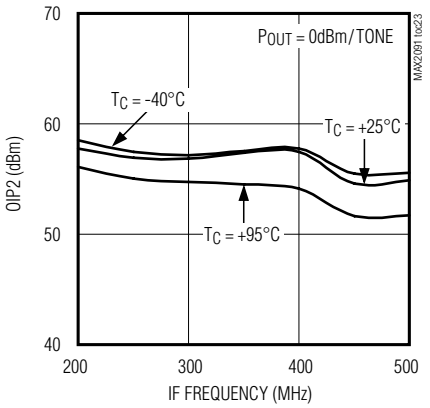
典型工作特性(续)

(*Typical Application Circuit* **configured for AGC amp only (IF_IN to IF_OUT)**, analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

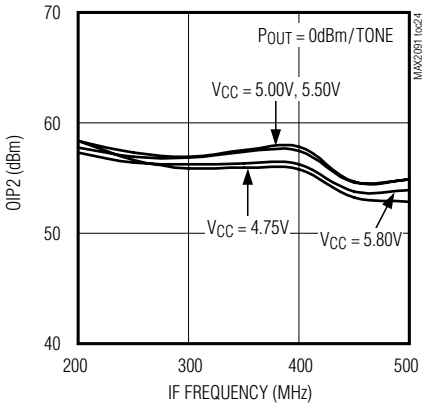
3RD HARMONIC vs. V_{PLVSET} SETTING



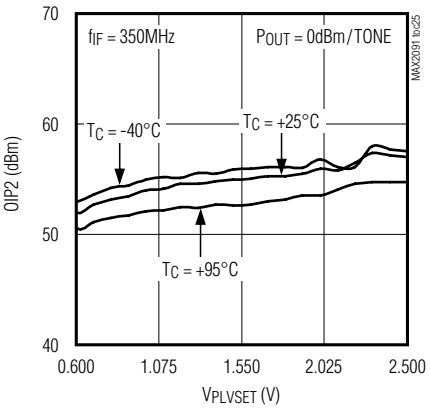
OIP2 vs. IF FREQUENCY



OIP2 vs. IF FREQUENCY



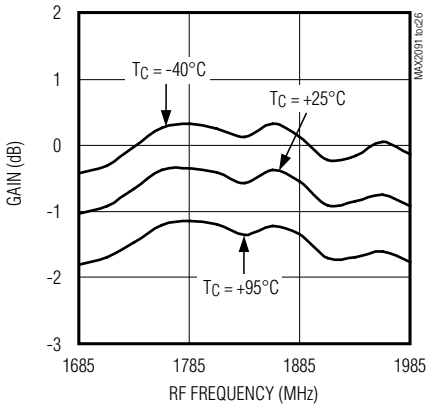
OIP2 vs. V_{PLVSET} SETTING



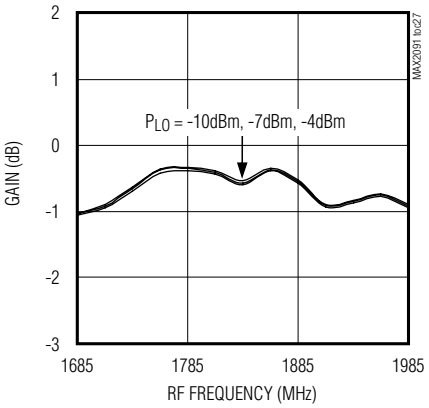
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

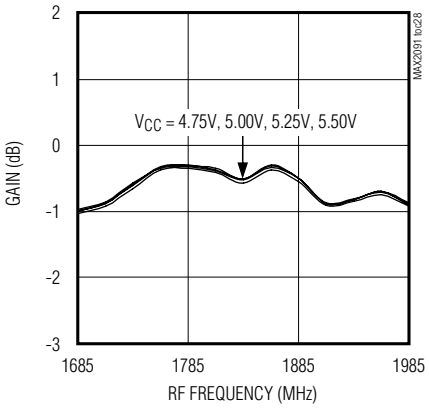
GAIN vs. RF FREQUENCY



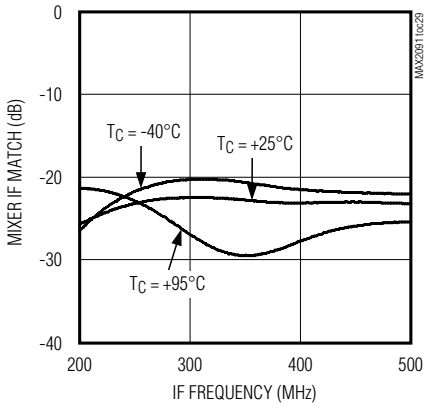
GAIN vs. RF FREQUENCY



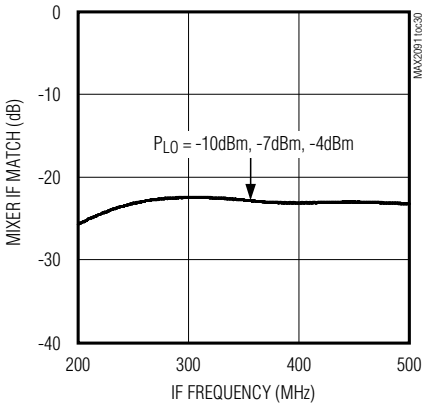
GAIN vs. RF FREQUENCY



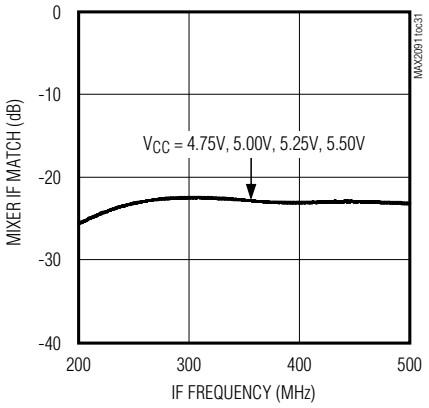
MIXER IF MATCH vs. IF FREQUENCY



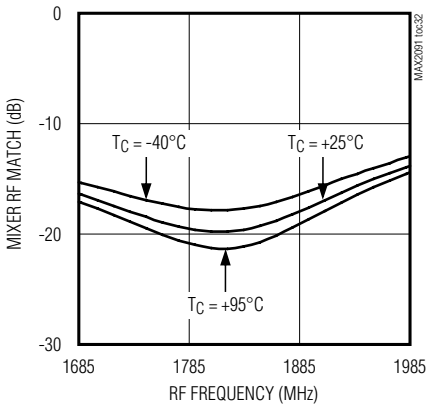
MIXER IF MATCH vs. IF FREQUENCY



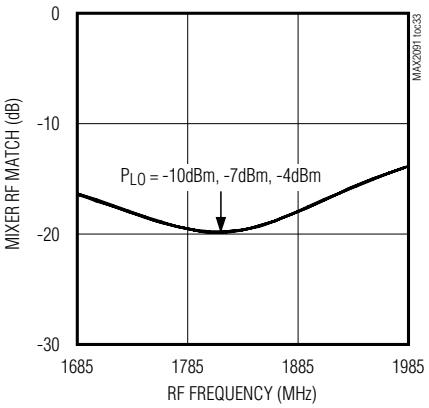
MIXER IF MATCH vs. IF FREQUENCY



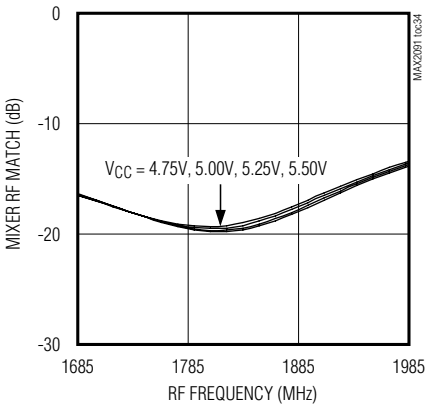
MIXER RF MATCH vs. RF FREQUENCY



MIXER RF MATCH vs. RF FREQUENCY



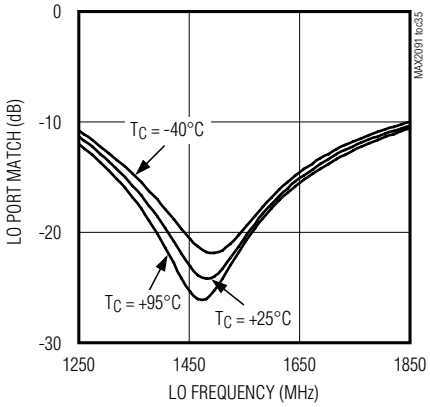
MIXER RF MATCH vs. RF FREQUENCY



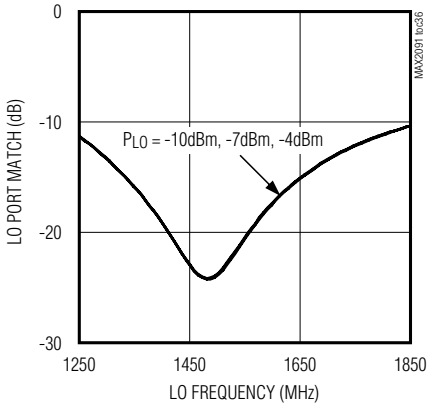
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

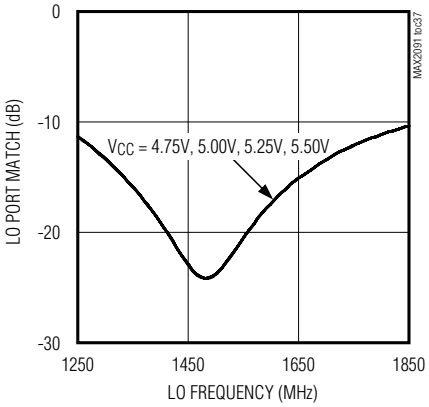
LO PORT MATCH vs. LO FREQUENCY



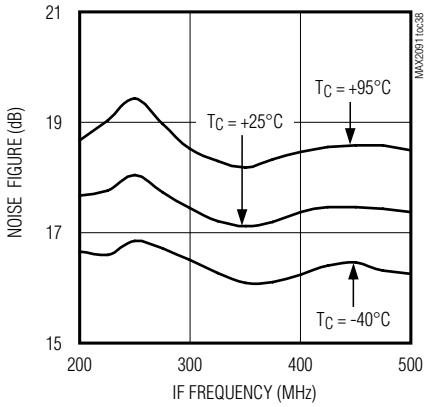
LO PORT MATCH vs. LO FREQUENCY



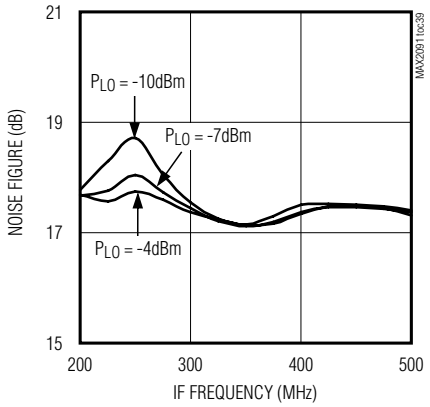
LO PORT MATCH vs. LO FREQUENCY



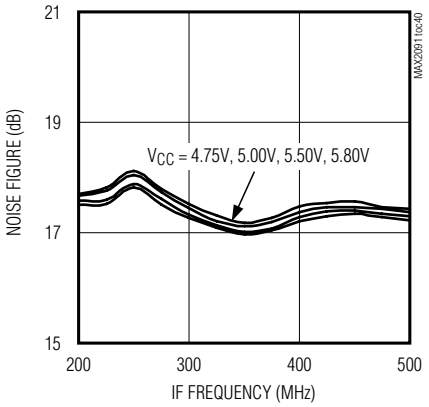
NOISE FIGURE vs. IF FREQUENCY



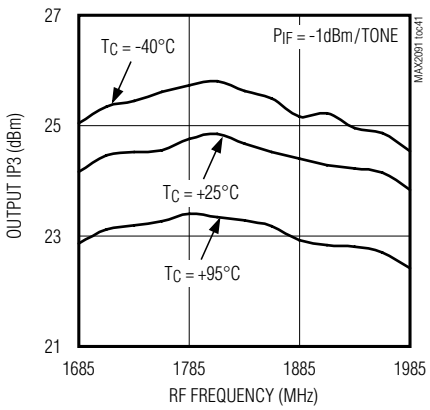
NOISE FIGURE vs. IF FREQUENCY



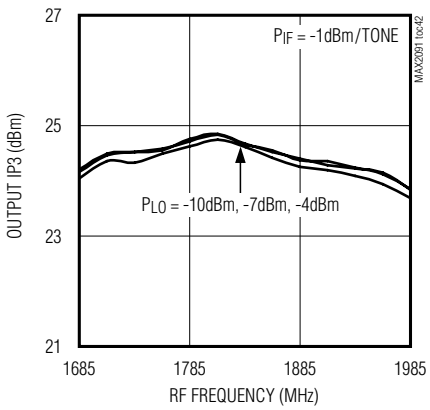
NOISE FIGURE vs. IF FREQUENCY



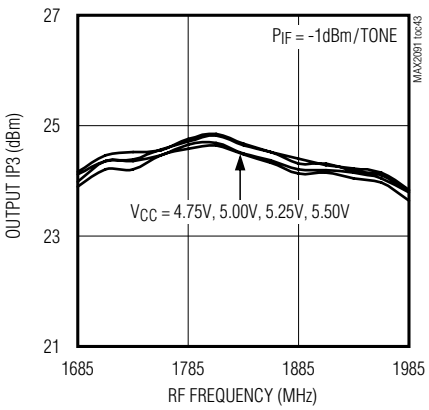
OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



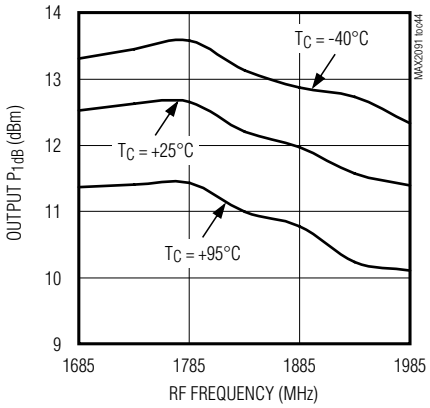
OUTPUT IP3 vs. RF FREQUENCY



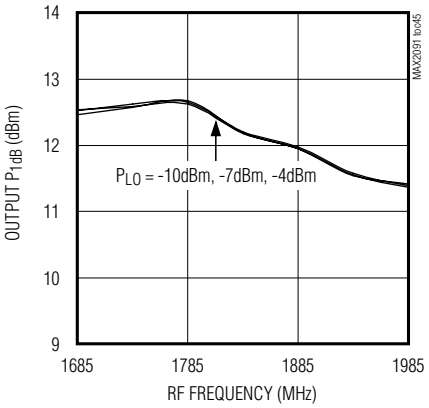
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY

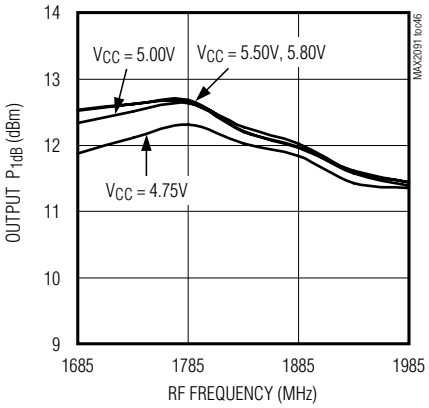


IMAGE REJECTION vs. RF FREQUENCY

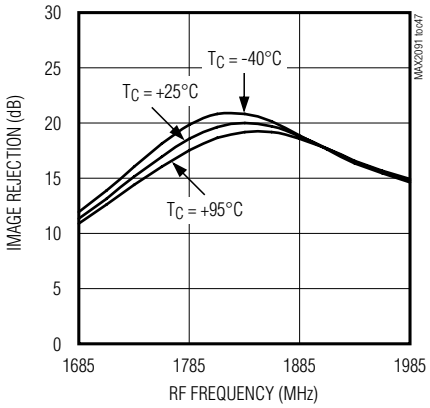


IMAGE REJECTION vs. RF FREQUENCY

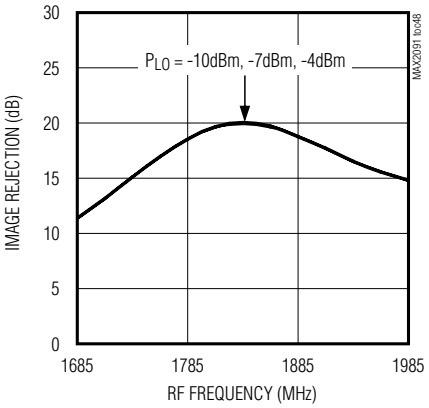
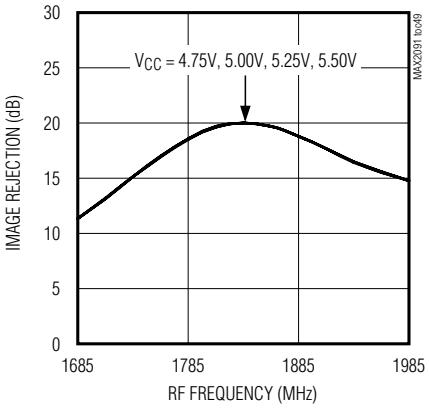
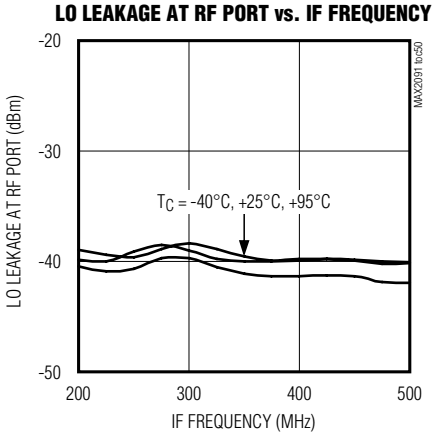


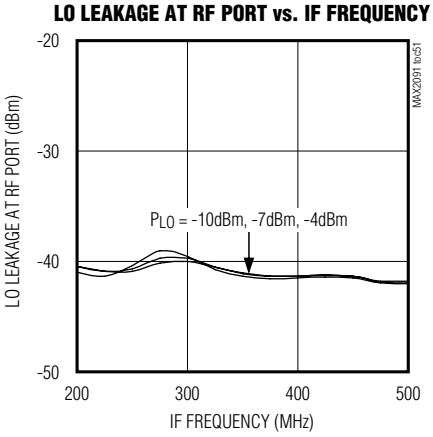
IMAGE REJECTION vs. RF FREQUENCY



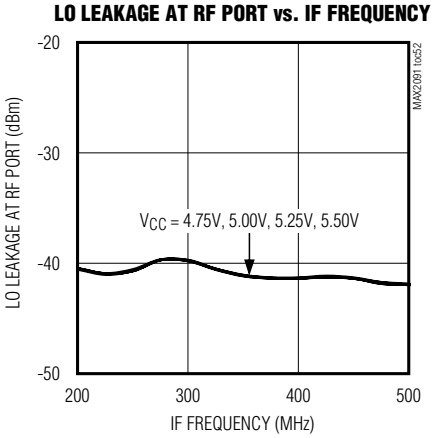
LO LEAKAGE AT RF PORT vs. IF FREQUENCY



LO LEAKAGE AT RF PORT vs. IF FREQUENCY



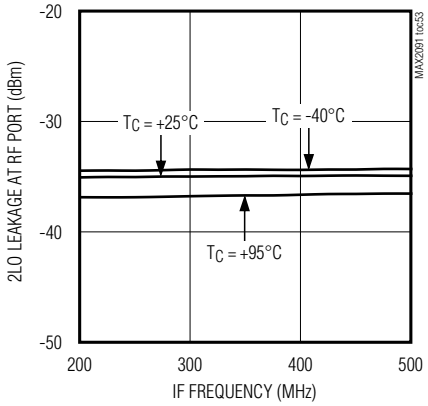
LO LEAKAGE AT RF PORT vs. IF FREQUENCY



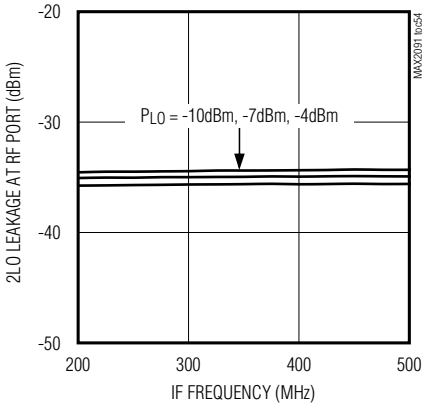
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

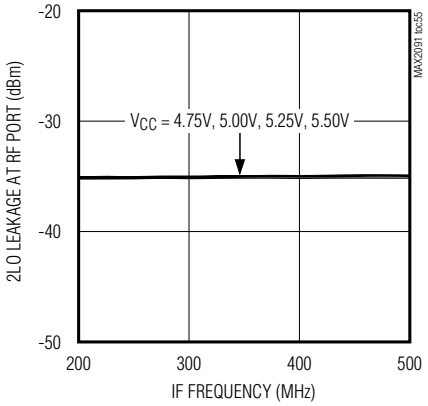
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



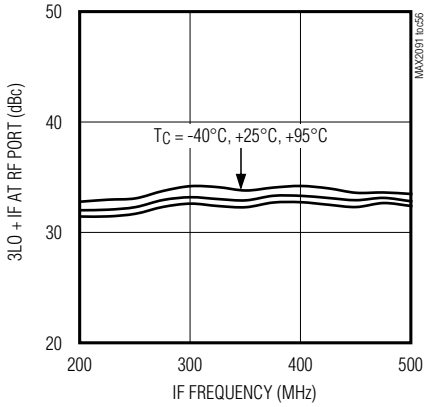
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



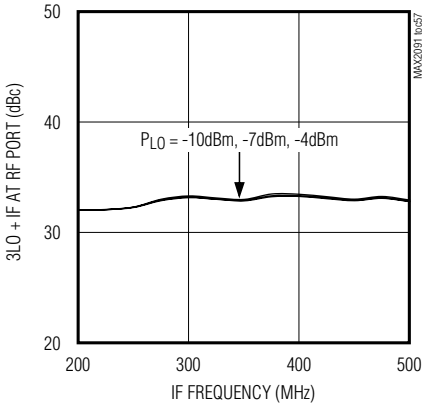
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



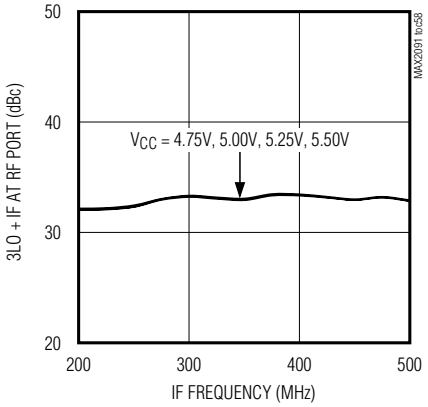
3LO + IF AT RF PORT vs. IF FREQUENCY



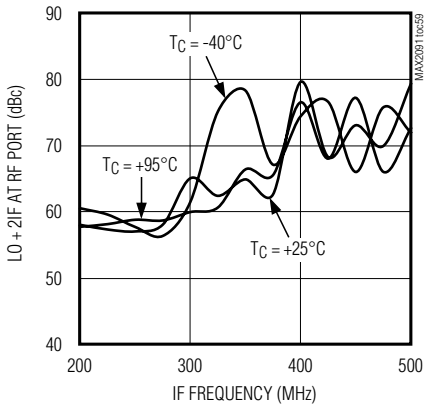
3LO + IF AT RF PORT vs. IF FREQUENCY



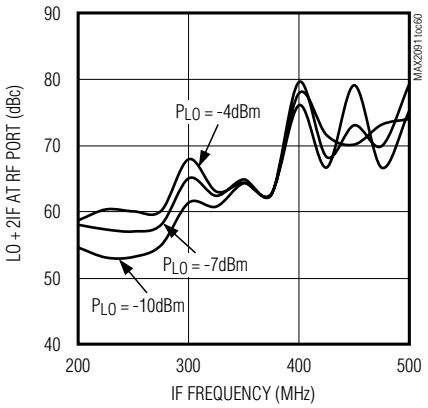
3LO + IF AT RF PORT vs. IF FREQUENCY



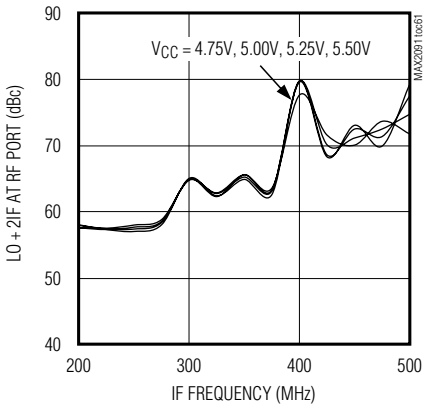
LO + 2IF AT RF PORT vs. IF FREQUENCY



LO + 2IF AT RF PORT vs. IF FREQUENCY



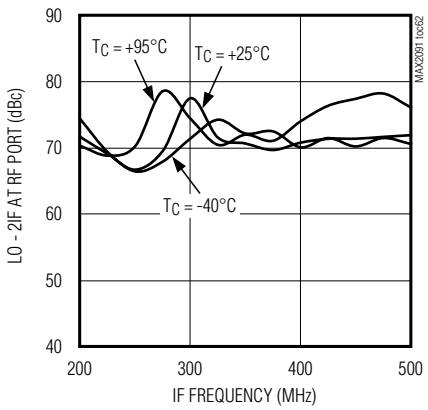
LO + 2IF AT RF PORT vs. IF FREQUENCY



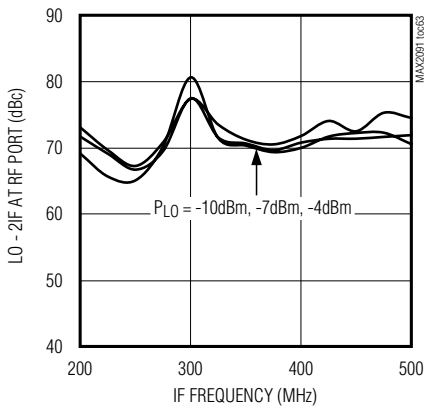
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

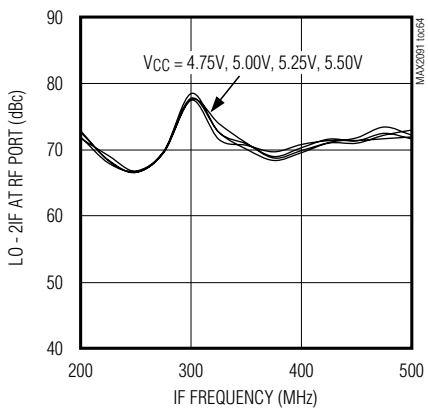
LO - 2IF AT RF PORT vs. IF FREQUENCY



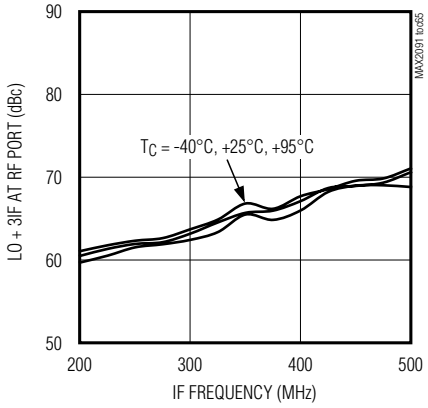
LO - 2IF AT RF PORT vs. IF FREQUENCY



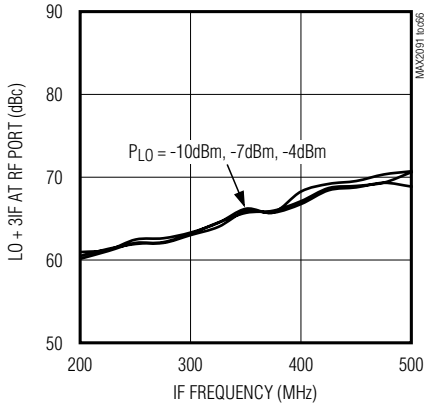
LO - 2IF AT RF PORT vs. IF FREQUENCY



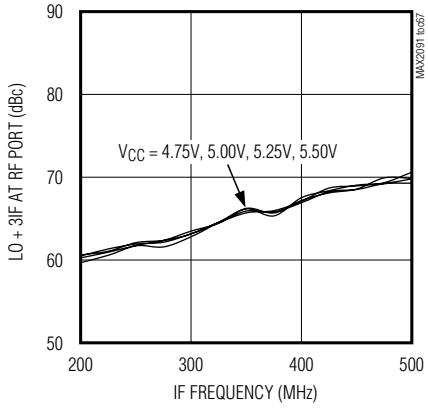
LO + 3IF AT RF PORT vs. IF FREQUENCY



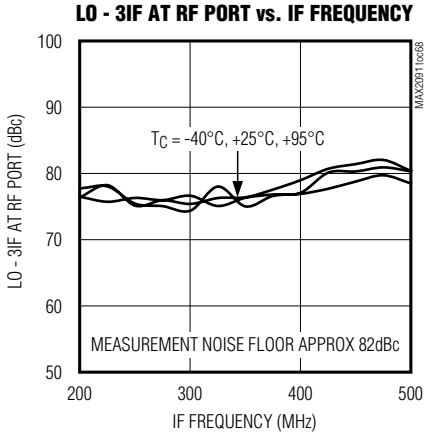
LO + 3IF AT RF PORT vs. IF FREQUENCY



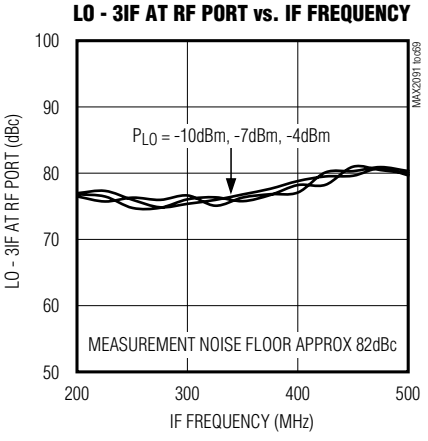
LO + 3IF AT RF PORT vs. IF FREQUENCY



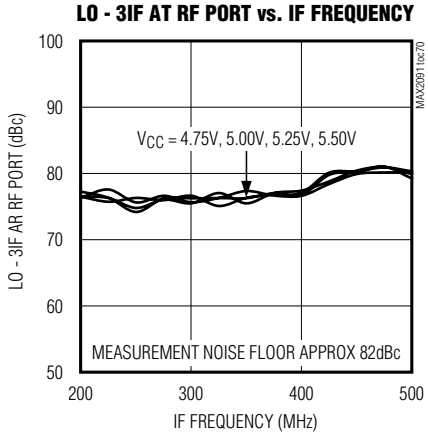
LO - 3IF AT RF PORT vs. IF FREQUENCY



LO - 3IF AT RF PORT vs. IF FREQUENCY



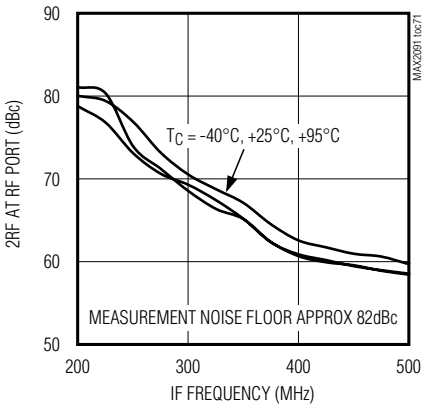
LO - 3IF AT RF PORT vs. IF FREQUENCY



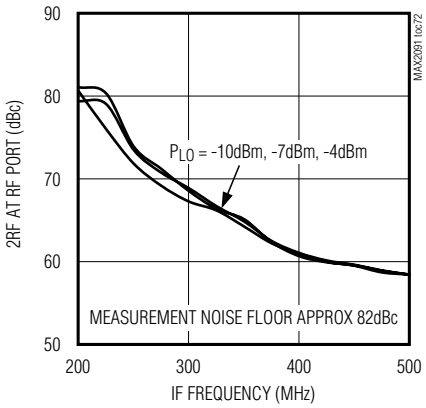
典型工作特性(续)

(*Typical Application Circuit* **configured for Mixer only (MIX_IN to RF_OUT),** V_{CC} = 5.5V, T_C = +25°C, f_{MIX_IN} = 350MHz, P_{MIX_IN} = -1dBm, f_{LO} = 1485MHz, P_{LO} = -7dBm, $f_{RF} = f_{IF\_IN} + f_{LO}$, $R_{SOURCE} = R_{LOAD}$ = 50Ω, CTRL1 = 1, CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

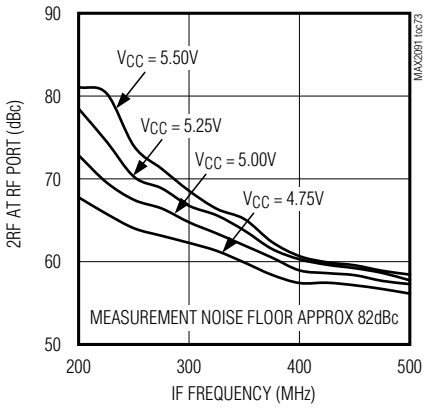
2RF AT RF PORT vs. IF FREQUENCY



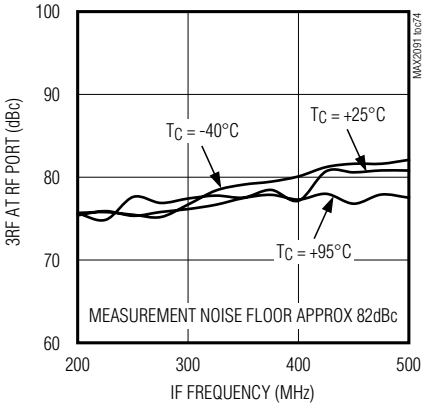
2RF AT RF PORT vs. IF FREQUENCY



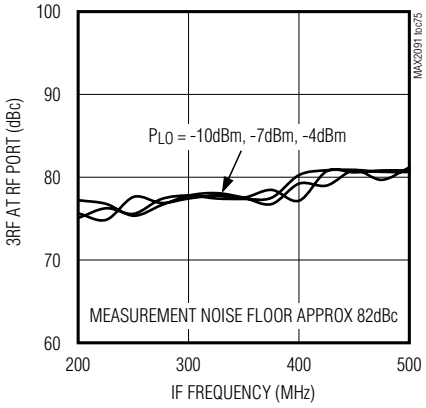
2RF AT RF PORT vs. IF FREQUENCY



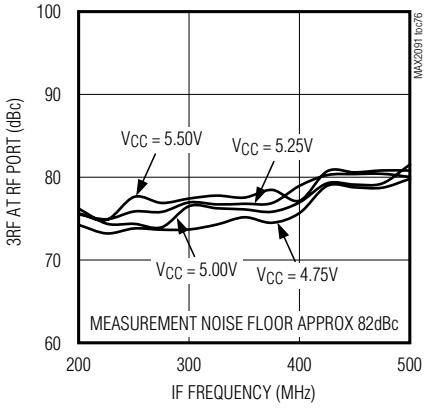
3RF AT RF PORT vs. IF FREQUENCY



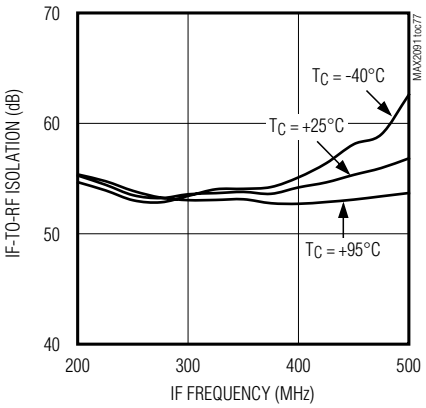
3RF AT RF PORT vs. IF FREQUENCY



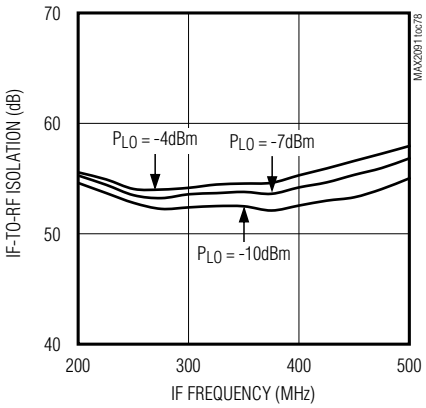
3RF AT RF PORT vs. IF FREQUENCY



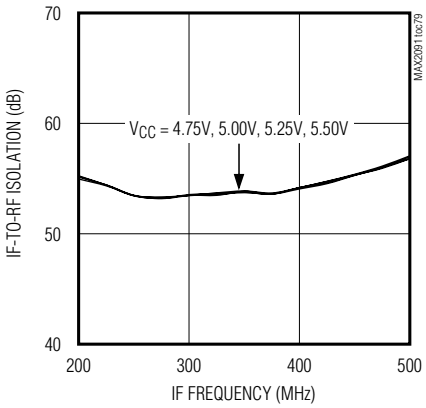
IF-TO-RF ISOLATION vs. IF FREQUENCY



IF-TO-RF ISOLATION vs. IF FREQUENCY



IF-TO-RF ISOLATION vs. IF FREQUENCY



典型工作特性(续)

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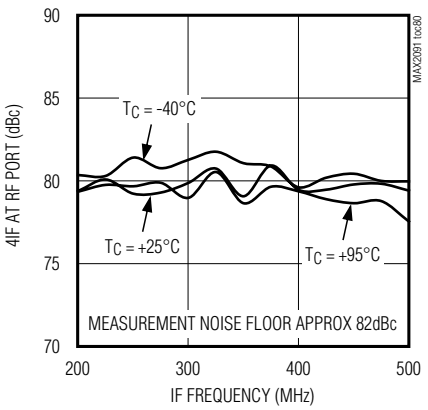
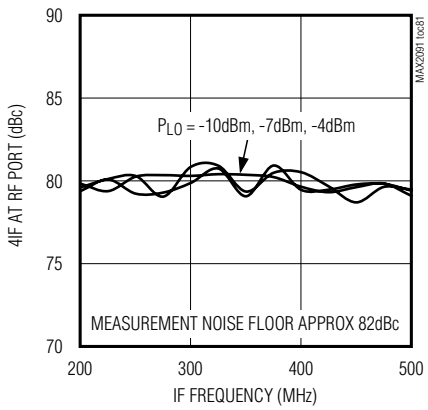
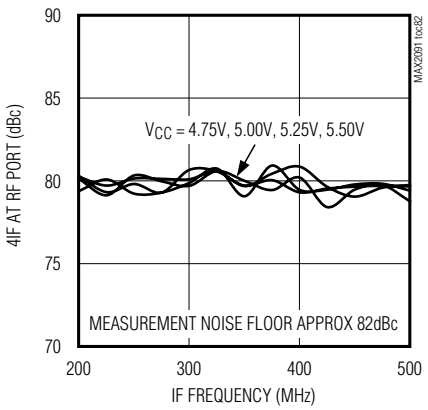
4IF AT RF PORT vs. IF FREQUENCY



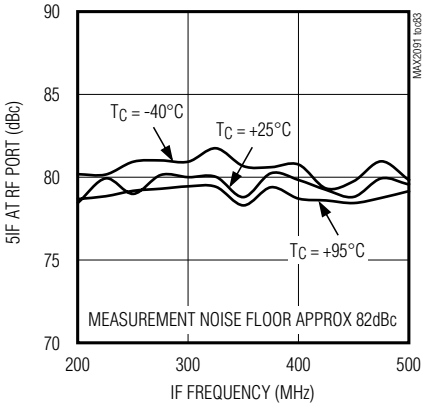
4IF AT RF PORT vs. IF FREQUENCY



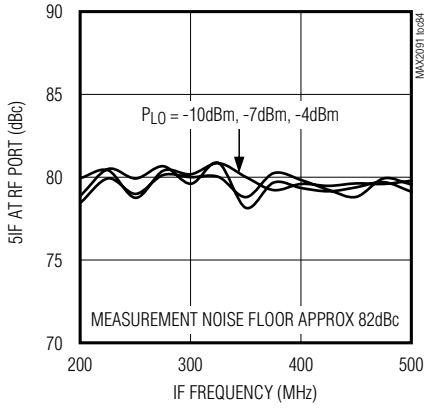
4IF AT RF PORT vs. IF FREQUENCY



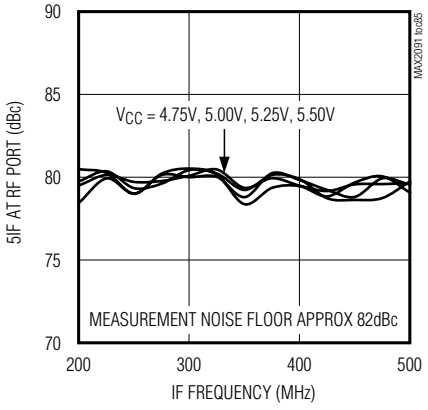
5IF AT RF PORT vs. IF FREQUENCY



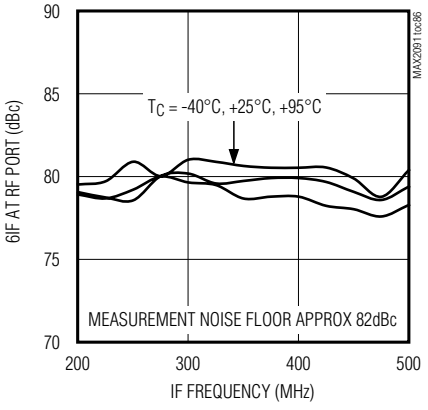
5IF AT RF PORT vs. IF FREQUENCY



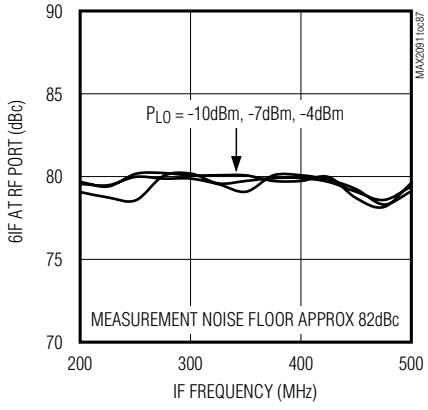
5IF AT RF PORT vs. IF FREQUENCY



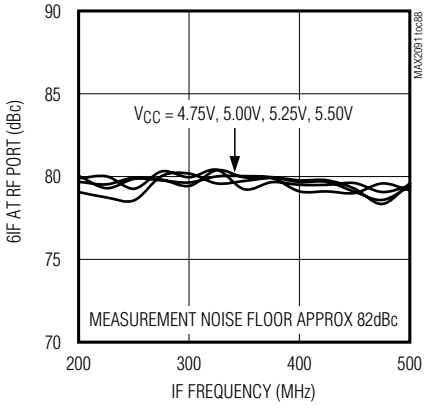
6IF AT RF PORT vs. IF FREQUENCY



6IF AT RF PORT vs. IF FREQUENCY



6IF AT RF PORT vs. IF FREQUENCY



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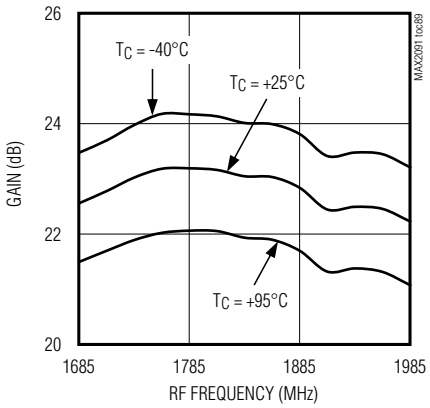
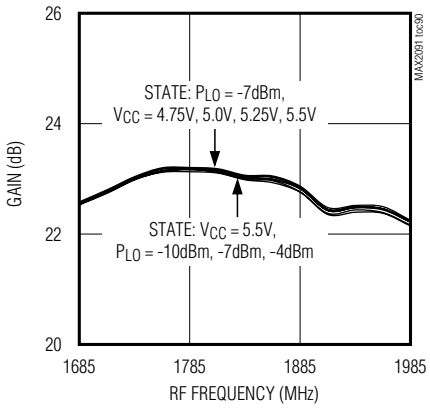
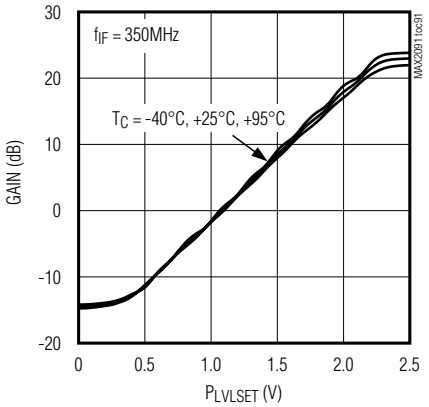
GAIN vs. RF FREQUENCY



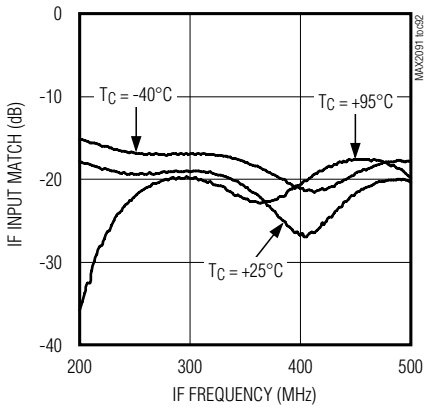
GAIN vs. RF FREQUENCY



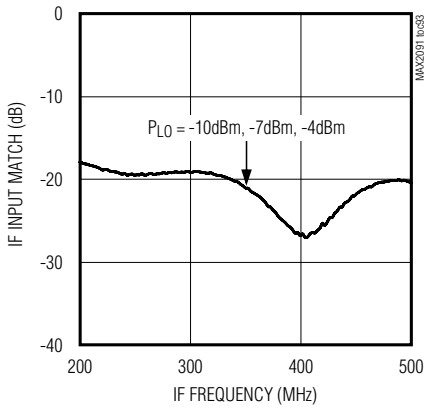
GAIN vs. P_{LVLSET} SETTING



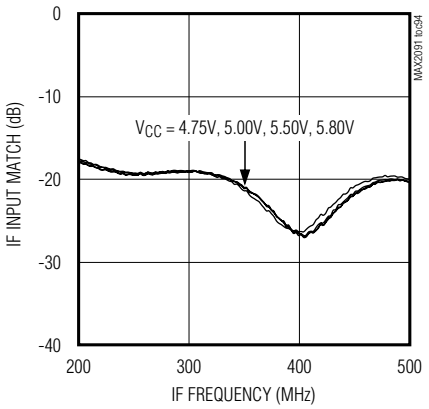
IF INPUT MATCH vs. IF FREQUENCY



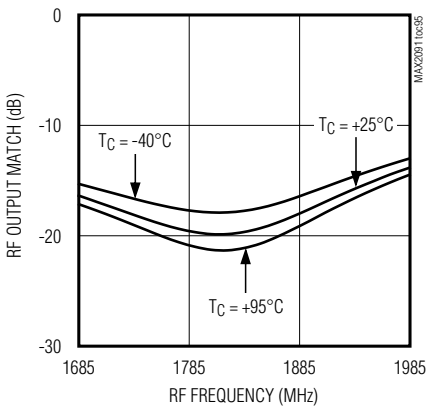
IF INPUT MATCH vs. IF FREQUENCY



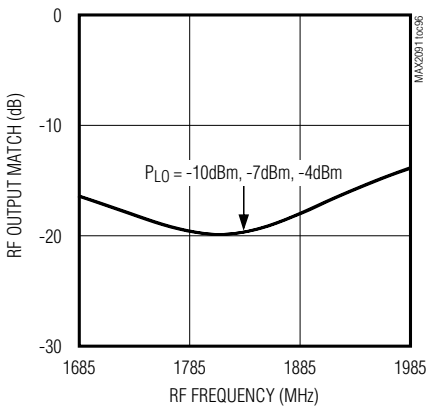
IF INPUT MATCH vs. IF FREQUENCY



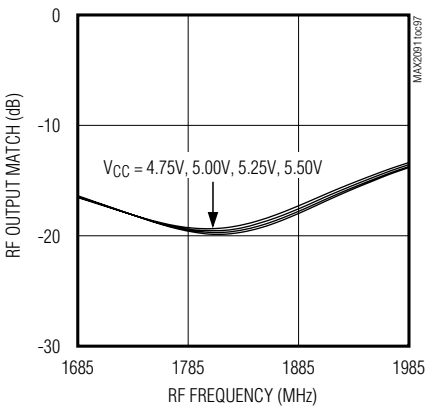
RF OUTPUT MATCH vs. RF FREQUENCY



RF OUTPUT MATCH vs. RF FREQUENCY



RF OUTPUT MATCH vs. RF FREQUENCY



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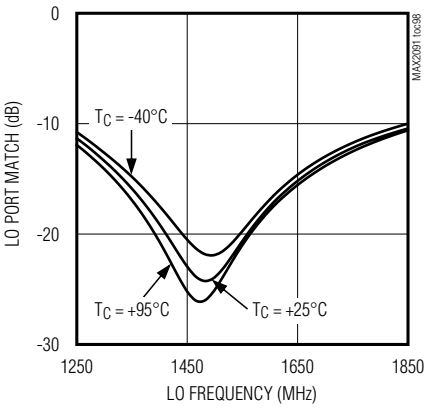
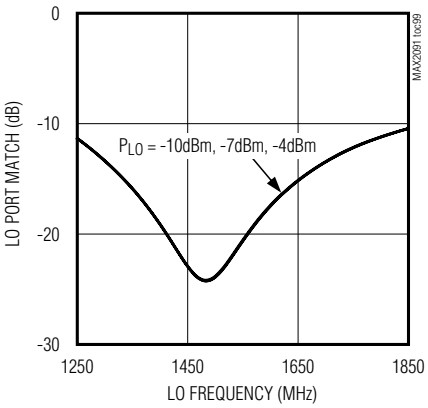
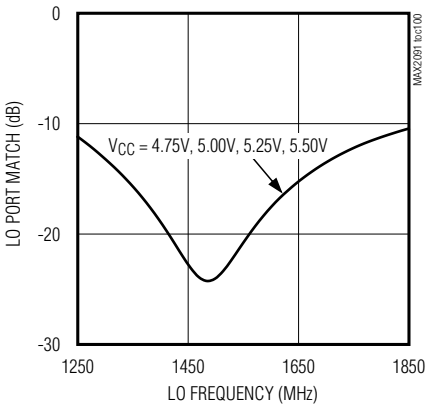
LO PORT MATCH vs. LO FREQUENCY



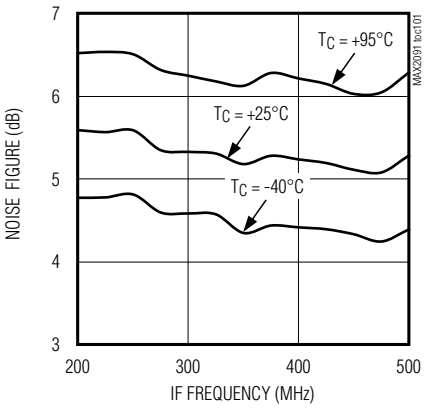
LO PORT MATCH vs. LO FREQUENCY



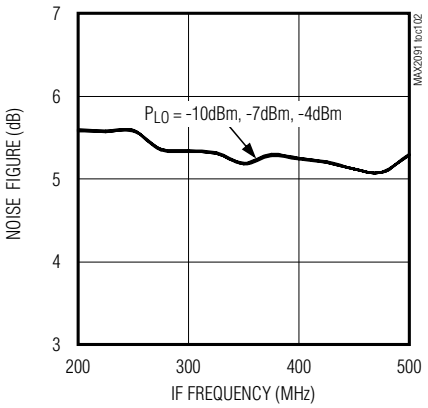
LO PORT MATCH vs. LO FREQUENCY



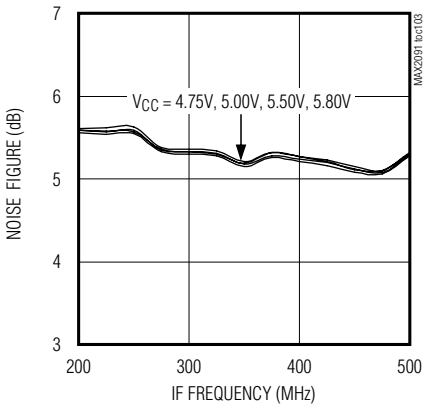
NOISE FIGURE vs. IF FREQUENCY



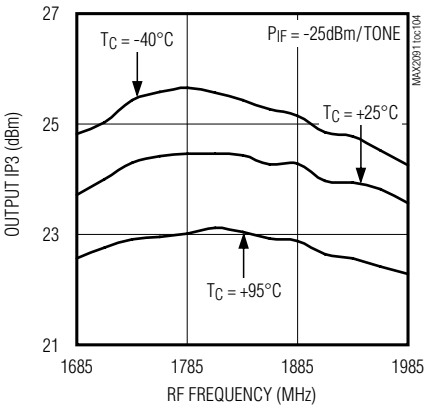
NOISE FIGURE vs. IF FREQUENCY



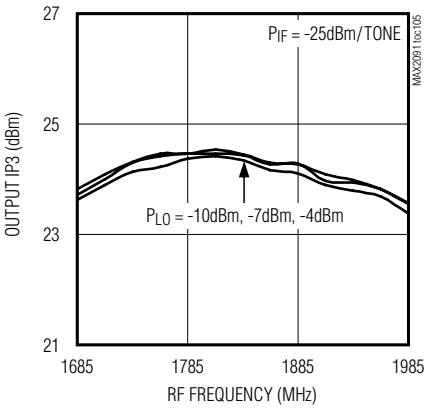
NOISE FIGURE vs. IF FREQUENCY



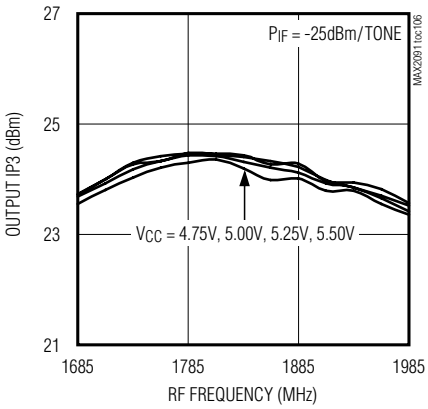
OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



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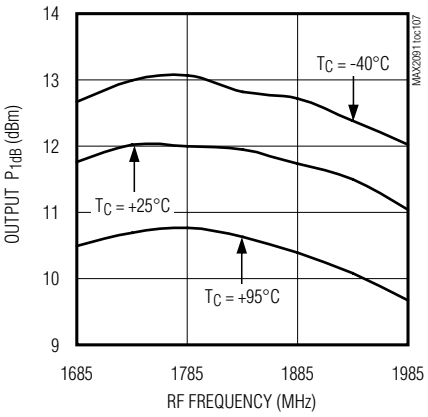
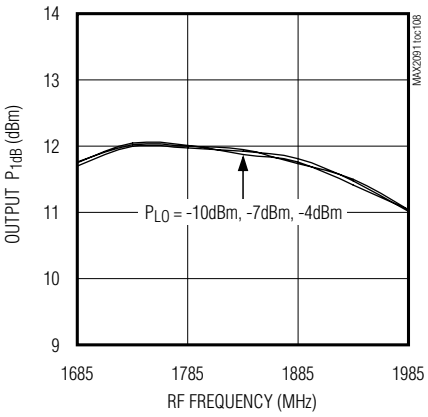
OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY

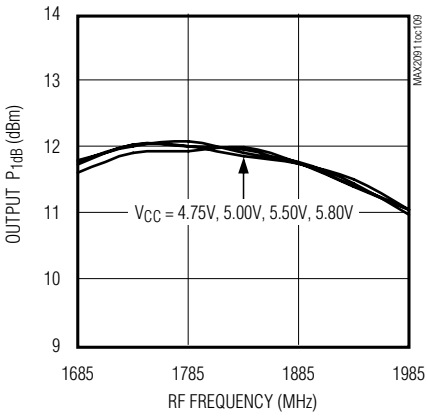


IMAGE REJECTION vs. RF FREQUENCY

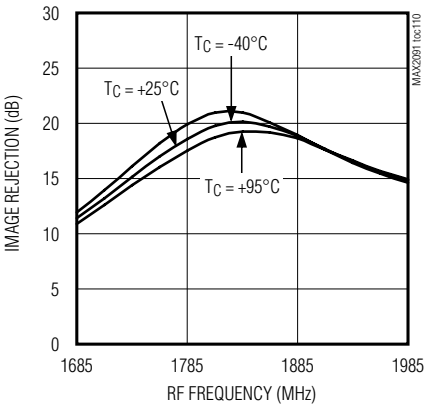


IMAGE REJECTION vs. RF FREQUENCY

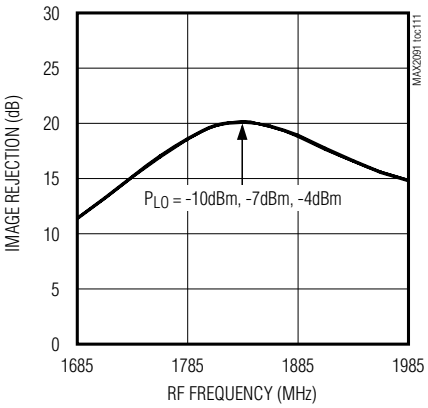
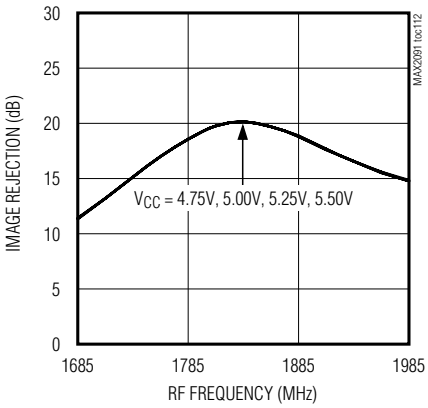
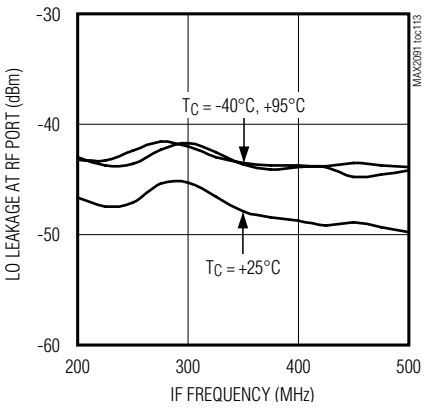


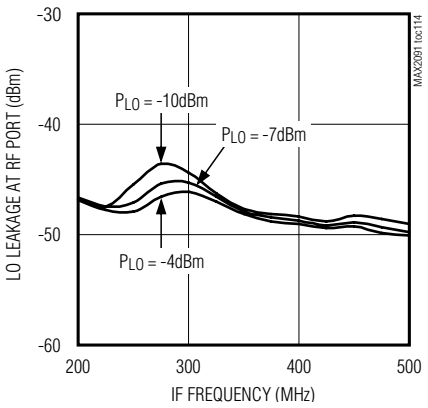
IMAGE REJECTION vs. RF FREQUENCY



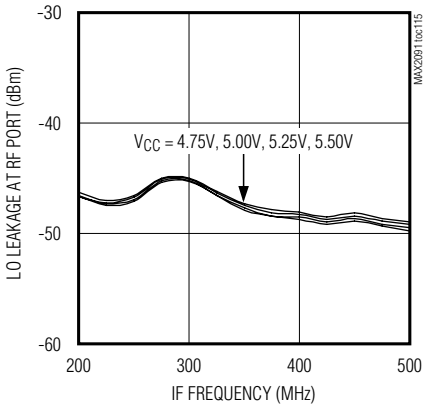
LO LEAKAGE AT RF PORT vs. IF FREQUENCY



LO LEAKAGE AT RF PORT vs. IF FREQUENCY



LO LEAKAGE AT RF PORT vs. IF FREQUENCY



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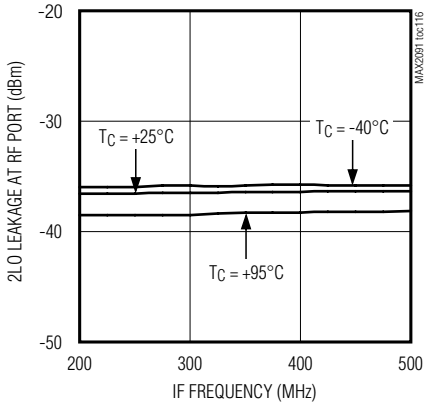
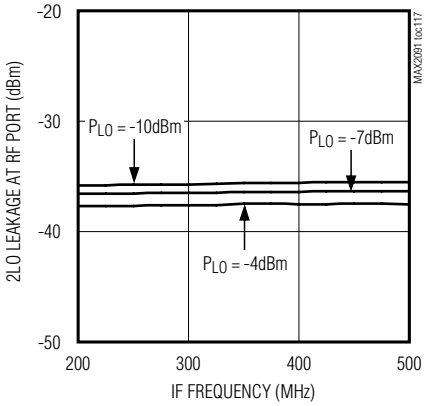
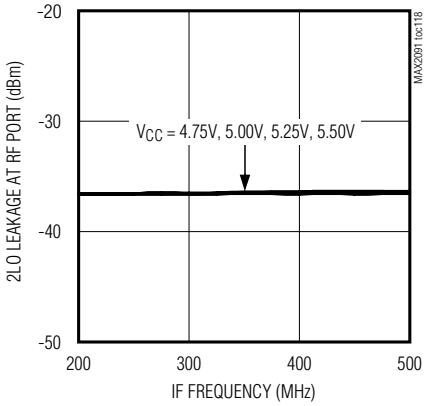
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



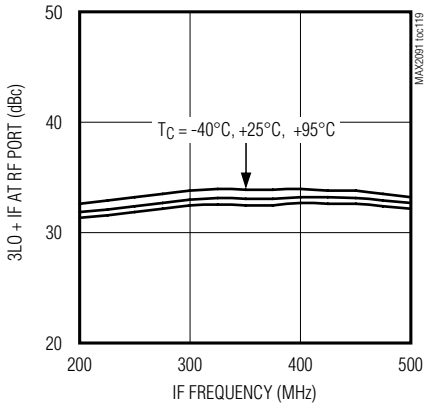
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



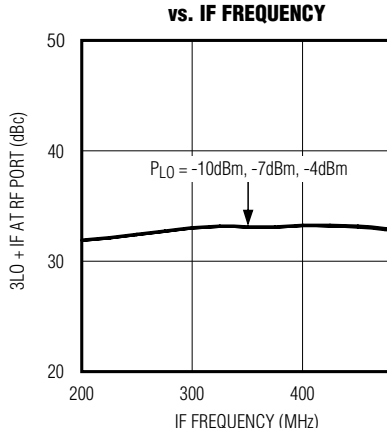
2LO LEAKAGE AT RF PORT vs. IF FREQUENCY



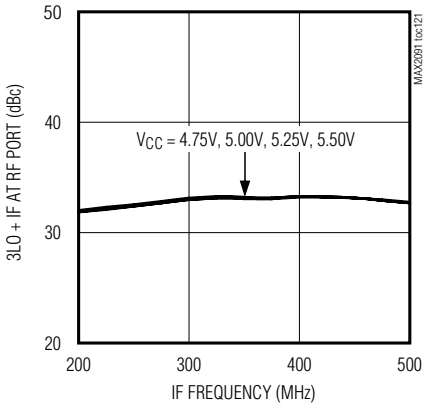
3LO + IF AT RF PORT vs. IF FREQUENCY



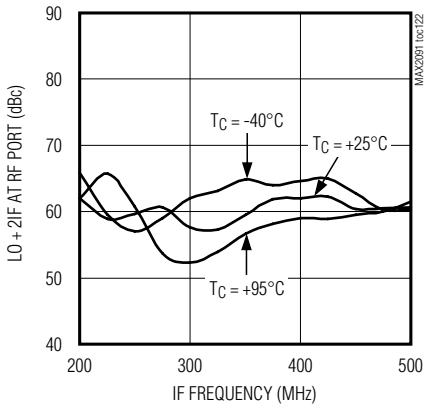
3LO + IF AT RF PORT vs. IF FREQUENCY



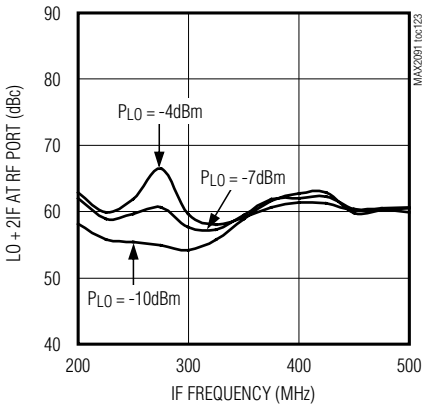
3LO + IF AT RF PORT vs. IF FREQUENCY



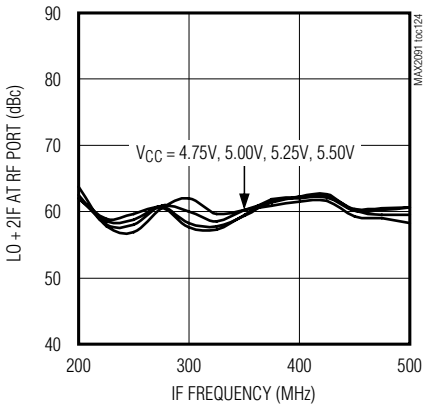
LO + 2IF AT RF PORT vs. IF FREQUENCY



LO + 2IF AT RF PORT vs. IF FREQUENCY

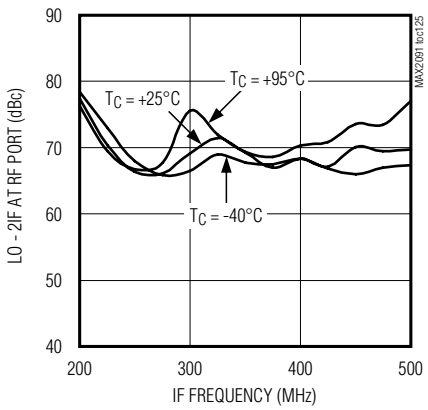


LO + 2IF AT RF PORT vs. IF FREQUENCY

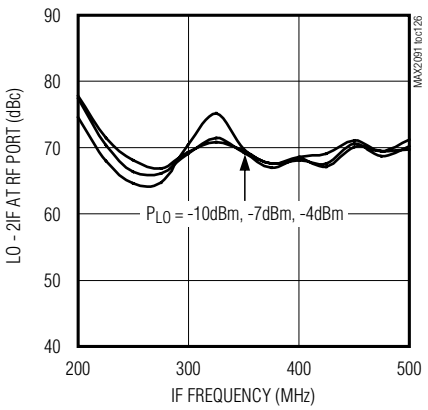


(*Typical Application Circuit* **configured for Full Cascade with interstage attenuator network (IF_IN to RF_OUT),** analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, f_{LO}= 1485MHz, P_{LO} = -7dBm, f_{RF} = f_{IF_IN} + f_{LO}, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1 CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

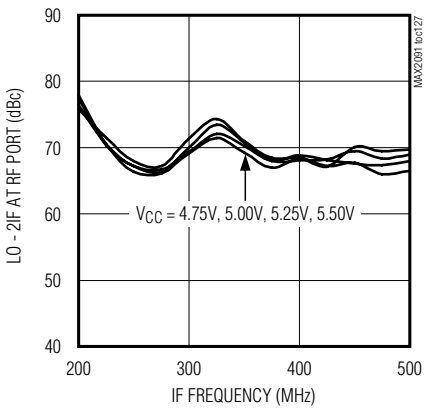
LO - 2IF AT RF PORT vs. IF FREQUENCY



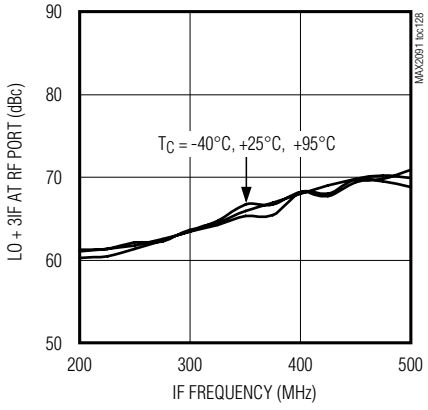
LO - 2IF AT RF PORT vs. IF FREQUENCY



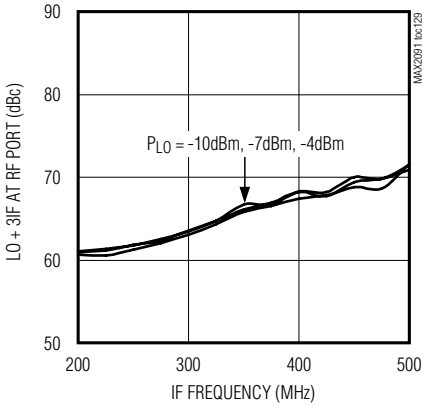
LO - 2IF AT RF PORT vs. IF FREQUENCY



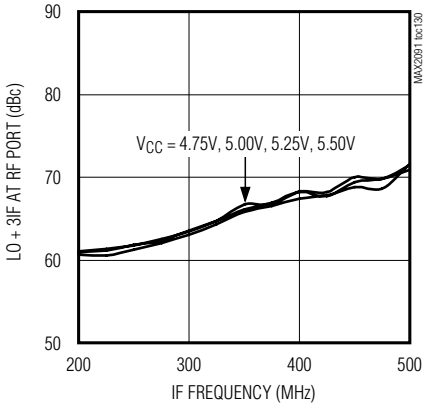
LO + 3IF AT RF PORT vs. IF FREQUENCY



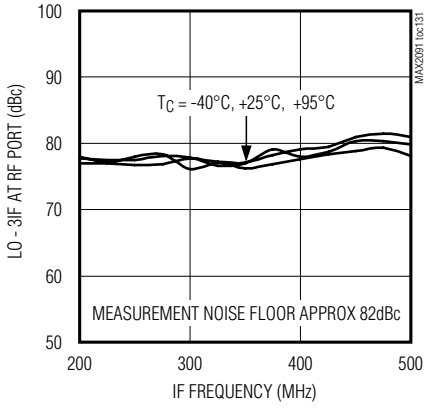
LO + 3IF AT RF PORT vs. IF FREQUENCY



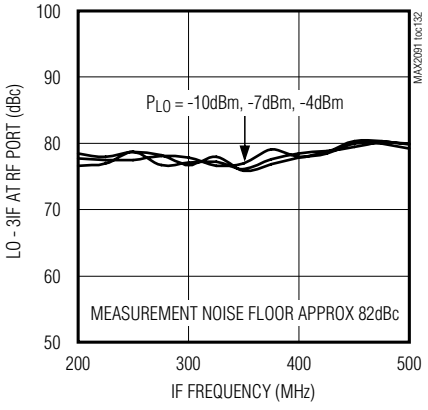
LO + 3IF AT RF PORT vs. IF FREQUENCY



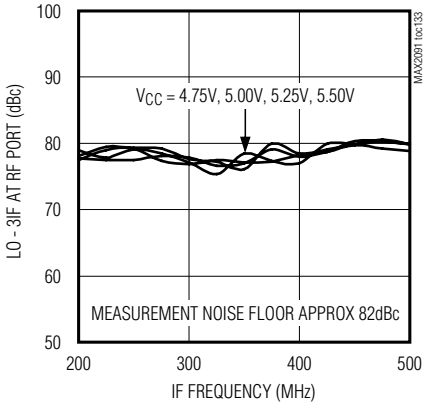
LO - 3IF AT RF PORT vs. IF FREQUENCY



LO - 3IF AT RF PORT vs. IF FREQUENCY

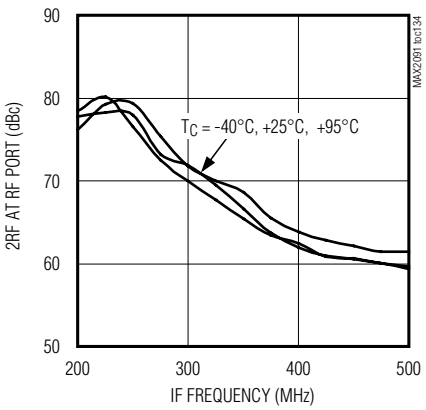


LO - 3IF AT RF PORT vs. IF FREQUENCY

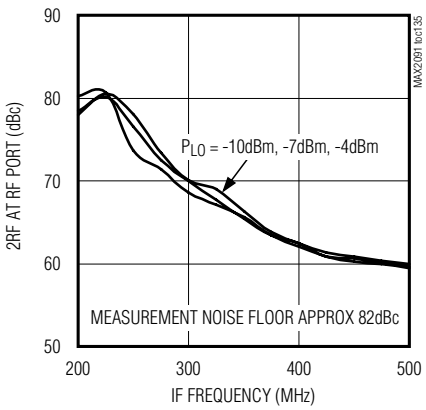


(*Typical Application Circuit* **configured for Full Cascade with interstage attenuator network (IF_IN to RF_OUT),** analog attenuator set to maximum gain ($V_{PLVLSET}$ = 2.5V), V_{CC} = 5.5V, T_C = +25°C, f_{IF_IN} = 350MHz, P_{IF_IN} = -25dBm, f_{LO}= 1485MHz, P_{LO} = -7dBm, f_{RF} = f_{IF_IN} + f_{LO}, R_{SOURCE} = R_{LOAD} = 50Ω, CTRL1 = 1 CTRL2 = 0, ALM_THRES = ALM = open, unless otherwise noted.)

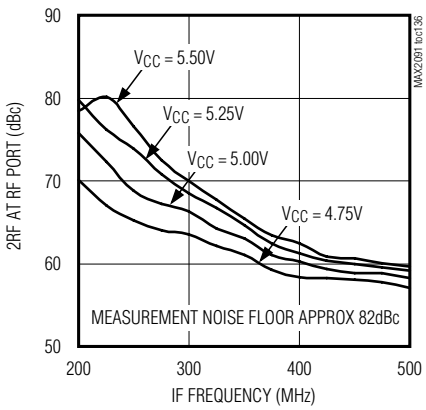
2RF AT RF PORT vs. IF FREQUENCY



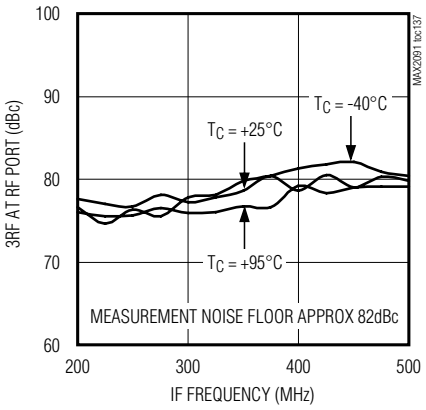
2RF AT RF PORT vs. IF FREQUENCY



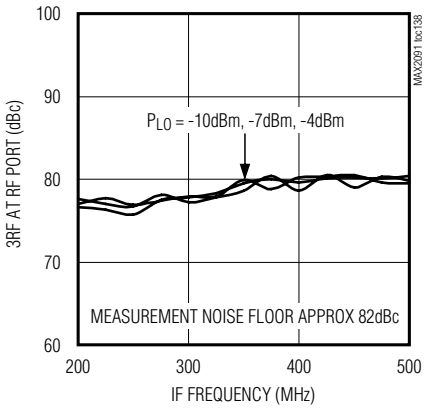
2RF AT RF PORT vs. IF FREQUENCY



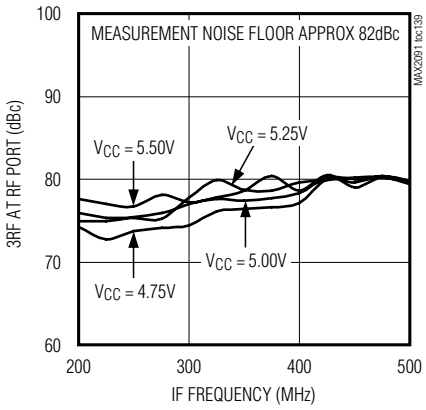
3RF AT RF PORT vs. IF FREQUENCY



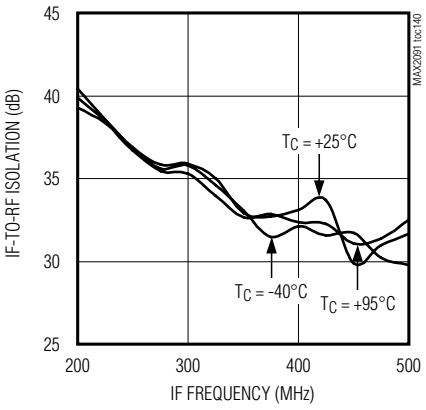
3RF AT RF PORT vs. IF FREQUENCY



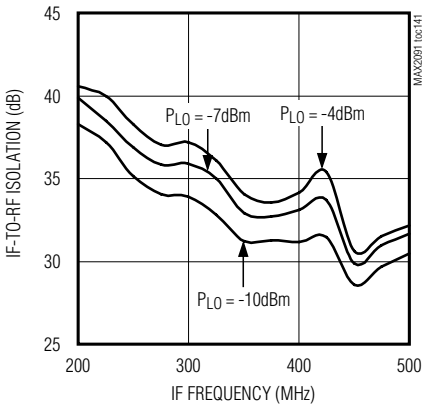
3RF AT RF PORT vs. IF FREQUENCY



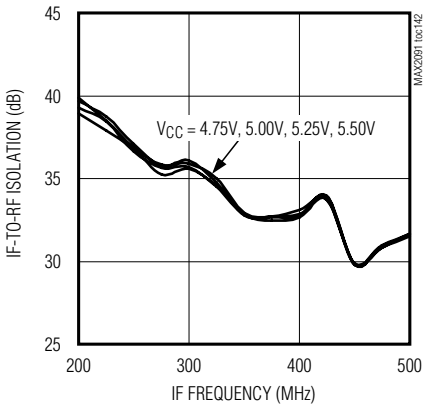
IF-TO-RF ISOLATION vs. IF FREQUENCY



IF-TO-RF ISOLATION vs. IF FREQUENCY



IF-TO-RF ISOLATION vs. IF FREQUENCY



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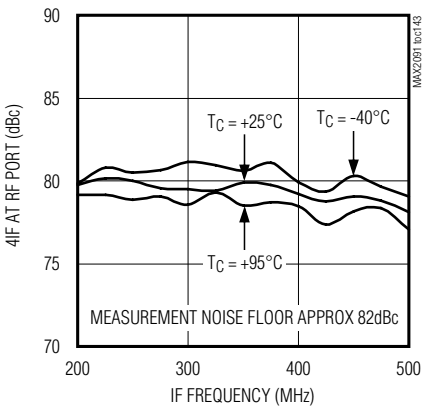
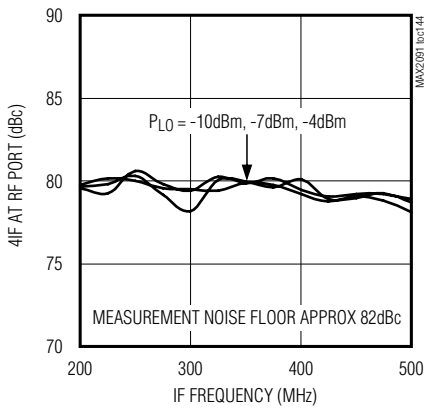
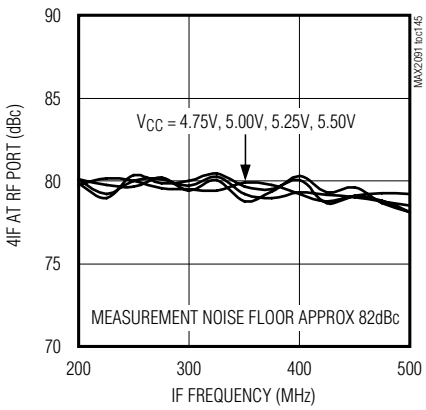
4IF AT RF PORT vs. IF FREQUENCY



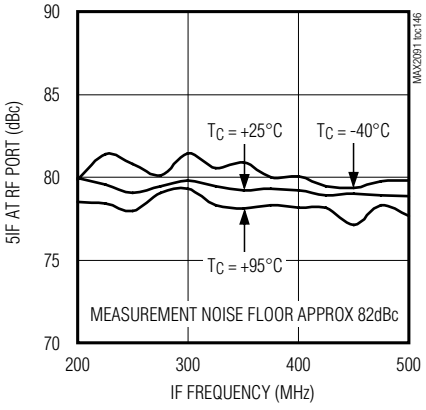
4IF AT RF PORT vs. IF FREQUENCY



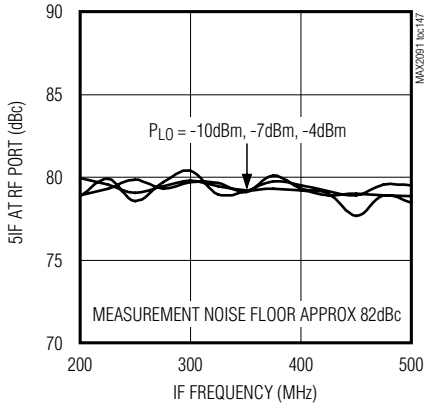
4IF AT RF PORT vs. IF FREQUENCY



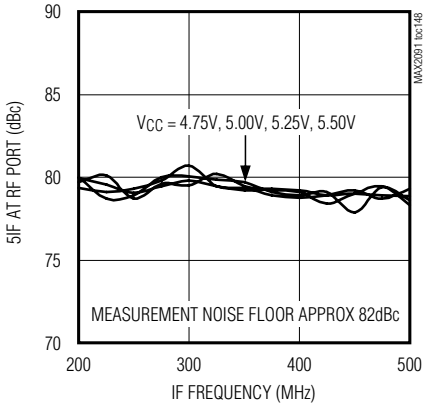
5IF AT RF PORT vs. IF FREQUENCY



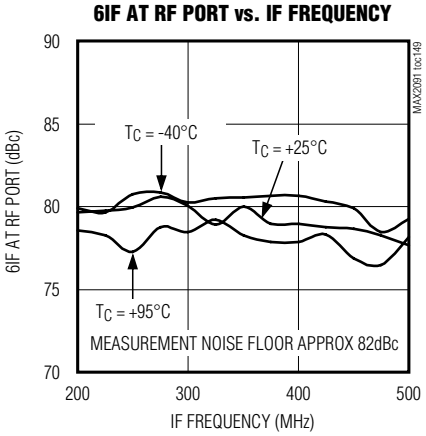
5IF AT RF PORT vs. IF FREQUENCY



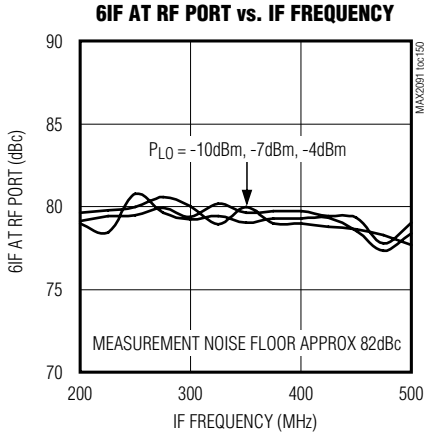
5IF AT RF PORT vs. IF FREQUENCY



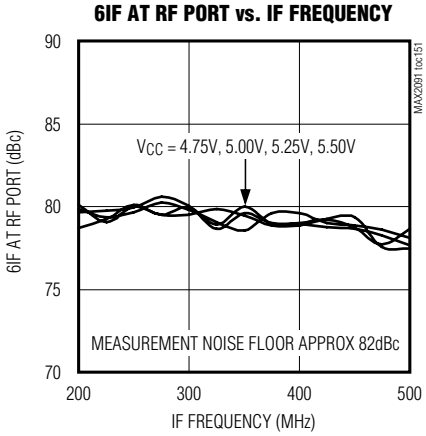
6IF AT RF PORT vs. IF FREQUENCY



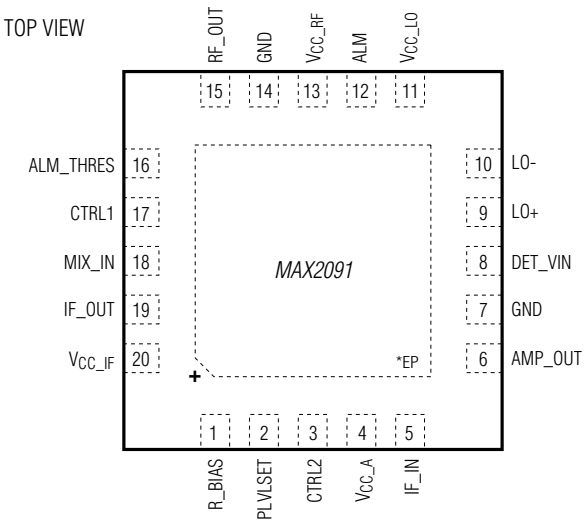
6IF AT RF PORT vs. IF FREQUENCY



6IF AT RF PORT vs. IF FREQUENCY



引脚配置



TQFN
5mm x 5mm

引脚说明

引脚	名称	功能
1	R_BIAS	偏置电阻设置输入，在该引脚和地之间连接一个电阻。
2	PLVLSET	AGC环路门限电平输入/衰减器控制。
3	CTRL2	功能控制位(见表1)。
4	V_{CC_A}	电源输入，利用10nF电容旁路至地，电容尽量靠近引脚放置。
5	IF_IN	衰减器输入(50Ω)，需要隔直电容。
6	AMP_OUT	误差放大器输出。
7, 14	GND	地。
8	DET_VIN	来自外部检测器的误差放大器输入电压。
9	LO+	LO输入正端，需要隔直电容。
10	LO-	LO输入负端，连接至地。
11	V_{CC_LO}	LO驱动器电源输入，利用1µF和10nF电容旁路至地，电容尽量靠近引脚放置。
12	ALM	报警逻辑输出。
13	V_{CC_RF}	混频器电源输入，利用10nF电容旁路至地，尽量靠近引脚。
15	RF_OUT	混频器输出，需要隔直电容。
16	ALM_THRES	报警门限电压输入，详细工作信息请参见*报警工作*部分。

引脚说明(续)

引脚	名称	功能
17	CTRL1	功能控制位(见表1)。
18	MIX_IN	混频器输入，详细连接信息请参见*典型应用*电路。
19	IF_OUT	驱动器放大器输出(50Ω)，详细连接信息请参见*典型应用*电路。
20	V_{CC_IF}	驱动器-放大器电源输入，利用10nF电容旁路至地，电容尽量靠近引脚放置。
—	EP	裸焊盘，内部连接至GND。将该裸焊盘通过多个接地过孔焊接到PCB焊盘，使热量有效扩散至PCB接地区域。为了获得良好的RF性能，也需要这种多过孔接地方式(见*布局考虑*部分)。

表1. 模式控制逻辑

CTRL1	CTRL2	VGA	MIXER	ERROR AMPLIFIER	ALC LOOP	ALARM	FUNCTIONAL DESCRIPTION
0	0	Disabled	Disabled	Disabled	Disabled	Disabled	Power-Down Mode
1	0	Enabled	Enabled	Disabled	Disabled	Disabled	VGA/Mixer Only Mode
1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Closed ALC Mode: ALC loop locks DET_VIN to PLVLSET
0	1	—	—	—	—	—	**Factory Test Mode (Do Not Use)**

详细说明

MAX2091单芯片SiGeBiCMOS上变频混频器IC集成了模拟可变增益放大器、上变频混频器和镜频滤波器。器件对50MHz至500MHz IF信号进行放大，然后与LO信号混频，并对所产生的1735MHz至1935MHz上变频信号提供片上滤波，作为信号处理的最后一级。

模拟衰减器由外部模拟电压控制。器件具有23dB增益(无衰减)、5.4dB NF(无衰减，包括衰减器插入损耗)和+24.5dBm OIP3。所有这些特性都使MAX2091成为各种发射系统的理想上变频器选择。与MAX2092 RF VGA配对使用构成完备的2芯片IF-RF信号调理方案，用于微波点对点发送设备。

应用信息

工作模式

MAX2091可工作在多种不同模式，如表1所示。

仅VGA/混频器工作模式

仅工作在VGA/混频器模式时，设置CTRL1 = 逻辑1、CTRL2 = 逻辑0，向PLVLSET施加0至2.5V直流电压，以手动调节IF衰减器，进而调节RF_OUT功率。IF_IN由-25dBm至+5dBm固定输入功率驱动时，随着PLVLSET增大，RF_OUT的输出功率将以19.5dB/V速率增大。该模式下，关断误差放大器和报警，以减小供电电流(10mA典型值)。仅工作在VGA/混频器模式时，不需要安装元件R5、R7、C8、C9和C16。

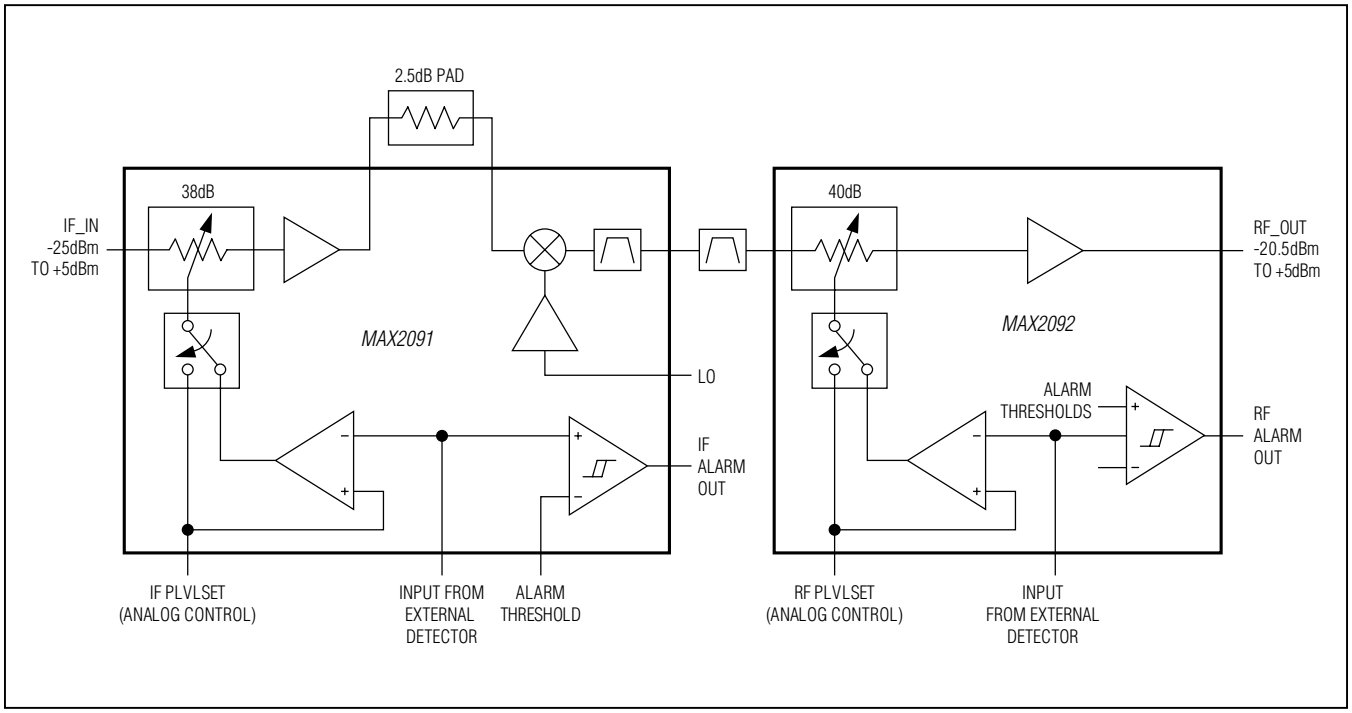


图1. 采用MAX2091和MAX2092级联的IF–RF通道

闭环ALC工作模式

闭环ALC模式下，设置CTRL1 = CTRL2 = 逻辑1。通过外部设置PLVLSET电压，当IF_IN功率为-25dBm至+5dBm时，在RF_OUT提供-3dBm。对于其它输入功率范围，PLVLSET可由外部0至2.5V的直流电压驱动，从而在RF_OUT提供所需要的输出功率(见*典型应用电路*)。误差放大器将外部检测器的电压与PLVLSET进行比较，以伺服方式驱动IF衰减器，直到误差放大器的差分输入误差电压接近为零。IF_IN的输入功率变化时，伺服环路将维持检测器的输入功率水平。理想情况下，推荐使用输出电压范围为0.1V至2.4V直流的检测器；但MAX2091能够支持输出范围在0至2.5V直流的任意检测器(已经考虑IF_OUT的耦合网络)。

配合MAX2092 RF VGA使用时，建议MAX2091的标称RF输出设置在大约-3dBm。在这一特定功率设置下，IF输入功率范围为-25dBm至+5dBm时，MAX2091和MAX2092级联后能够产生-20.5dBm至+5dBm的恒定RF输出功率，详细信息请参考图1。需要的话，可联络厂商获得有关Maxim MAX2091和MAX2092参考设计的详细信息。

控制输入

MAX2091有四路控制输入：CTRL1、CTRL2、ALM_THRES和PLVLSET。VCC必须先于这些引脚上电。如果不能实现这一条件，则必须在控制输入与控制引脚之间串联一个200Ω电阻，以限制片上ESD二极管导通。CTRL1和CTRL2为3V逻辑控制，不能由5V逻辑驱动。如果不能提供逻辑控制信号，但需要逻辑高电平，则可使用分压器由5V VCC电源产生3V逻辑高电平。

VGA输出焊盘

如图1和*典型应用电路*所示，允许在VGA输出和混频器输入之间安装一个T型衰减器。应用中使用2.5dB默认值，也可选择所要求的其它数值。或者，在较宽的工作频带内使用附加频率增益斜率修正，利用简单的均衡器电路代替衰减器。

此外，可在VGA输出和混频器输入之间使用低通滤波器，以减小下变频到混频器输出时在VGA输出产生的镜频噪声(RF + LO)，详细信息请联络厂商。

报警

DET_IN高于1.35V标称值时，报警输出(ALM)保持在逻辑高电平。ALM_THRES的输入电阻为135kΩ，由内部设置在1.35V（典型值），以在DET_IN低于1.35V时触发ALM。ALM_THRES电压也可由外部驱动，以更改功率触发门限。ALM比较器的典型滞回为29mV。

混频器LO输入

混频器设计支持-10dBm至-4dBm的LO+信号水平，LO-接地。VCC施加至MAX2091后，如果LO+低于-15dBm，混频器的LO驱动器会在RF_OUT产生有害的杂散信号。这种情况下，应向LO+施加-10dBm至-4dBm信号，使混频器正常工作。为了避免无效的LO+信号造成RF_OUT的杂散信号，可采用关断模式(CTRL1 = CTRL2 = 逻辑0)禁止RF_OUT。

布局考虑

MAX2091的引脚排列经过优化设计，能够很方便地与相关分立元件连接，实现紧凑的物理布局。MAX2091采用20引脚、TQFN封装，其裸焊盘(EP)提供了至管芯的低热阻通路。将MAX2091所在的PCB设计通过EP导热非常关键。此外，将裸焊盘通过一个低电感路径连接至电气地。EP必须直接或通过一系列电镀过孔焊接到PCB的接地区域。

表2. 典型应用电路元件值

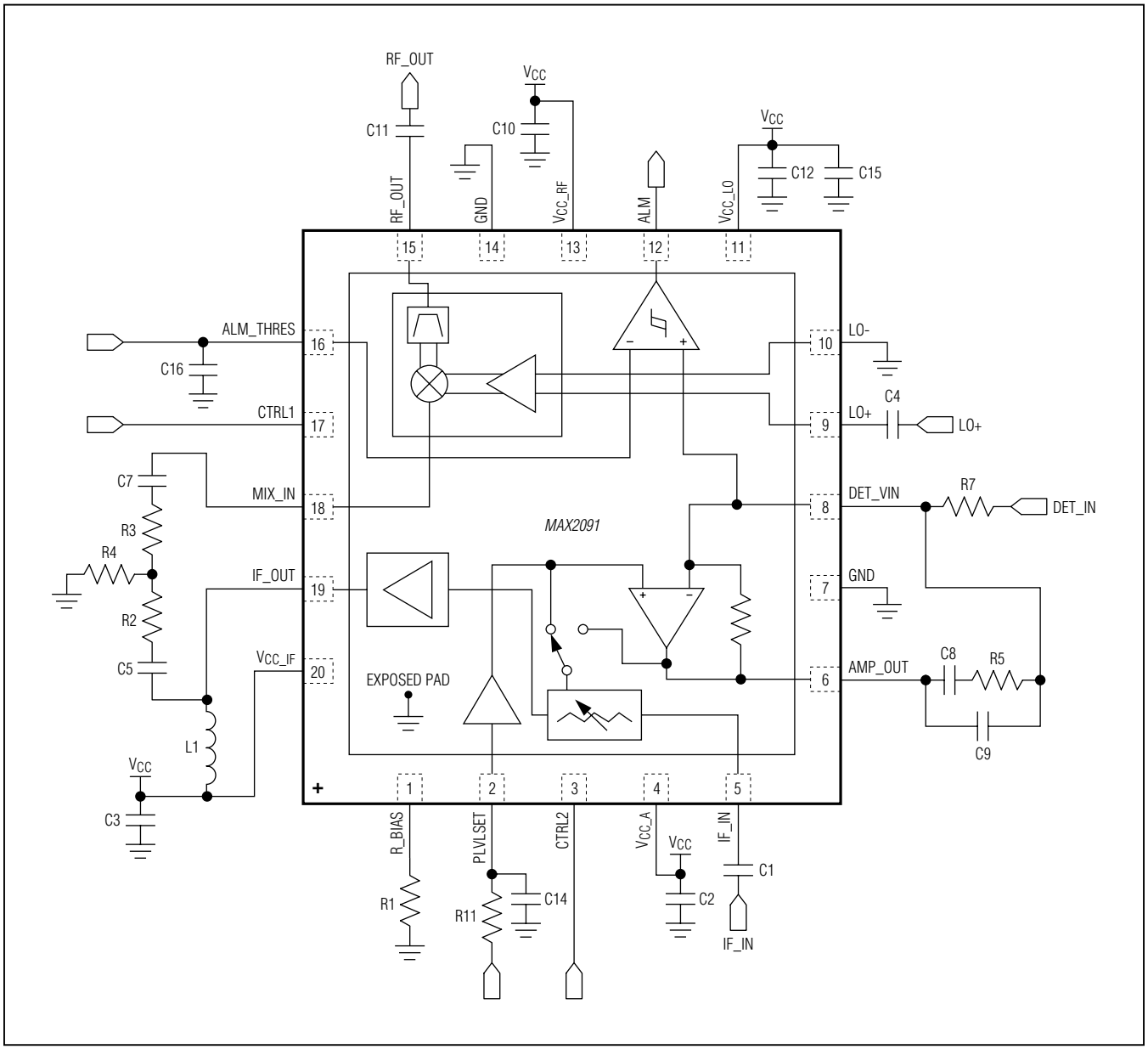
COMPONENT	MODE OF OPERATION		VALUE	SIZE	VENDOR	DESCRIPTION
	VGA/MIXER ONLY	CLOSED-ALC				
C1, C5, C7	✓	✓	1000pF	0402	Murata	C0G Dielectric
C2, C3, C10, C12	✓	✓	0.01µF	0402	Murata	X7R Dielectric
C4, C11	✓	✓	100pF	0402	Murata	C0G Dielectric
C8		✓	100nF	0603	Murata	X7R Dielectric
C9		✓	820pF	0402	Murata	C0G Dielectric
C14*			Do Not Install	0402		
C15	✓	✓	1µF	0603	Murata	X7R Dielectric
C16		✓	0.01µF	0402	Murata	X7R Dielectric
L1	✓	✓	330nH	0603	Coilcraft	Ferrite LS series 5% Tolerance
R1	✓	✓	1.78kΩ	0402	Panasonic	1% Tolerance
R2, R3**	✓	✓	7.1Ω	0402	Panasonic	1% Tolerance
R4**	✓	✓	174Ω	0402	Panasonic	1% Tolerance
R5		✓	150Ω	0402	Panasonic	1% Tolerance
R7		✓	24kΩ	0402	Panasonic	5% Tolerance
R11*	✓	✓	0Ω	0402	Panasonic	1% Tolerance
U1	✓	✓	—	20-pin TQFN (5mm x 5mm)	Maxim	MAX2091ETP+

注：*Mode of Operation栏中的“对号”表示该元件用于各项相关应用。*

**C14和R11构成可选的低通网络，以滤除外部PLVLSET控制源中的潜在噪声。*

***R2-R4构成可选的2.5dB固定衰减器。*

典型应用电路


RF_OUT
VCC
C11
C10
VCC
C12
C15
RF_OUT
GND
VCC_RF
ALM
VCC_LO
15
14
13
12
11
ALM_THRES
16
C16
CTRL1
17
MIX_IN
18
IF_OUT
19
VCC_IF
20
EXPOSED PAD
MAX2091
10
LO-
9
LO+
C4
LO+
8
DET_VIN
R7
DET_IN
7
GND
6
AMP_OUT
C8
R5
C9
C7
R3
R4
R2
C5
L1
VCC
C3
1
2
3
4
5
R_BIAS
PLVLSET
CTRL2
VCC_A
VCC
IF_IN
C1
R1
R11
C14
C2
IF_IN

定购信息

器件	温度范围	引脚–封装
MAX2091ETP+	-40°C to +95°C	20 TQFN-EP*
MAX2091ETP+T	-40°C to +95°C	20 TQFN-EP*
MAX2091BETP+**	-40°C to +95°C	20 TQFN-EP*
MAX2091BETP+T**	-40°C to +95°C	20 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
***未来产品—请联系工厂索取样本。*
T = 卷带包装。

芯片信息

PROCESS: SiGe BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maximintegrated.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
20 TQFN-EP	T2055-5	21-0140	90-0010

修订历史

修订号	修订日期	说明	修改页
0	7/12	最初版本。	—

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