19-6173; Rev 0; 12/11
备有评估板

MAX14591

高速、漏极开路逻辑电平转换器

概述

MAX14591为双通道、双向逻辑电平转换器，为多电压供电系统的数据传输提供必要的电平转换。外部电压V_{CC}和V_L设置器件两侧的逻辑电平。V_L侧的逻辑信号被转换成V_{CC}侧相同的逻辑信号，反之亦然。

器件优化用于高速、开漏工作的I²C总线和数据输入/输出(MDIO)管理总线。当$\overline{TS}$为高电平时，器件允许上拉到供电的I/O端口，从而保证电平转换功能关闭时，供电侧的I²C不受任何干扰地持续工作。

器件工作在-40°C至+85°C扩展级温度范围，采用8焊球WLP封装和8引脚TDFN封装。

应用

I²C通信设备

MDIO通信设备

通用逻辑电平转换

优势与特性

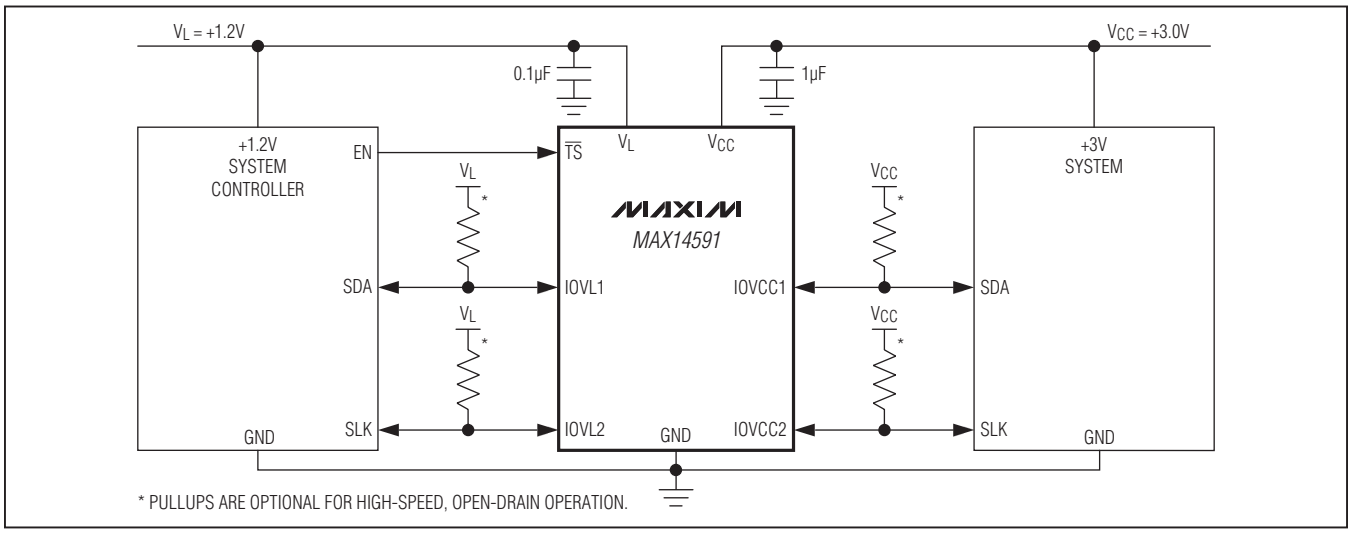
- 满足工业标准
  - ✧ 满足标准速度、快速和高速I²C的需求*
  - ✧ 支持高于4MHz的MDIO开漏总线*
- 提高设计灵活性
  - ✧ V_L侧可低至0.9V
  - ✧ 支持高于8MHz的推挽工作
- 低功耗
  - ✧ 23µA (典型值) V_{CC}电源电流
  - ✧ 0.5µA (典型值) V_L电源电流
- 高度集成
  - ✧ $\overline{TS}$为高电平时，供电侧的上拉电阻使能
  - ✧ 12kΩ (最大值)内部上拉
  - ✧ 低导通电阻R_{ON}：17Ω (最大值)
- 节省空间
  - ✧ 8焊球、0.4mm间距、0.8mm x 1.6mm WLP封装
  - ✧ 8引脚、2mm x 2mm TDFN封装

** 需要外部上拉。*

定购信息在数据资料的最后给出。

相关型号以及配合该器件使用的推荐产品，请参见：china.maxim-ic.com/MAX14591.related。

典型工作电路



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to GND.
V_{CC}, V_L, $\overline{TS}$ .....-0.5V to +6V
IOVCC1, IOVCC2 ..... -0.5V to +(V_{CC} + 0.5V)
IOVL1, IOVL2 .....-0.5V to +(V_L + 0.5V)
Short-Circuit Duration IOVCC1, IOVCC2,
IOVL1, IOVL2 to GND .....Continuous
V_{CC}, IOVCC_ Maximum Continuous Current at +110°C...100mA
V_L, IOVL_ Maximum Continuous Current at +110°C 40mA
$\overline{TS}$ Maximum Continuous Current at +110°C.....70mA
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 6.2mW/°C above +70°C).....496mW
WLP (derate 11.8mW/°C above +70°C).....944mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (TDFN only, soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA})..... 162°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... 20°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})..... 85°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to min(V_{CC} + 0.3V, +3.6V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power Supply Range	V_L		0.9		5.5	V
	V_{CC}		1.65		5.5	
V_{CC} Supply Current	I_{CC}	IOVCC_ = V_{CC}, IOVL_ = V_L, $\overline{TS}$ = V_{CC}		23	47	µA
V_L Supply Current	I_L	IOVCC_ = V_{CC}, IOVL_ = V_L, $\overline{TS}$ = V_{CC}		0.5	6	µA
V_{CC} Shutdown Supply Current	$I_{CC-SHDN}$	$\overline{TS}$ = GND		1	2.2	µA
		$\overline{TS}$ = V_{CC}, V_L = GND, IOVCC_ = unconnected		1	2.2	
V_L Shutdown Supply Current	I_{L-SHDN}	$\overline{TS}$ = GND		0.1	1	µA
		$\overline{TS}$ = V_L, V_{CC} = GND, IOVL_ = unconnected		0.1	1	
IOVCC_, IOVL_ Three-State Leakage Current	I_{LEAK}	T_A = +25°C, $\overline{TS}$ = GND		0.1	1	µA
$\overline{TS}$ Input Leakage Current	I_{LEAK_TS}	T_A = +25°C			1	µA
V_{CC} Shutdown Threshold	V_{TH_VCC}	$\overline{TS}$ = V_L, V_{CC} falling, V_L = 0.9V		0.8	1.35	V
V_L Shutdown Threshold	V_{TH_VL}	$\overline{TS}$ = V_{CC}, V_L falling	0.15	0.3	0.8	V
V_L Above V_{CC} Shutdown Threshold	V_{TH_VL-VCC}	V_L rising above V_{CC}, V_{CC} = +1.65V	0.4	0.73	1.1	V
IOVL_ Pullup Resistor	R_{VL_PU}	Inferred from V_{OHL} Measurements	3	7.6	12	kΩ
IOVCC_ Pullup Resistor	R_{VCC_PU}	Inferred from V_{OHC} Measurements	3	7.6	12	kΩ
IOVL_ to IOVCC_ DC Resistance	$R_{IOVL-IOVCC}$	Inferred from V_{OHx} Measurements		6	17	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to min(V_{CC} + 0.3V, +3.6V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
IOVL_ Input-Voltage High	V_{IHL}	IOVL_ rising, V_L = +0.9V, V_{CC} = +1.65V (Note 4)	V_L - 0.2			V
IOVL_ Input-Voltage Low	V_{ILL}	IOVL_ falling, V_L = +0.9V, V_{CC} = +1.65V (Note 4)			0.15	V
IOVCC_ Input-Voltage High	V_{IHC}	IOVCC_ rising, V_L = +0.9V, V_{CC} = +1.65V (Note 4)	V_{CC} - 0.4			V
IOVCC_ Input-Voltage Low	V_{ILC}	IOVCC_ falling, V_L = +0.9V, V_{CC} = +1.65V (Note 4)			0.2	V
$\overline{TS}$ Input-Voltage High	V_{IH}	$\overline{TS}$ rising, V_L = +0.9V or +3.6V, $V_{CC} > V_L$	V_L - 0.15			V
$\overline{TS}$ Input-Voltage Low	V_{IL}	$\overline{TS}$ falling, V_L = +0.9V or +3.6V, $V_{CC} > V_L$			0.2	V
IOVL_ Output-Voltage High	V_{OHL}	IOVL_ source current 20µA, $V_{IOVCC\_}$ = V_L to V_{CC} ($V_{CC} \geq V_L$)	0.7 x V_L			V
IOVL_ Output-Voltage Low	V_{OLL}	IOVL_ sink current 5mA, $V_{IOVCC\_} \leq 0.05V$			0.2	V
IOVCC_ Output-Voltage High	V_{OHC}	IOVCC_ source current 20µA, $V_{IOVL\_}$ = V_L	0.7 x V_{CC}			V
IOVCC_ Output-Voltage Low	V_{OLC}	IOVCC_ sink current 5mA, $V_{IOVL\_} \leq 0.05V$			0.25	V
RISE/FALL TIME ACCELERATOR STAGE						
Accelerator Pulse Duration		V_L = +0.9V, V_{CC} = +1.65V	9	22	48	ns
IOVL_ Output Accelerator Source Impedance		V_L = +0.9V, IOVL_ = GND, V_{CC} = +1.65V		26		Ω
		V_L = +3.3V, IOVL_ = GND, V_{CC} = +5V		6.8		
IOVCC_ Output Accelerator Source Impedance		V_{CC} = +1.65V, IOVCC_ = GND		26		Ω
		V_{CC} = +5V, IOVCC_ = GND		6.5		
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			+150		°C
Thermal Hysteresis	T_{HYST}			10		°C
ESD PROTECTION						
All Pins		HBM		±2		kV

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to +3.6V, $V_{CC} \geq V_L$, $\overline{TS}$ = V_L, C_{VCC} = 1µF, C_{VL} = 0.1µF, $C_{IOVL\_} \leq$ 100pF, $C_{IOVCC\_} \leq$ 100pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3V, V_L = +1.2V and T_A = +25°C. All timing is 10% to 90% for rise time and 90% to 10% for fall time.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time for Q1	t_{ON}	$V_{\overline{TS}}$ = 0V to V_L (see the *Block Diagram*)			80	200	µs
IOVCC_ Rise Time	t_{RCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)			3.7	10	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 2)			7.9		
IOVCC_ Fall Time	t_{FCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)			5.1	15	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 2)			6.1		
IOVL_ Rise Time	t_{RL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)			2.7	8	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 4)			13		
IOVL_ Fall Time	t_{FL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)			2.8	12	ns
		Open-drain driving, V_L = +1.2V, V_{CC} = +3V (Figure 4)			3.3		
Propagation Delay (Driving IOVL_)	t_{PD_LCC}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 1)	Rising		3.4	7	ns
			Falling		3	8	
Propagation Delay (Driving IOVCC_)	t_{PD_CCL}	Push-pull driving, V_L = +1.2V, V_{CC} = +3V (Figure 3)	Rising		1.9	3	ns
			Falling		1.5	7	
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 6ns				1.3	ns
Maximum Data Rate		Push-pull operation		8			MHz
		Open-drain operation (Note 6)		4			

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 4: V_{IHL}, V_{ILL}, V_{IHC}, and V_{ILC} are intended to define the range where the accelerator triggers.

Note 5: Guaranteed by design.

Note 6: External pullup resistors are required.

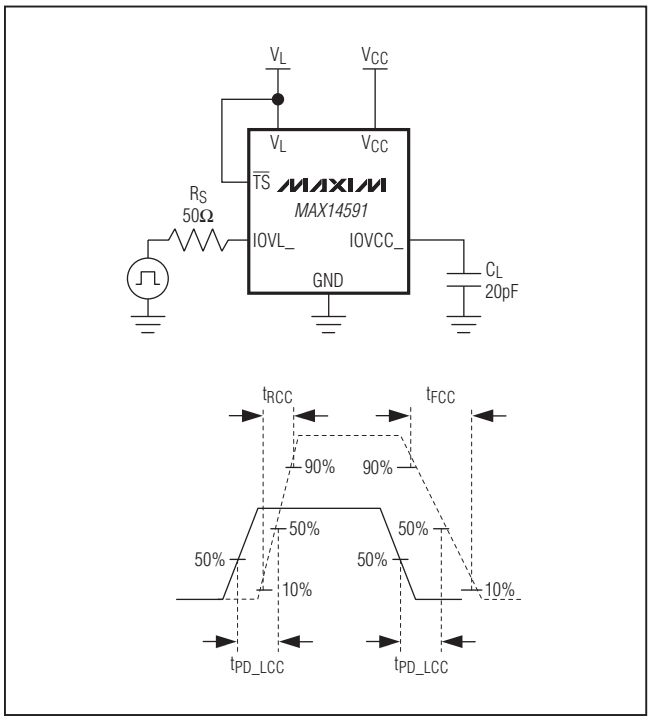


图1. 推挽驱动IOVL_

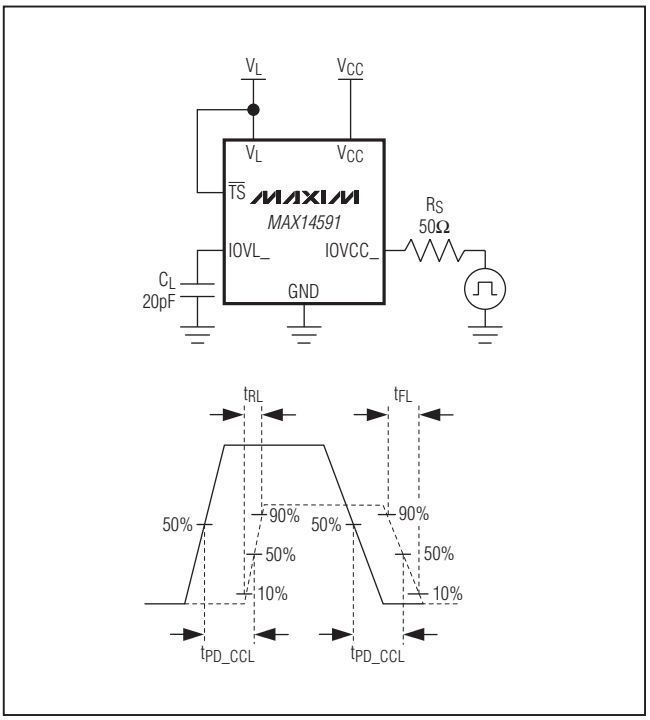


图3. 推挽驱动IOVCC_

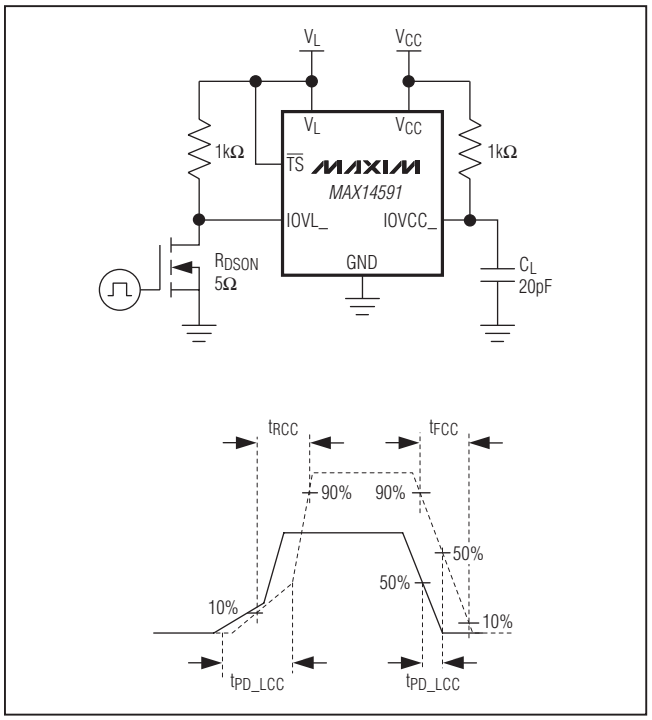


图2. 开漏驱动IOVL_

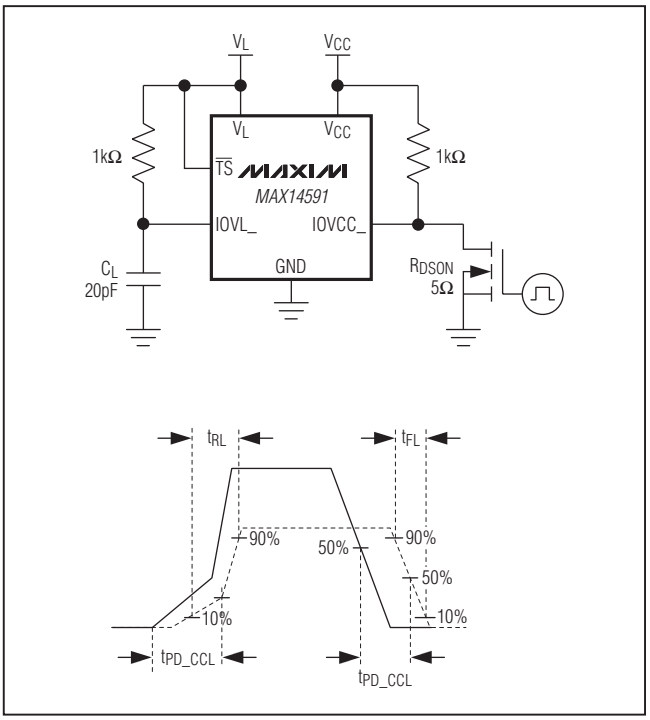
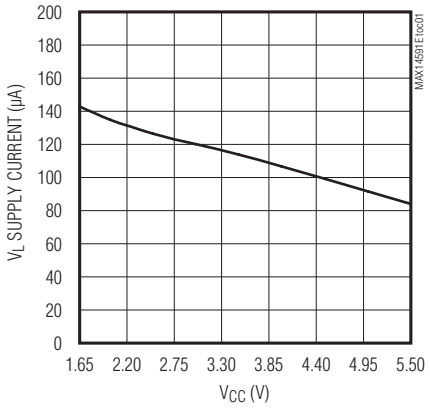


图4. 开漏驱动IOVCC_

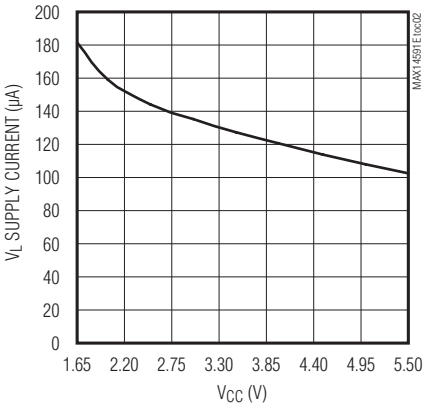
典型工作特性

(V_{CC} = +3V, V_L = +1.5V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

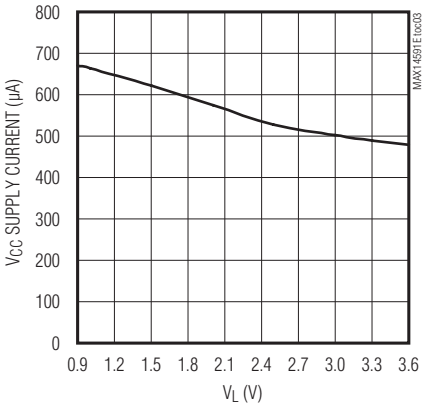
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVL_)



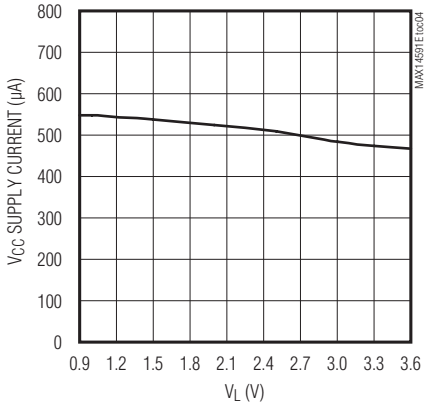
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVCC_)



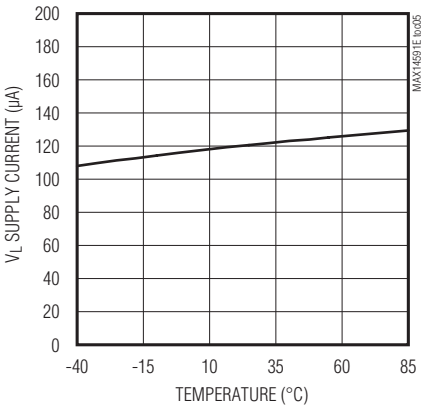
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVL_)



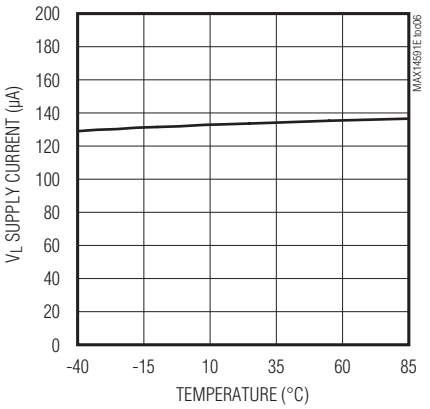
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVCC_)



V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (OPEN-DRAIN DRIVING ONE IOVL_)



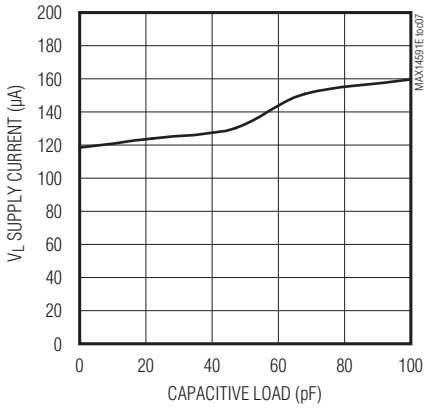
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL DRIVING ONE IOVCC_)



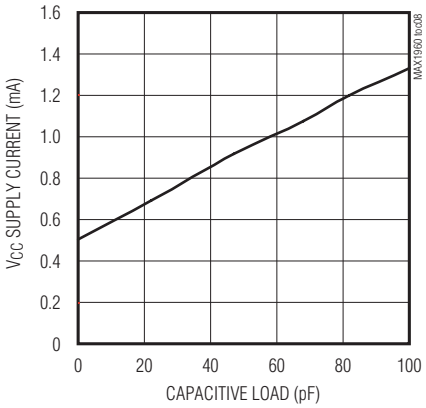
典型工作特性(续)

(V_{CC} = +3V, V_L = +1.5V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

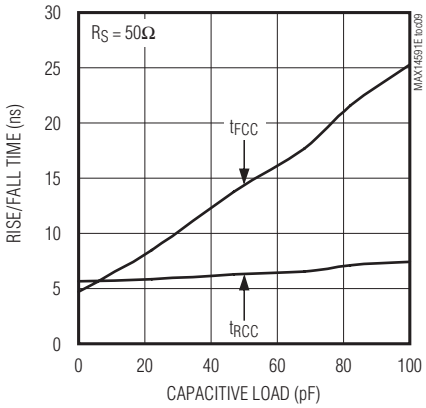
V_L DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (OPEN-DRAIN DRIVING ONE IOVL_)



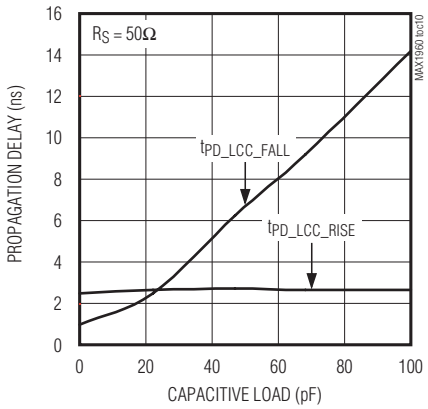
V_{CC} DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



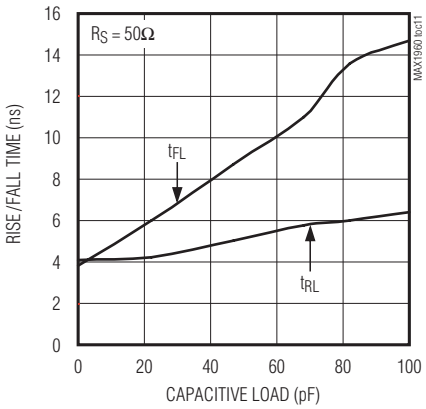
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



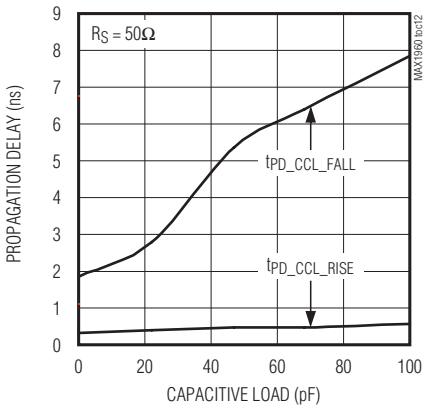
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVCC_)



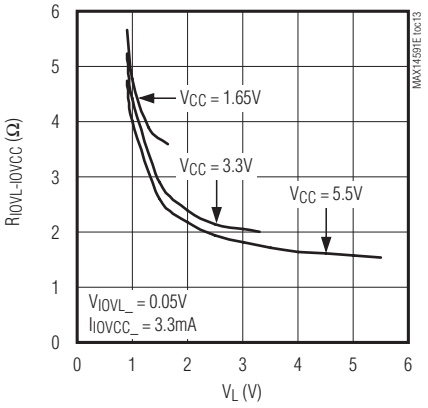
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVCC_)



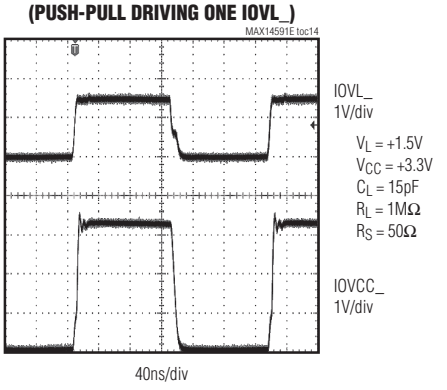
典型工作特性(续)

(V_{CC} = +3V, V_L = +1.5V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

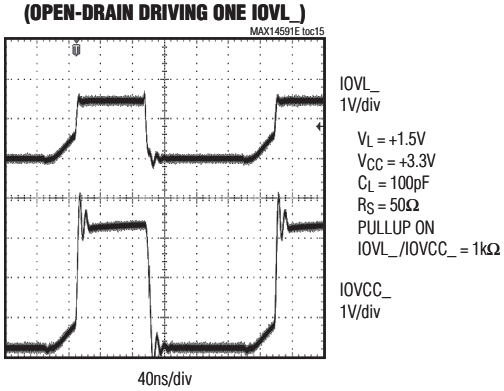
RIOVL-IOVCC vs. VL



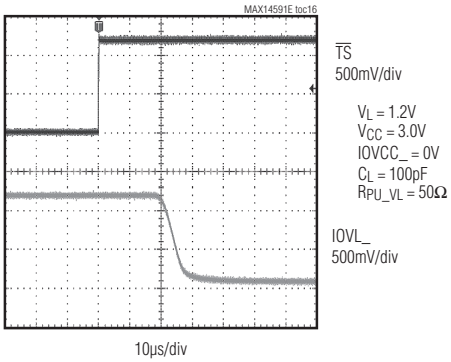
RAIL-TO-RAIL DRIVING (PUSH-PULL DRIVING ONE IOVL_)



RAIL-TO-RAIL DRIVING (OPEN-DRAIN DRIVING ONE IOVL_)

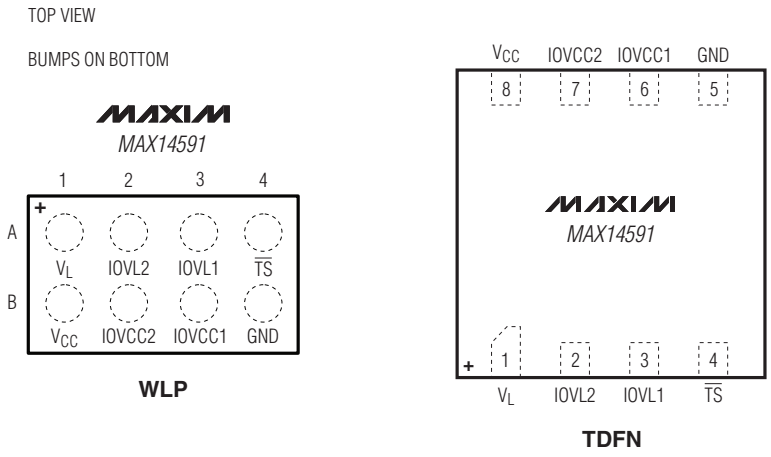


EXITING SHUTDOWN MODE



高速、漏极开路逻辑电平转换器

引脚配置

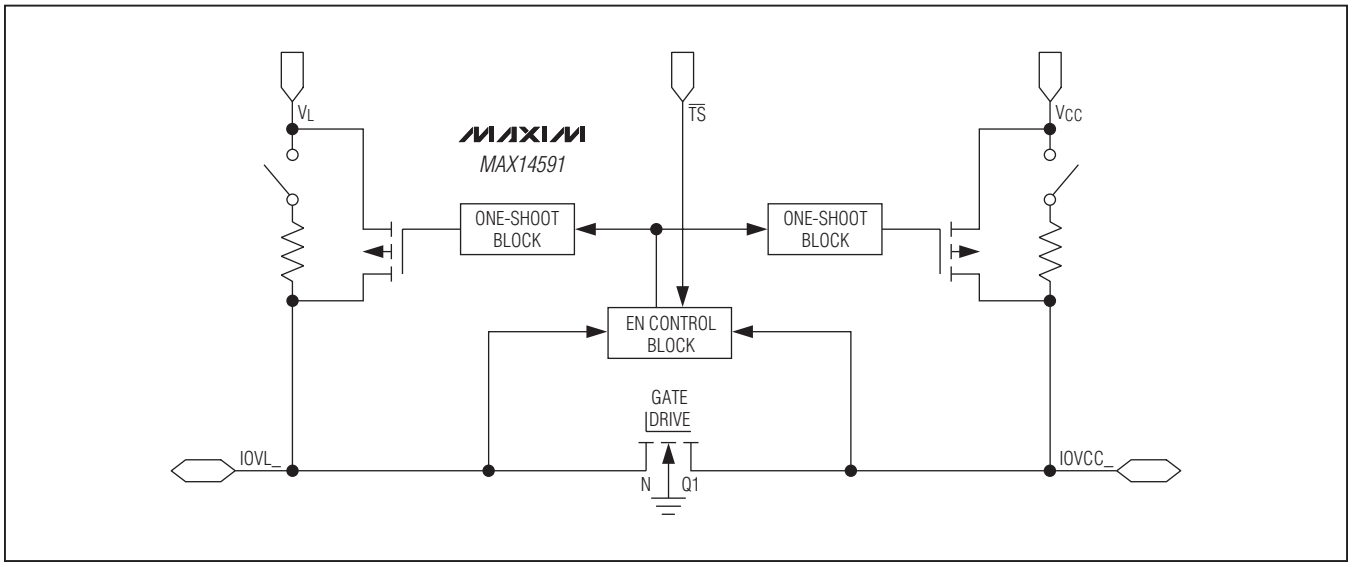


引脚说明

焊球/引脚		名称	功能
WLP	**TDFN**		
A1	1	V_L	逻辑电源电压，+0.9V至min(V_{CC} + 0.3V, +3.6V)。利用0.1µF陶瓷电容将V_L旁路至GND，电容尽量靠近器件放置。
A2	2	IOVL2	输入/输出2，以V_L为参考。
A3	3	IOVL1	输入/输出1，以V_L为参考。
A4	4	$\overline{TS}$	低电平有效三态输入。驱动$\overline{TS}$为低电平时，将器件置于关断模式，此时输出为高阻，断开内部上拉电阻；驱动$\overline{TS}$为高电平时，器件置于正常工作模式。
B1	8	V_{CC}	电源电压，+1.65V至+5.5V。利用1µF陶瓷电容将V_{CC}旁路至GND，电容尽量靠近器件放置。
B2	7	IOVCC2	输入/输出2，以V_{CC}为参考。
B3	6	IOVCC1	输入/输出1，以V_{CC}为参考。
B4	5	GND	地。

高速、漏极开路逻辑电平转换器

方框图



详细说明

MAX14591为双通道、双向电平转换器。器件将V_L侧低至+0.9V的低压电平转换成V_{CC}侧的高压电平，反之亦然。器件优化于开漏、高速工作环境，例如：I²C总线和MDIO总线。

器件具有低导通电阻(最大17Ω)，这一点对于高速、开漏工作非常重要。器件内置上拉电阻，当对应的电源打开，并且$\overline{TS}$为高电平时，提供有效上拉。

电平转换

为了使器件正常工作，应确保+1.65V ≤ V_{CC} ≤ +5.5V，以及+0.9V ≤ V_L ≤ V_{CC}。V_L供电，而V_{CC}小于V_L时，器件将自动禁用逻辑电平转换功能。此外，$\overline{TS}$ = GND时，器件进入关断模式。

高速工作

器件满足高速I²C和MDIO开漏工作要求。开漏工作模式下，最大数据率至少为4MHz，总线上的总电容应等于或小于100pF。

三态输入TS

器件具有三态输入，可将器件置于高阻模式。$\overline{TS}$为低电平时，IOVCC_和IOVL_全部为高阻，断开内部上拉电阻。$\overline{TS}$为高电平时，如果对应电源在稳压范围以内，则连通内部上拉电阻；该侧没有电源供电时，则断开电阻。许多便携式应用中，一侧电源关闭，但另一侧仍保持工作，此时需要接上拉电阻，器件的这一功能省去了外部上拉电阻。在两个电源均处于规定范围以内之前，关闭电平转换功能。

热关断保护

器件具有热关断保护，防止器件过热损坏。结温超过+150°C (典型值)时，器件进入热关断；温度下降大约10°C (典型值)后，器件恢复正常工作。器件处于热关断时，禁用电平转换功能。

应用信息

布局建议

MAX14591电路板布板时，应遵循标准的高速布局规则。例如，为将线路耦合降至最小，使其它未连接至器件的信号线与器件的输入和输出线之间的距离应保持在PCB基板高度的1倍以上。

增强ESD

所有引脚具有ESD保护架构，在器件操作与装配期间可承受高达±2kV (HBM)的静电放电冲击。发生ESD事件后，器件将继续保持工作，不会闭锁。

ESD测试条件

ESD性能取决于多种条件。关于测试配置、测试方法及测试结果的可靠性报告，请联系Maxim。

人体模式

图5所示为人体模型，图6所示为对低阻放电时产生的电流波形。该模型包括一个100pF电容，先充电至所要求的ESD电压，然后通过1.5kΩ电阻向被测器件放电。

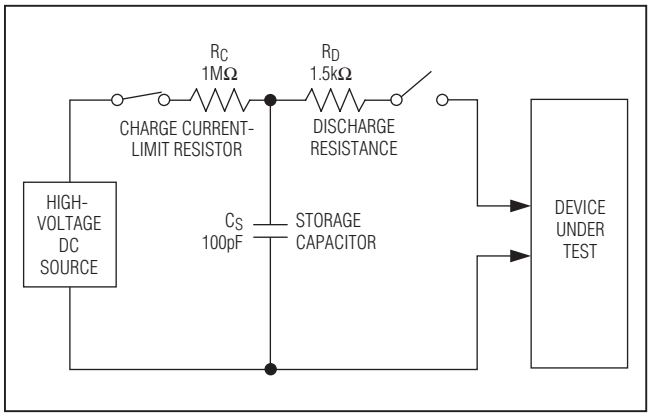


图5. 人体ESD测试模型

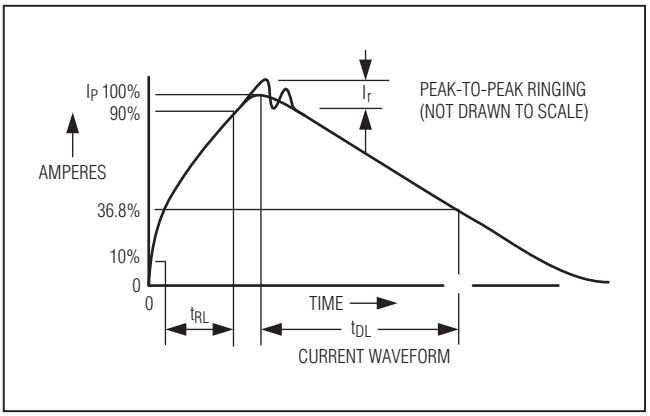


图6. 人体测试电流波形

定购信息

PART	TOP MARK	PIN-PACKAGE
MAX14591ETA+T	BNS	8 TDFN-EP*
MAX14591EWA+T	AAD	8 WLP

注：所有器件均可工作在-40°C至+85°C温度范围。
+表示无铅(Pb)/符合RoHS标准的封装。
T = 卷带包装。

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
8 TDFN-EP	T822CN+1	**21-0487**	**90-0349**
8 WLP	W80A1+1	**21-0555**	参见 **应用笔记1891**

修订历史

修订号	修订日期	说明	修改页
0	12/11	最初版本。	—

Maxim北京办事处
北京8328信箱 邮政编码100083
免费电话：800 810 0310
电话：010–6211 5199
传真：010–6211 5299