

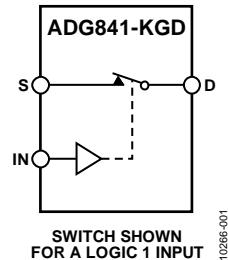
## Known Good Die

**ADG841-KGD**

### FEATURES

- Ultralow on resistance**
- 0.28 Ω typical**
- 0.48 Ω max at 125°C**
- Excellent audio performance, ultralow distortion**
- 0.025 Ω typical**
- 0.052 Ω max RON flatness**
- 1.65 V to 3.6 V single supply**
- High current carrying capability**
- 300 mA continuous current**
- 500 mA peak current**
- Automotive temperature range: -40°C to +125°C**
- Rail-to-rail operation**
- Typical power consumption (<0.01 μW)**
- Known good die (KGD): these die are fully guaranteed to data sheet specifications**

### FUNCTIONAL BLOCK DIAGRAM



SWITCH SHOWN  
FOR A LOGIC 1 INPUT

102688-001

Figure 1.

### APPLICATIONS

- Handsets**
- PDAs**
- MP3 players**
- Power routing**
- Battery-powered systems**
- Communication systems**
- Modems**
- PCMCIA cards**

### GENERAL DESCRIPTION

The **ADG841-KGD** is a low voltage CMOS device containing a single-pole, single-throw (SPST) switch. The **ADG841-KGD** is closed for a Logic 1 input. The device offers ultralow on resistance of less than 0.48 Ω over the full temperature range. The **ADG841-KGD** is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies.

Additional application and technical information can be found in the [ADG841](#) data sheet.

### PRODUCT HIGHLIGHTS

1. <0.48 Ω over full temperature range of -40°C to +125°C.
2. Compatible with 1.8 V CMOS logic.
3. High current handling capability (300 mA continuous current at 3.3 V).
4. Low THD + N (0.02% typical).

Table 1. **ADG841-KGD** Truth Table

Logic (IN)	<b>ADG841-KGD</b>
0	Off
1	On

Rev. B

[Document Feedback](#)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

Features .....	1	Specifications—1.65 V to 1.95 .....	5
Applications.....	1	Absolute Maximum Ratings .....	6
Functional Block Diagram .....	1	ESD Caution .....	6
General Description .....	1	Pin Configuration and Function Descriptions.....	7
Product Highlights .....	1	Test Circuits.....	8
Revision History .....	2	Outline Dimensions.....	9
Specifications—2.7 V to 3.6 V .....	3	Die Specifications and Assembly Recommendations .....	9
Specifications—2.5 V ± 0.2 V .....	4	Ordering Guide .....	9

## REVISION HISTORY

### 12/14—Rev. A to Rev. B

Changes to Table 7 .....

9

### 10/14—Rev. 0 to Rev. A

Changes to Test Circuits Section Layout .....

8

Changes to Table 7 .....

9

### 11/11—Revision 0: Initial Version

## SPECIFICATIONS—2.7 V TO 3.6 V

$V_{DD}$  = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted. The temperature range is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 2.

Parameter	+25°C	−40°C to +85°C		−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range			0 V to $V_{DD}$		V	$V_{DD} = 2.7\text{ V}$
On Resistance ( $R_{ON}$ )	0.28			$\Omega$ typ	$V_{DD} = 2.7\text{ V}, V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -100\text{ mA}$	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.37	0.43	0.48	$\Omega$ max	See Figure 3	
	0.025			$\Omega$ typ	$V_{DD} = 2.7\text{ V}, V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -100\text{ mA}$	
	0.034	0.044	0.052	$\Omega$ max		
LEAKAGE CURRENTS						$V_{DD} = 3.6\text{ V}$
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_S = 0.6\text{ V}/3.3\text{ V}, V_D = 3.3\text{ V}/0.6\text{ V}$ ; see Figure 4	
Channel On Leakage $I_D, I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6\text{ V}$ or $3.3\text{ V}$ ; see Figure 5	
DIGITAL INPUTS						
Input High Voltage, $V_{INH}$			2	V min		
Input Low Voltage, $V_{INL}$			0.8	V max		
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$	
			$\pm 0.1$	$\mu\text{A}$ max		
Digital Input Capacitance, $C_{IN}$	3.2			pF typ		
DYNAMIC CHARACTERISTICS <sup>1</sup>						
$t_{ON}$	10.5			ns typ	$R_L = 50\ \Omega, C_L = 35\ \text{pF}$	
	14	15.5	16.5	ns max	$V_S = 1.5\text{ V}$ ; see Figure 8	
$t_{OFF}$	6.5			ns typ	$R_L = 50\ \Omega, C_L = 35\ \text{pF}$	
	7.8	8	8.2	ns max	$V_S = 1.5\text{ V}$ ; see Figure 8	
Charge Injection	200			pC typ	$V_S = 1.5\text{ V}, R_S = 0\ \Omega, C_L = 1\ \text{nF}$ ; see Figure 9	
Off Isolation	−54			dB typ	$R_L = 50\ \Omega, C_L = 5\ \text{pF}, f = 100\ \text{kHz}$ ; see Figure 6	
Total Harmonic Distortion (THD + N)	0.012			%	$R_L = 32\ \Omega, f = 20\ \text{Hz}$ to $20\ \text{kHz}, V_S = 3\ \text{V p-p}$	
Insertion Loss	−0.02			dB typ	$R_L = 50\ \Omega, C_L = 5\ \text{pF}$ ; see Figure 7	
−3 dB Bandwidth	21			MHz typ	$R_L = 50\ \Omega, C_L = 5\ \text{pF}$ ; see Figure 7	
$C_S$ (OFF)	160			pF typ		
$C_D$ (OFF)	160			pF typ		
$C_D, C_S$ (ON)	238			pF typ		
POWER REQUIREMENTS						$V_{DD} = 3.6\text{ V}$
$I_{DD}$	0.003	1	4	$\mu\text{A}$ typ	Digital inputs = 0 V or 3.6 V	
				$\mu\text{A}$ max		

<sup>1</sup> Guaranteed by design; not subject to production test.

## SPECIFICATIONS— $2.5\text{ V} \pm 0.2\text{ V}$

$V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. The temperature range is  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Table 3.

Parameter	+25°C	−40°C to +85°C		−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.3				$\Omega$ typ	$V_{DD} = 2.3\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -100\text{ mA}$
	0.35	0.4		0.45	$\Omega$ max	See Figure 3
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.025				$\Omega$ typ	$V_{DD} = 2.3\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -100\text{ mA}$
	0.04	0.05		0.05	$\Omega$ max	
LEAKAGE CURRENTS						
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$				nA typ	$V_{DD} = 2.7\text{ V}$
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$				nA typ	$V_S = 0.6\text{ V}/2.4\text{ V}$ , $V_D = 2.4\text{ V}/0.6\text{ V}$ ; see Figure 4
DIGITAL INPUTS						
Input High Voltage, $V_{INH}$			1.7		V min	
Input Low Voltage, $V_{INL}$			0.7		V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\pm 0.1$	$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
Digital Input Capacitance, $C_{IN}$	3.2				$\mu\text{A}$ max	
DYNAMIC CHARACTERISTICS <sup>1</sup>					pF typ	
$t_{ON}$	13				ns typ	$R_L = 50\text{ }\Omega$ , $C_L = 35\text{ pF}$
	16.5	18	19		ns max	$V_S = 1.5\text{ V}$ ; see Figure 8
$t_{OFF}$	7				ns typ	$R_L = 50\text{ }\Omega$ , $C_L = 35\text{ pF}$
	8.2	8.4	8.6		ns max	$V_S = 1.5\text{ V}$ ; see Figure 8
Charge Injection	150				pC typ	$V_S = 1.25\text{ V}$ , $R_S = 0\text{ }\Omega$ , $C_L = 1\text{ nF}$ ; see Figure 9
Off Isolation	−54				dB typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 6
Total Harmonic Distortion (THD + N)	0.022				%	$R_L = 32\text{ }\Omega$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ , $V_S = 1.5\text{ V}$ p-p
Insertion Loss	−0.02				dB typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ ; see Figure 7
−3 dB Bandwidth	21				MHz typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ ; see Figure 7
$C_S$ (OFF)	170				pF typ	
$C_D$ (OFF)	170				pF typ	
$C_D$ , $C_S$ (ON)	238				pF typ	
POWER REQUIREMENTS						
$I_{DD}$	0.003	1	4		$\mu\text{A}$ typ	$V_{DD} = 2.7\text{ V}$
					$\mu\text{A}$ max	Digital inputs = 0 V or 2.7 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**SPECIFICATIONS—1.65 V TO 1.95**

$V_{DD}$  = 1.65 V to 1.95 V, GND = 0 V, unless otherwise noted. The temperature range is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 4.

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.37			$\Omega$ typ	$V_{DD} = 1.8 \text{ V}, V_S = 0 \text{ V to } V_{DD}, I_{DS} = -100 \text{ mA}$
	0.4	0.84	0.84	$\Omega$ max	See Figure 3
	0.6	1.8	1.8	$\Omega$ max	$V_{DD} = 1.65 \text{ V}, V_S = 0 \text{ V to } V_{DD}, I_{DS} = -100 \text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.17			$\Omega$ typ	$V_{DD} = 1.65 \text{ V}, V_S = 0 \text{ V to } V_{DD}, I_{DS} = -100 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_{DD} = 1.95 \text{ V}$
Channel On Leakage $I_D, I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = 0.6 \text{ V}/1.65 \text{ V}, V_D = 1.65 \text{ V}/0.6 \text{ V}; \text{ see Figure 4}$
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			0.65 $V_{DD}$	V min	
Input Low Voltage, $V_{INL}$			0.35 $V_{DD}$	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.1$	$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
Digital Input Capacitance, $C_{IN}$	4			$\mu\text{A}$ max	
DYNAMIC CHARACTERISTICS <sup>1</sup>				pF typ	
$t_{ON}$	19			ns typ	$R_L = 50 \Omega, C_L = 35 \text{ pF}$
	26	28	30	ns max	$V_S = 1.5 \text{ V}; \text{ see Figure 8}$
$t_{OFF}$	8			ns typ	$R_L = 50 \Omega, C_L = 35 \text{ pF}$
	9.5	9.8	10	ns max	$V_S = 1.5 \text{ V}; \text{ see Figure 8}$
Charge Injection	100			pC typ	$V_S = 1 \text{ V}, R_S = 0 \text{ V}, C_L = 1 \text{ nF}; \text{ see Figure 9}$
Off Isolation	–54			dB typ	$R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 100 \text{ kHz}; \text{ see Figure 6}$
Total Harmonic Distortion (THD + N)	0.14			%	$R_L = 32 \Omega, f = 20 \text{ Hz to } 20 \text{ kHz}, V_S = 1.2 \text{ V p-p}$
Insertion Loss	–0.02			dB typ	$R_L = 50 \Omega, C_L = 5 \text{ pF}; \text{ see Figure 7}$
–3 dB Bandwidth	21			MHz typ	$R_L = 50 \Omega, C_L = 5 \text{ pF}; \text{ see Figure 7}$
$C_S$ (OFF)	178			pF typ	
$C_D$ (OFF)	178			pF typ	
$C_D, C_S$ (ON)	238			pF typ	
POWER REQUIREMENTS					
$I_{DD}$	0.003	1	4	$\mu\text{A}$ typ	$V_{DD} = 1.95 \text{ V}$
				$\mu\text{A}$ max	Digital inputs = 0 V or 1.95 V

<sup>1</sup> Guaranteed by design; not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +4.6 V
Analog Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs <sup>1</sup>	-0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C

<sup>1</sup> Overvoltages at S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

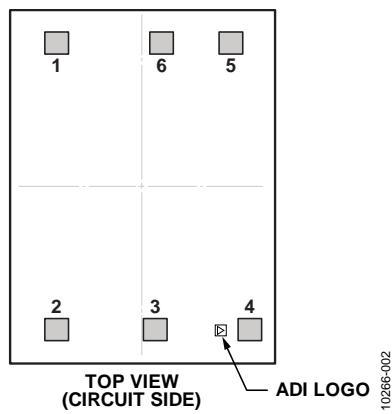
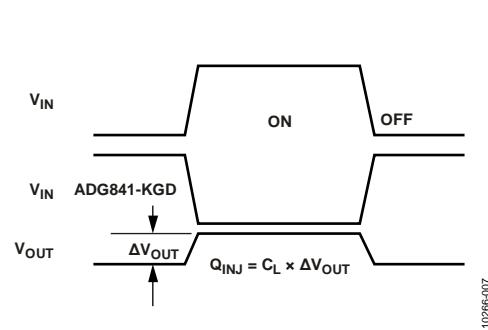
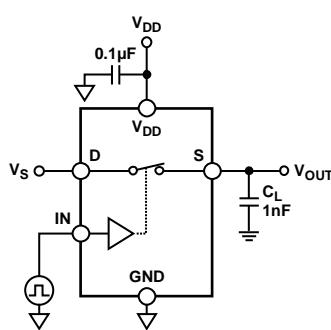
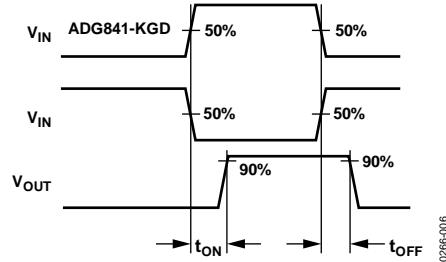
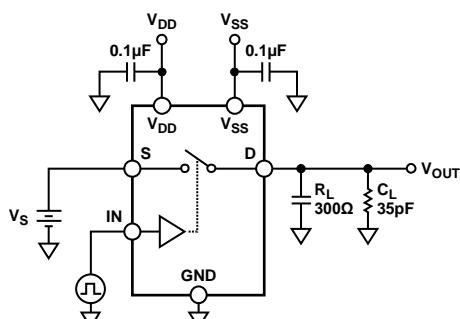
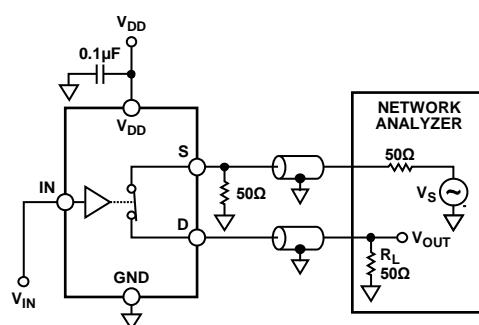
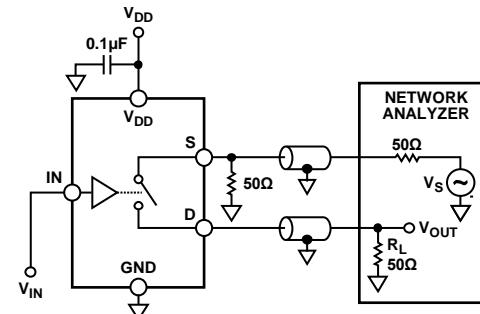
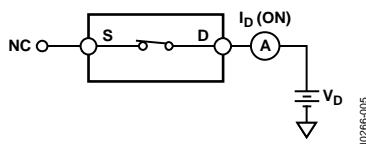
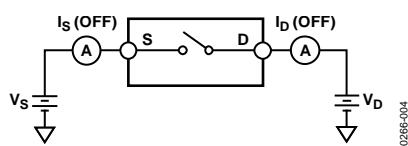
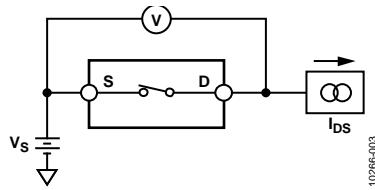


Table 6. Pad Function Descriptions

Pad No.	X-Axis (μm)	Y-Axis (μm)	Mnemonic	Pad Type	Description
1	-254	+401	V <sub>DD</sub>	Single	Positive Power Supply Pad.
2	-254	-401	IN	Single	Logic Control Input Pad.
3	+6	-401	S	Single	Source Pad.
4	+306	-401	GND	Single	Ground Pad.
5	+249	+401	NC	Single	No Connect.
6	+39	+401	D	Single	Drain Pad.

## TEST CIRCUITS



## OUTLINE DIMENSIONS

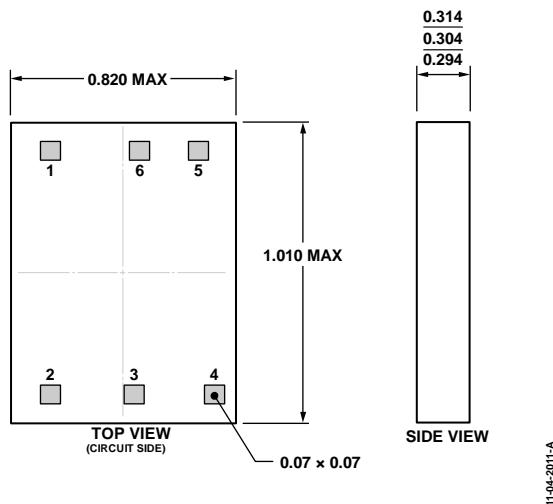


Figure 10. 6-Pad Bare Die [CHIP]  
(C-6-3)

Dimensions shown in millimeters

## DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Chip Size	735 x 925	µm
Scribe Line Width	85 x 85	µm
Die Size	820 x 1010	µm (maximum)
Thickness	304 ± 10	µm
Bond Pad	70 x 70	µm (minimum)
Bond Pad Composition	99.5 Al, 0.5 Cu	%
Backside	Bare	Not Applicable
Passivation	Nitride	Not Applicable

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Four first

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG841-KGD-CHIPS	-40°C to +125°C	6-Pad Bare Die [CHIP]	C-6-3