EVALUATION KIT AVAILABLE

19-5875; Rev 1; 8/11

MAX2769B

通用型GPS接收机

概述

MAX2769B是下一代单芯片全球导航卫星系统(GNSS)接收机，用于GPS、GLONASS、伽利略以及北斗导航卫星系统。这款单转换GNSS接收机适合高性能工业和汽车应用。

MAX2769B采用Maxim先进的低功耗SiGe BiCMOS工艺，能够以较低的成本提供业界最高的性能和集成度。单芯片内集成了完整的接收链路，包括双输入LNA、混频器、镜频抑制滤波器、PGA、VCO、N分频频率合成器、晶体振荡器和多位ADC。该接收器的总噪声系数低至1.4dB。

MAX2769B集成了单芯片滤波器，无需外部IF滤波器，仅需少量外部元件即可构建完整的低成本GPS RF接收机方案。

MAX2769B是目前设计最为灵活的一款接收机。片内Σ–Δ N分频合成器可以在主机系统所提供的任意参考频率或晶振频率下，以±30Hz (f_{XTAL} = 32MHz)的精度设置IF频率。ADC可以同时为I和Q通道各输出一位或两位量化值的CMOS逻辑电平，或者为I通道输出三位量化值的CMOS逻辑电平。也可以提供I和Q通道的模拟输出。

MAX2769B采用带裸焊盘的5mm x 5mm、28引脚薄型QFN封装。

应用

汽车导航系统

本地使能移动电话

PND (个人导航设备)

远程信息处理(物品跟踪、库存管理)

舰艇/航空导航系统

软件GPS

笔记本电脑和上网本

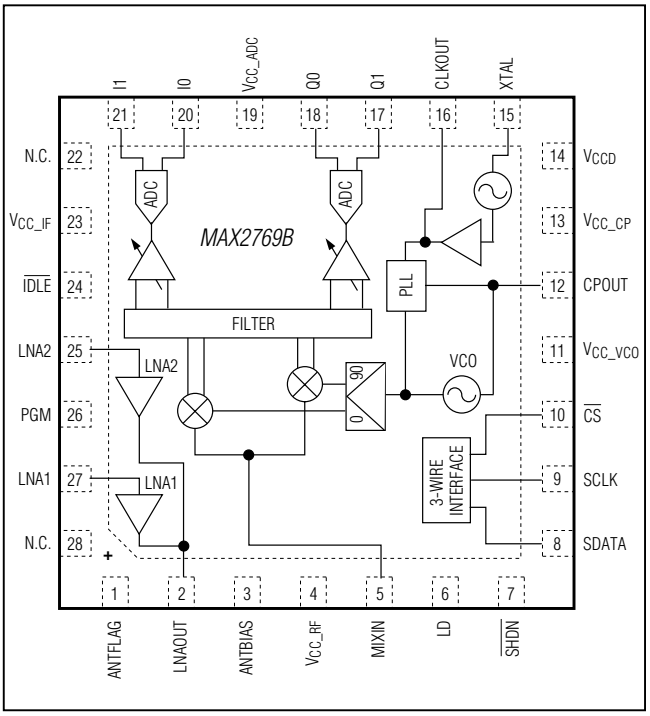
相关型号以及配合该器件使用的推荐产品，请参见：china.maxim-ic.com/MAX2769B.related。

特性

- ♦ 符合AEC–Q100汽车认证
- ♦ GPS/GLONASS/伽利略/北斗系统
- ♦ 40pF输出时钟驱动能力
- ♦ 无需外部IF SAW或分立式滤波器
- ♦ 可编程设置IF频率
- ♦ 集成VCO的N分频频率合成器支持宽范围的参考时钟频率
- ♦ 内部独立的双输入LNA分别用于无源和有源天线输入
- ♦ 总噪声系数1.4dB
- ♦ 内置晶体振荡器
- ♦ 内置有源天线传感器
- ♦ 供电电压为2.7V至3.3V
- ♦ 小尺寸28引脚、符合RoHS标准的薄型QFN无铅封装 (5mm x 5mm)

定购信息在数据资料的最后给出。

原理框图



本文是英文数据资料的译文，文中可能存在翻译上的不准确或错误。如需进一步确认，请在您的设计中参考英文资料。

有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maximintegrated.com。

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to Ground ..... -0.3V to +4.2V
Other Pins Except LNA_, MIXIN, XTAL, and LNAOUT to Ground ..... -0.3V to +(Operating $V_{CC\_}$ + 0.3V)
Maximum RF Input Power ..... +15dBm
Continuous Power Dissipation (T_A = +70°C)
TQFN (derates 27mW/°C above +70°C) 2500mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS*

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7	2.85	3.3	V
Supply Current	Default mode, LNA1 is active (Note 2)	18	27	31	mA
	Default mode, LNA2 is active (Note 2)	15	25	30.5	
	Idle Mode™, $\overline{IDLE}$ = low, $\overline{SHDN}$ = high		5		
	Shutdown mode, $\overline{SHDN}$ = low		200		µA
Voltage Drop at ANTBIAS from V_{CC_RF}	Sourcing 20mA at ANTBIAS		0.2		V
Short-Circuit Protection Current at ANTBIAS	ANTBIAS is shorted to ground		57		mA
Active Antenna Detection Current	To assert logic-high at ANTFLAG		1.1		mA
DIGITAL INPUT AND OUTPUT					
Digital Input Logic-High	Measure at the $\overline{SHDN}$ pin	1.5			V
Digital Input Logic-Low	Measure at the $\overline{SHDN}$ pin			0.4	V

Idle Mode是Maxim Integrated Products, Inc.的商标。

AC ELECTRICAL CHARACTERISTICS*

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CASCADED RF PERFORMANCE					
RF Frequency	L1 band		1575.42		MHz
Noise Figure	LNA1 input active, default mode (Note 3)		1.4		dB
	LNA2 input active, default mode (Note 3)		2.7		
	Measured at the mixer input		10.3		
Out-of-Band 3rd-Order Input Intercept Point	Measured at the mixer input (Note 4)		-7		dBm
In-Band Mixer Input Referred 1dB Compression Point	Measured at the mixer input		-85		dBm
Mixer Input Return Loss			10		dB
Image Rejection			25		dB
Spurs at LNA1 Input	LO leakage		-101		dBm
	Reference harmonics leakage		-103		
Maximum Voltage Gain	Measured from the mixer to the baseband analog output	91	96	103	dB
Variable Gain Range		55	59		dB
FILTER RESPONSE					
Passband Center Frequency	FBW = 00		4		MHz
	FBW = 10		4		
	FBW = 01		9.27		
Passband 3dB Bandwidth	FBW = 00		2.5		MHz
	FBW = 10		4.2		
	FBW = 01		9.66		
Lowpass 3dB Bandwidth	FBW = 11		9		MHz
Stopband Attenuation	3rd-order filter, bandwidth = 2.5MHz, measured at 4MHz offset		30		dB
	5th-order filter, bandwidth = 2.5MHz, measured at 4MHz offset	40	49.5		
LNA					
LNA1 INPUT					
Power Gain			19		dB
Noise Figure			0.83		dB
Input IP3	(Note 5)		-1.1		dBm
Output Return Loss			10		dB
Intput Return Loss			8		dB

AC ELECTRICAL CHARACTERISTICS* (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LNA2 INPUT					
Power Gain			13		dB
Noise Figure			1.14		dB
Input IP3	(Note 5)		1		dBm
Output Return Loss			19		dB
Input Return Loss			11		dB
FREQUENCY SYNTHESIZER					
LO Frequency Range	0.2V < V_{TUNE} < ($V_{CC\_}$ - 0.3V)	1550		1610	MHz
LO Tuning Gain			57		MHz/V
Reference Input Frequency		8		44	MHz
Main Divider Ratio		36		32,767	—
Reference Divider Ratio		1		1023	—
Charge-Pump Current	ICP = 0		0.5		mA
	ICP = 1		1		
TCXO INPUT BUFFER/OUTPUT CLOCK BUFFER					
Frequency Range		8		32	MHz
Output Logic-Level High (V_{OH})	With respect to ground, I_{OH} = 10µA (DC-coupled)	2			V
Output Logic-Level Low (V_{OL})	With respect to ground, I_{OL} = 10µA (DC-coupled)			0.8	V
Capacitive Slew Current	Load = 10kΩ + 40pF, f_{CLKOUT} = 32MHz		11		mA
Output Load			10||40		kΩ||pF
Reference Input Level	Sine wave	0.5			V_{P-P}
Clock Output Multiply/Divide Range	/4, /2, /1 (x2, max input frequency of 16MHz)	÷4		x2	—
ADC					
ADC Differential Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB
ADC Integral Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB

Note 1: MAX2769B is production tested at T_A = +25°C and +85°C. All min/max specifications are guaranteed by design and characterization from -40°C to +85°C, unless otherwise noted. Default register settings are not production tested or guaranteed. User must program the registers upon power-up.

Note 2: Default, low-NF mode of the IC. LNA choice is gated by the ANT_FLAG signal. In the normal mode of operation without an active antenna, LNA1 is active. If an active antenna is connected and ANT_FLAG switches to 1, LNA1 is automatically disabled and LNA2 becomes active. PLL is in an integer-N mode with f_{COMP} = f_{TCXO}/16 = 1.023MHz and ICP = 0.5mA. The complex IF filter is configured as a 5th-order Butterworth filter with a center frequency of 4MHz and bandwidth of 2.5MHz. Output data is in a 2-bit sign/magnitude format at CMOS logic levels in the I channel only.

Note 3: The LNA output connects to the mixer input without a SAW filter between them.

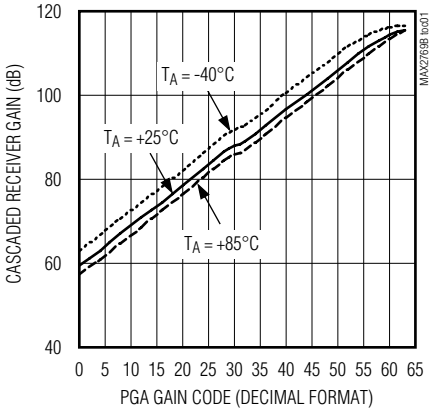
Note 4: Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm/tone. Passive pole at the mixer output is programmed to be 13MHz.

Note 5: Measured from the LNA input to the LNA output. Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm per tone.

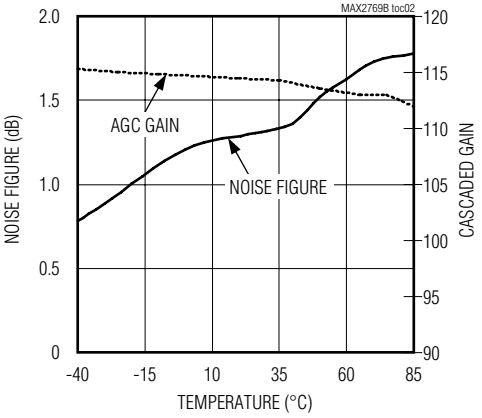
典型工作特性

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

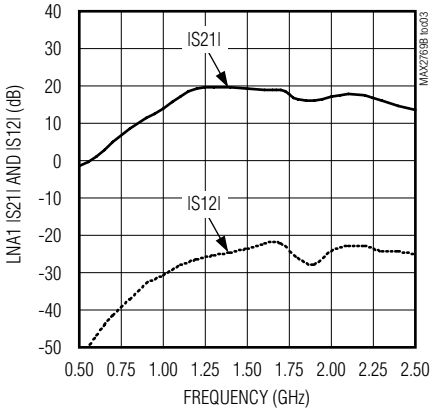
CASCADED RECEIVER GAIN vs. PGA GAIN CODE



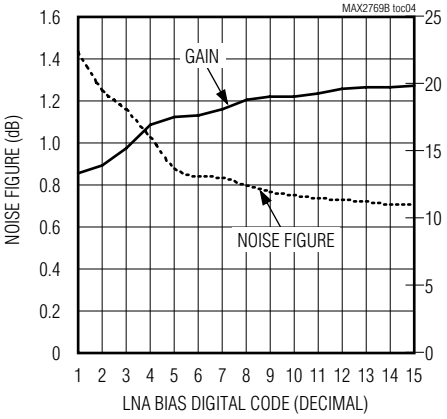
CASCADED GAIN AND NOISE FIGURE vs. TEMPERATURE



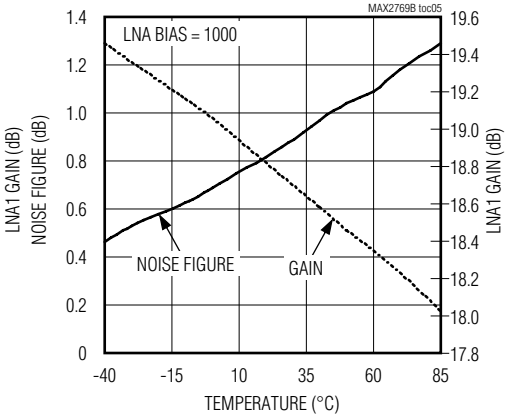
LNA1 |S21| AND |S12| vs. FREQUENCY



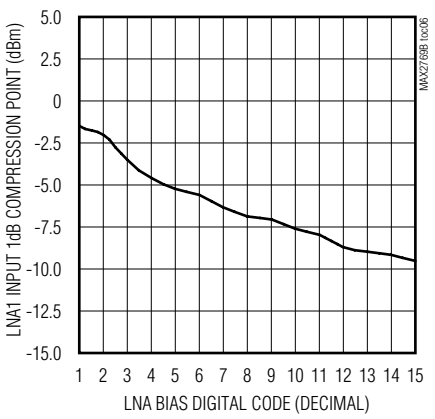
LNA1 GAIN AND NOISE FIGURE vs. LNA1 BIAS DIGITAL CODE



LNA1 GAIN AND NOISE FIGURE vs. TEMPERATURE



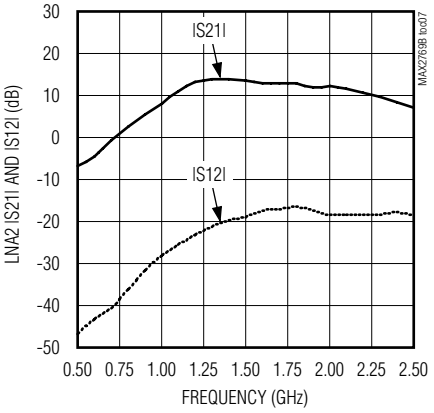
LNA1 INPUT 1dB COMPRESSION POINT vs. LNA1 BIAS DIGITAL CODE



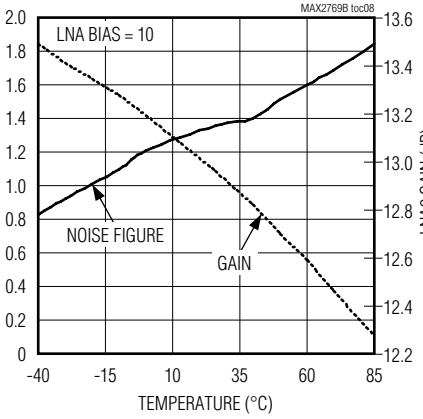
典型工作特性(续)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

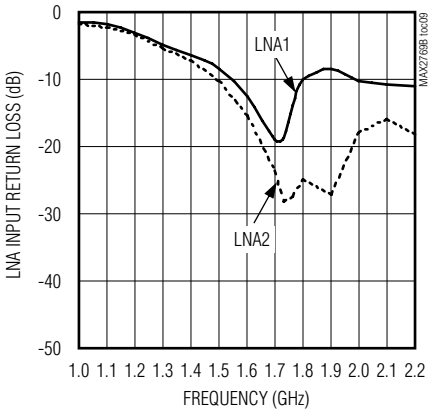
LNA2 IS21I AND IS12I vs. FREQUENCY



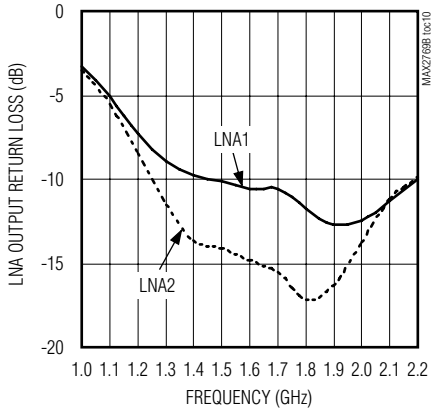
LNA2 GAIN AND NOISE FIGURE vs. TEMPERATURE



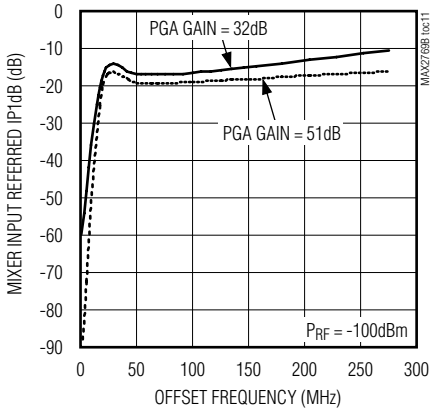
LNA INPUT RETURN LOSS vs. FREQUENCY



LNA OUTPUT RETURN LOSS vs. FREQUENCY



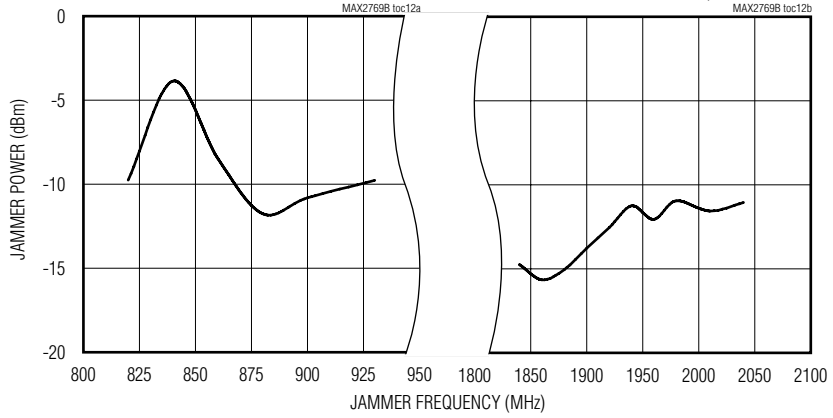
MIXER INPUT REFERRED IP1dB vs. OFFSET FREQUENCY



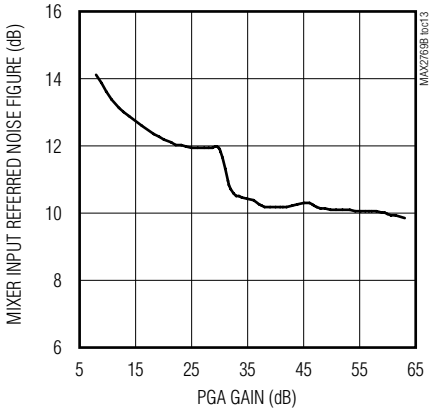
典型工作特性(续)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

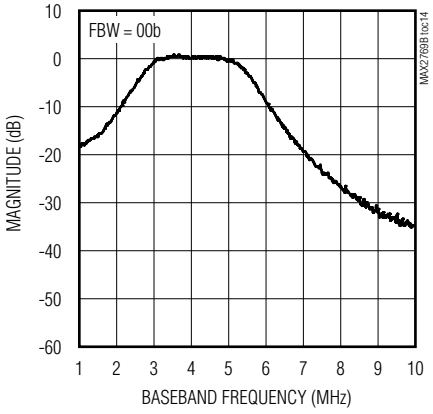
1dB CASCADED NOISE FIGURE DESENSITIZATION vs. JAMMER FREQUENCY



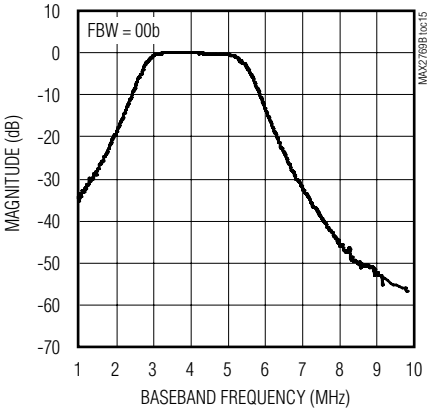
MIXER INPUT REFERRED NOISE FIGURE vs. PGA GAIN



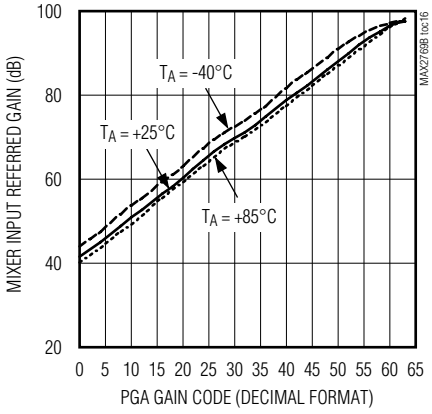
3RD-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



5TH-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



MIXER INPUT REFERRED GAIN vs. PGA GAIN CODE



典型工作特性(续)

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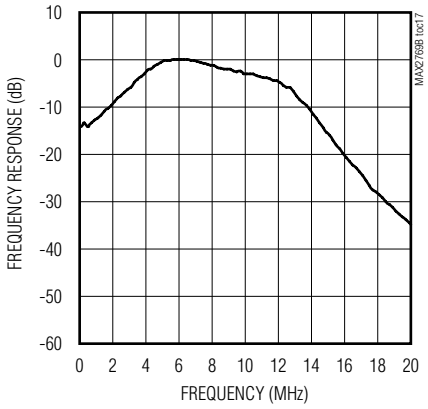
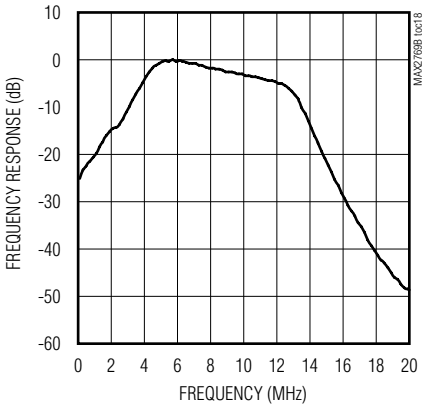
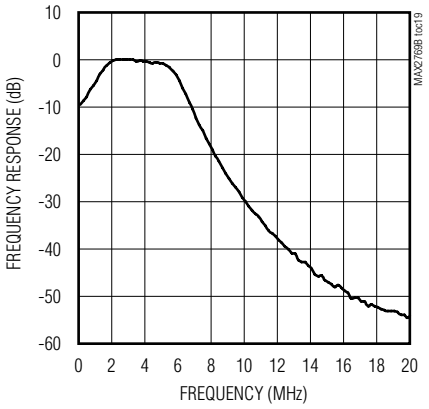
3RD-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 01)



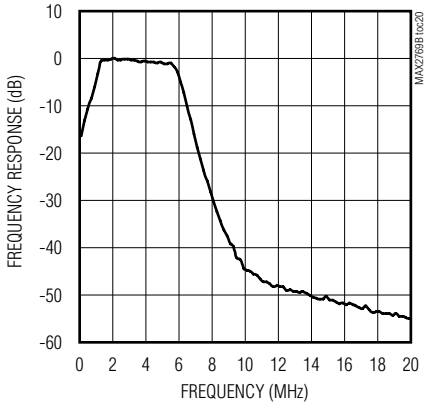
5TH-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 01)



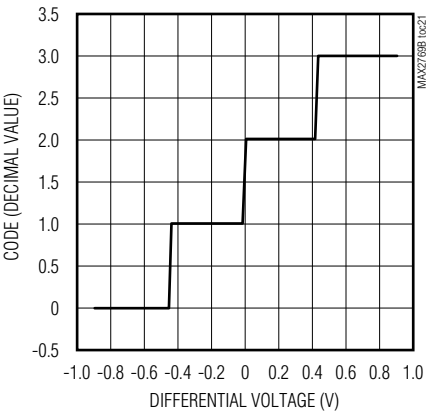
3RD-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 10)



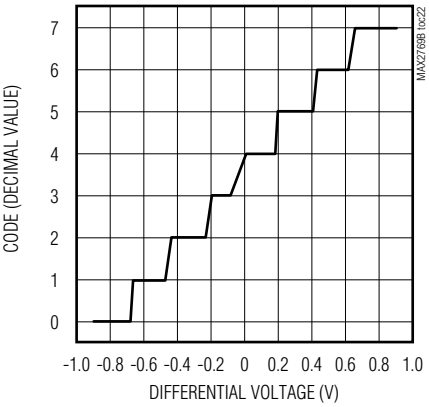
5TH-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 10)



2-BIT ADC TRANSFER CURVE



3-BIT ADC TRANSFER CURVE



典型工作特性(续)

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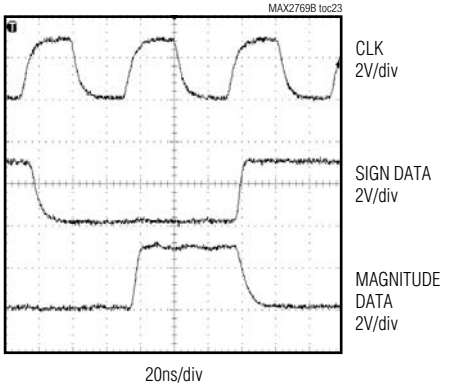
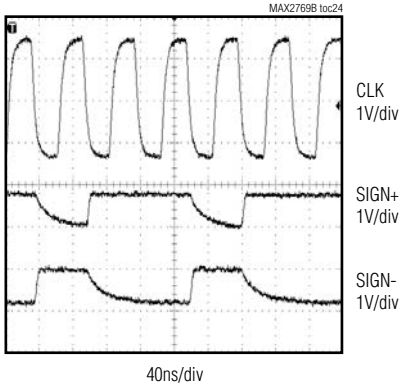
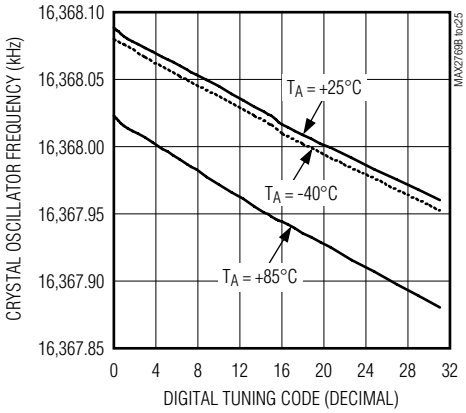
DIGITAL OUTPUT CMOS LOGIC



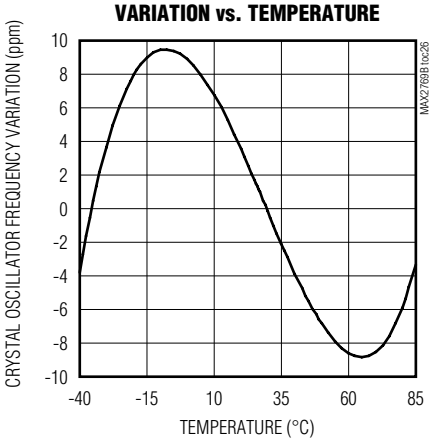
DIGITAL OUTPUT DIFFERENTIAL LOGIC



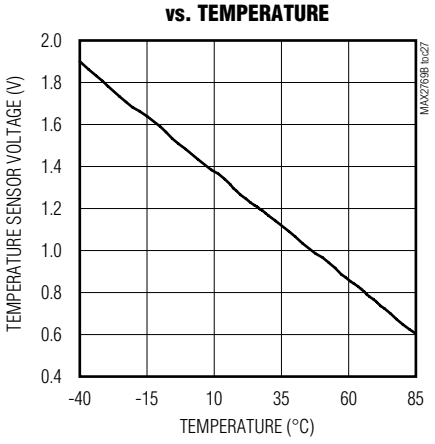
CRYSTAL OSCILLATOR FREQUENCY vs. DIGITAL TUNING CODE



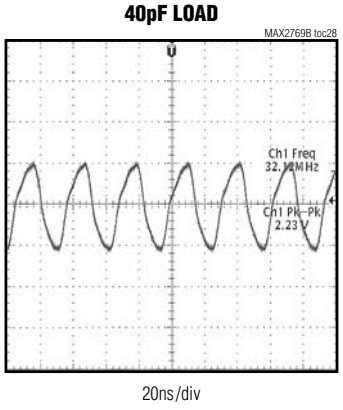
CRYSTAL OSCILLATOR FREQUENCY VARIATION vs. TEMPERATURE



TEMPERATURE SENSOR VOLTAGE vs. TEMPERATURE



CLOCK OUTPUT DRIVER WITH 40pF LOAD



典型应用电路

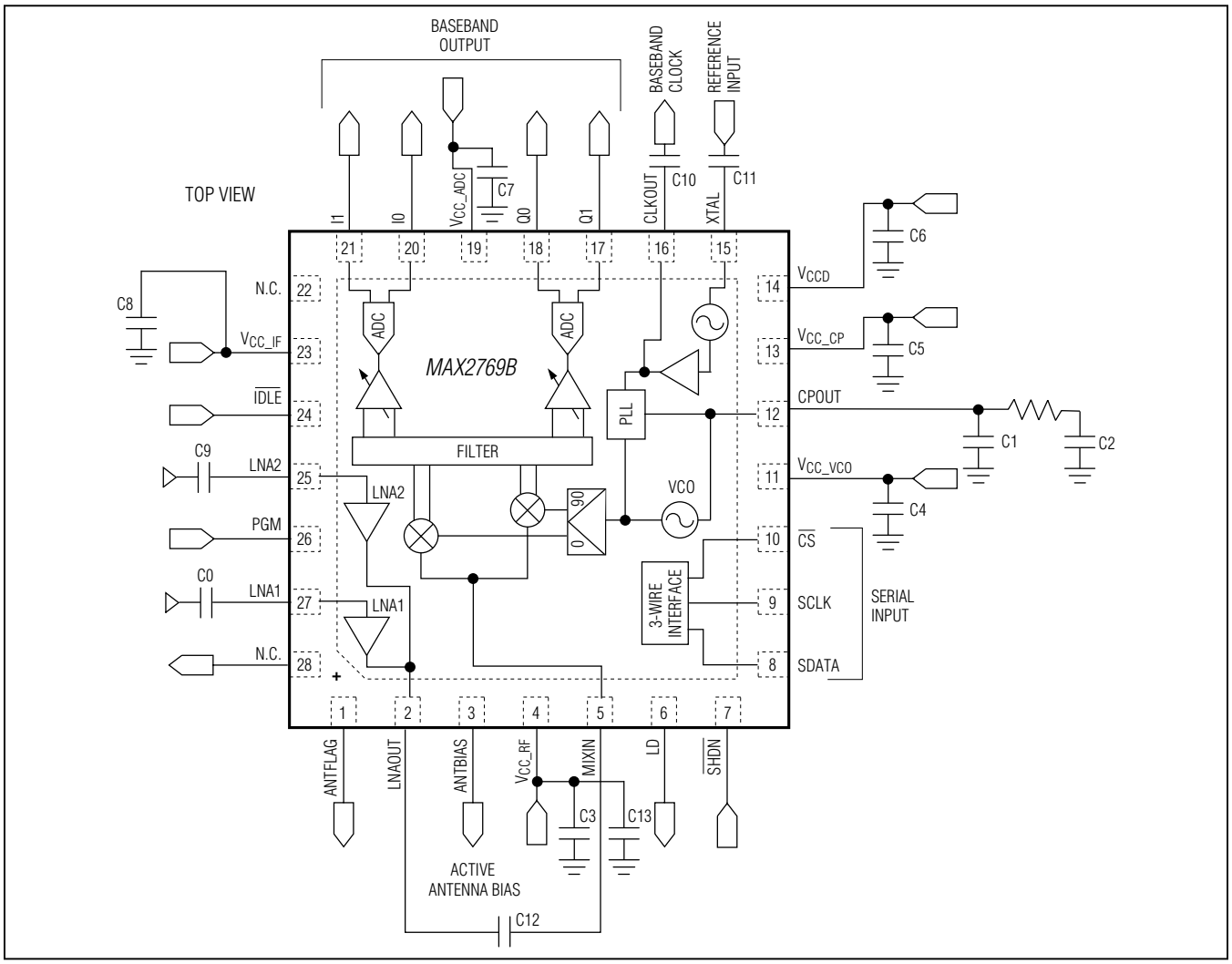
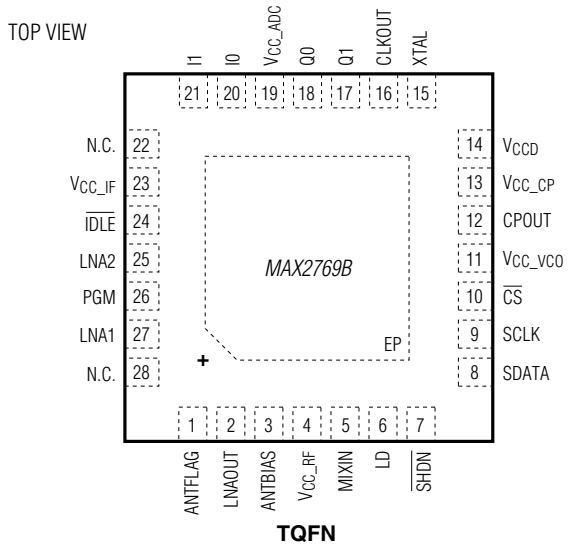


表1. 元件列表

DESIGNATION	QUANTITY	DESCRIPTION
C0, C9	2	0.47nF AC-coupling capacitors
C1	1	27pF PLL loop filter capacitor
C2	1	0.47nF PLL loop filter capacitor
C3–C8	6	0.1µF supply voltage bypass capacitor
C10, C11	2	10nF AC-coupling capacitor
C12	1	0.47nF AC-coupling capacitor
C13	1	0.1nF supply voltage bypass capacitor
R1	1	20kΩ PLL loop filter resistor

引脚配置



引脚说明

引脚	名称	功能
1	ANTFLAG	有源天线标识逻辑输出，逻辑高电平表示有源天线连接至ANTBIAS引脚。
2	LNAOUT	LNA输出，LNA输出内部匹配至50Ω。
3	ANTBIAS	带缓冲的电源电压输出，为外部有源天线提供偏压。
4	V_{CC_RF}	RF电路供电电源，利用并联的100nF和100pF电容将其旁路至地，电容尽量靠近引脚放置。
5	MIXIN	混频器输入，混频器输入内部匹配至50Ω。
6	LD	锁存检测器CMOS逻辑输出，逻辑高电平表示PLL已锁定。
7	$\overline{SHDN}$	工作状态控制逻辑输入，逻辑低电平关断整个器件。
8	SDATA	3线串口数字输入。
9	SCLK	3线串口时钟输入，$\overline{CS}$为低电平时有效。数据在SCLK的上升沿移入。

引脚说明(续)

引脚	名称	功能
10	$\overline{CS}$	3线串口的片选逻辑输入，$\overline{CS}$为低电平时，允许串行数据移入；完成加载操作时，将$\overline{CS}$置为高电平。
11	V_{CC_VCO}	VCO电源电压，利用100nF电容将其旁路至地，电容尽量靠近引脚放置。
12	CPOUT	电荷泵输出，在该端口并联一个电容C和R、C串联网络，作为PLL环路滤波器(参见*典型应用电路*)。
13	V_{CC_CP}	PLL电荷泵供电电源，利用100nF电容将其旁路至地，电容尽量靠近引脚放置。
14	V_{CCD}	数字电路供电电源，利用100nF电容将其旁路至地，电容尽量靠近引脚放置。
15	XTAL	XTAL或参考时钟振荡器输入。时钟连接至XTAL，如果使用TCXO，则通过隔直电容连接。
16	CLKOUT	参考时钟输出。
17	Q1	Q通道电压输出，Q通道ADC输出的第0位和第1位或模拟差分电压输出。
18	Q0	
19	V_{CC_ADC}	ADC供电电源，利用100nF电容将其旁路至地，电容尽量靠近引脚放置。
20	I0	I通道电压输出，I通道ADC输出的第0位和第1位或模拟差分电压输出。
21	I1	
22	N.C.	不连接，保持该引脚浮空。
23	V_{CC_IF}	IF电路供电电源，利用100nF电容将其旁路至地，电容尽量靠近引脚放置。
24	$\overline{IDLE}$	工作状态控制逻辑输入，逻辑低电平将使器件进入空闲模式，此时XTAL振荡器仍保持有效工作，其它所有电路关闭。
25	LNA2	LNA输入端口2，该端口通常用于有源天线，内部匹配至50Ω。
26	PGM	逻辑控制输入，接地时启用串行接口；置为逻辑高电平时，则根据表3，将SDATA、$\overline{CS}$和SCLK连接至电源或地，提供8种器件状态的硬件编码设置。
27	LNA1	LNA输入端口1，该端口通常用于无源天线，内部匹配至50Ω (参见*典型应用电路*)。
28	N.C.	不连接，保持该引脚开路。
—	EP	裸焊盘，以超低电感引线接地，在PCB接地区域布置多个过孔。

详细说明

集成有源天线检测器

MAX2769B包括一个低压差开关，为外部有源天线提供偏压。为了使能天线开关输出，将配置寄存器1中的ANTEN设置为逻辑1，这将闭合开关，使天线偏压引脚连接至V_{CC_RF}，以获得低压差(20mA负载电流下压差为200mV)偏置。ANTEN为逻辑低电平时，关闭天线偏压。有源天线电路具有短路保护，防止输出短路至地。

低噪声放大器(LNA)

MAX2769B集成两个低噪声放大器，LNA1通常用于接收无源天线信号，该LNA需要交流耦合电容。默认状态下，偏置电流设置为4mA，典型噪声系数和IIP3分别为0.8dB和-1.1dBm左右。LNA2通常用于接收有源天线信号，LNA2内部匹配至50Ω，需要隔直流电容。配置寄存器1中的LNAMODE位用于控制两个LNA的工作模式，关于LNA工作模式的设置，请参见表6和表7。

混频器

MAX2769B内部集成了正交混频器，以输出低中频或零中频I、Q信号。正交混频器内部匹配至50Ω，需要低边LO注入。LNA的输出和混频器的输入均提供片外引脚，以方便连接SAW滤波器。

可编程增益放大器(PGA)

MAX2769B集成基带可编程增益放大器，其增益控制范围为59dB。利用串行接口，通过设置配置寄存器3中的GAININ位，设置PGA增益。将配置寄存器2中的第12、11位(AGCMODE)设置为10，可由3线接口直接控制PGA增益。

自动增益控制(AGC)

MAX2769B内部提供了一个控制环路，自动设置PGA增益，为ADC转换提供最佳输入功率，从而在其输出端建立所需要的幅值位密度。该算法对512个ADC时钟周期内的幅值位进行计数，然后将幅值位数与控制字(GAINREF)提供的基准进行比较。相应的幅值位密度表示为GAINREF的十进制数除以计数器长度512。例如，为实现33%幅值位密度(针对2位转换器优化)，将GAINREF设置为170，于是170/512 = 33%。

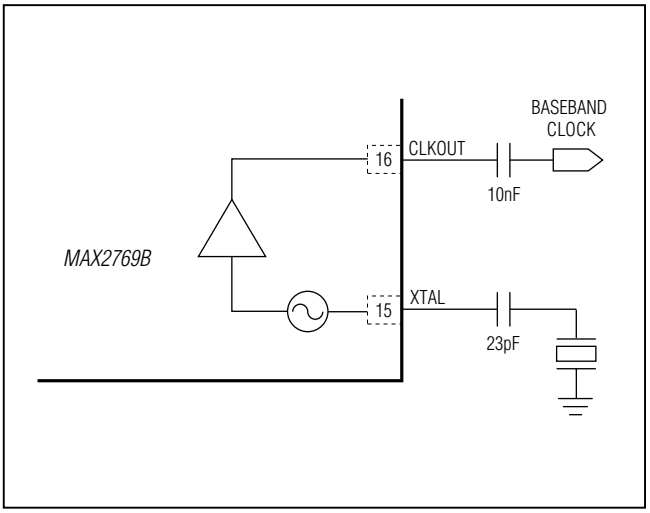


图1. MAX2769B评估板中的晶体振荡器示意图

基带滤波器

接收机的基带滤波器可设置为低通滤波器或带通滤波器。低通滤波器有两种配置，一种是将配置寄存器1中的F3OR5位置1，配置为3阶巴特沃斯滤波器，以减小群时延；或者是将F3OR5位置0，配置为5阶巴特沃斯滤波器，以获得更陡峭的带外抑制。双边带3dB带宽可选择为2.5MHz、4.2MHz、9.66MHz，也可通过配置寄存器1的FBW位进行选择。将配置寄存器1中的FCENX位更改为1，启用合成滤波器，将低通滤波器更换成带通滤波器，中心频率可由配置寄存器1中的FCEN和FCENMSB位设置。

表2. 输出数据格式

INTEGER VALUE	SIGN/MAGNITUDE			UNSIGNED BINARY			TWO'S COMPLEMENT BINARY		
	1b	2b	3b	1b	2b	3b	1b	2b	3b
7	0	01	011	1	11	111	0	01	011
5	0	01	010	1	11	110	0	01	010
3	0	00	001	1	10	101	0	00	001
1	0	00	000	1	10	110	0	00	000
-1	1	10	100	0	01	011	1	11	111
-3	1	10	101	0	01	010	1	11	110
-5	1	11	110	0	00	001	1	10	101
-7	1	11	111	0	00	000	1	10	100

合成器

MAX2769B集成20位Σ–Δ N分频合成器，允许器件调谐至所需要的VCO频率，精度约为±30Hz。合成器包括一个10位参考时钟分频器，分频比可在1至1023范围内设置；一个15位整数主分频器，分频比可在36至32767范围内设置；另外，还包括一个20位小数主分频器。参考时钟分频器可由PLL整数分频比寄存器中的RDIV位设置(见表11)，支持8MHz至32MHz的参考时钟频率。需要设置参考时钟分频比，使比较频率介于0.05MHz至32MHz之间。

PLL环路滤波器是合成器唯一的外部电路，典型的PLL滤波器为C–R–C网络，位于电荷泵输出端。电荷泵输出可吸入、源出的电流默认值为0.5mA，LO调谐增益为57MHz/V。*典型应用电路*给出了一个示例，推荐的环路滤波器元件为f_{COMP} = 1.023MHz，环路带宽 = 50kHz。

LO频率(f_{LO})除以f_{COMP}，可计算得到相应的整数和小数分频比。TCXO频率(f_{TCXO})除以参考时钟分频比(RDIV)，得到f_{COMP}。例如，设TCXO频率为20MHz，RDIV为1，标称LO频率为1575.42MHz，则可利用下式计算支持不同参考时钟和比较频率的分频比：

$$比较频率 = \frac{f_{TCXO}}{RDIV} = \frac{20MHz}{1} = 20MHz$$

$$LO频率分频比 = \frac{f_{LO}}{f_{COMP}} = \frac{1575.42MHz}{20MHz} = 78.771$$

整数分频比 = 78(d) = 000 000 0100 1110 (二进制)

小数分频比 = 0.771 x 220 = 808452 (十进制) = 1100 0101 0110 0000 0100

小数模式下，合成器工作不应采用大于251的整数分频比。

晶振

MAX2769B包括片上晶体振荡器。使用晶振时，需要外部并联模式晶体。建议通过交流耦合电容连接晶体与XTAL引脚，以优化相应的负载电容，并将晶振频率控制在中心频率。优化负载电容时，应考虑PCB走线的寄生损耗。例如，MAX2769B评估板采用16.368MHz晶体，设计用于12pF负载电容。利用23pF串联电容将晶振频率控制在中心位置，参见图1。此外，可利用5位串口数据，即PLL配置寄存器中的XTALCAP，调整晶振频率，调节范围取决于电容变化所能牵引晶体频率的程度。MAX2769B评估板使用的晶振频率调整范围约为200Hz。

MAX2769B提供参考时钟输出，通过设置PLL配置寄存器中的REFDIV位，时钟频率可调节至晶振频率、振荡器频率的四分之一、振荡器频率的一半(f_{XTAL} ≤ 16MHz)或振荡器频率的两倍。

ADC

MAX2769B具有片上ADC，对下变频GPS信号进行数字转换。ADC最大采样率约为50Msps，默认状态下，采样输出为2位格式(1位幅值和1位符号)，可配置为通过I、Q通道输出1位或2位数据，或只通过I通道输出1位、2位或3位数据。ADC支持三种不同格式的数字输出：无符号二进制、符号与幅值、或二进制补码，通过设置配置寄存器2中的FORMAT位实现。对于I或Q通道，I1或Q1引脚输出MSB位，I0或Q0引脚输出LSB位。3位情况下，仅可在I通道中选择输出数据格式，I1输出MSB，I0为第2位，而Q1为LSB。

图2所示为2位和3位情况下的ADC量化电平，说明了符号/幅度数据的映射关系。变量T = 1表示2位情况下的幅度门限位置。

ADC小数时钟分频器

12位小数时钟分频器位于ADC前面的时钟通路，可用于生成ADC时钟，该时钟为输入参考时钟的一部分。小数分频器模式下，瞬态分频比在整数分频比之间交替切换，以获得所需要的小数分频。例如，如果小数输出时钟比输入时钟频率降低4.5倍，则通过等效的一系列4分频和5分频交替周期，得到平均分频比4.5。小数分频比由下式给出：

$$f_{OUT}/f_{IN} = L_{COUNT}/(4096 - M_{COUNT} + L_{COUNT})$$

式中，L_{COUNT}和M_{COUNT}是通过串口设置的12位计数器值。

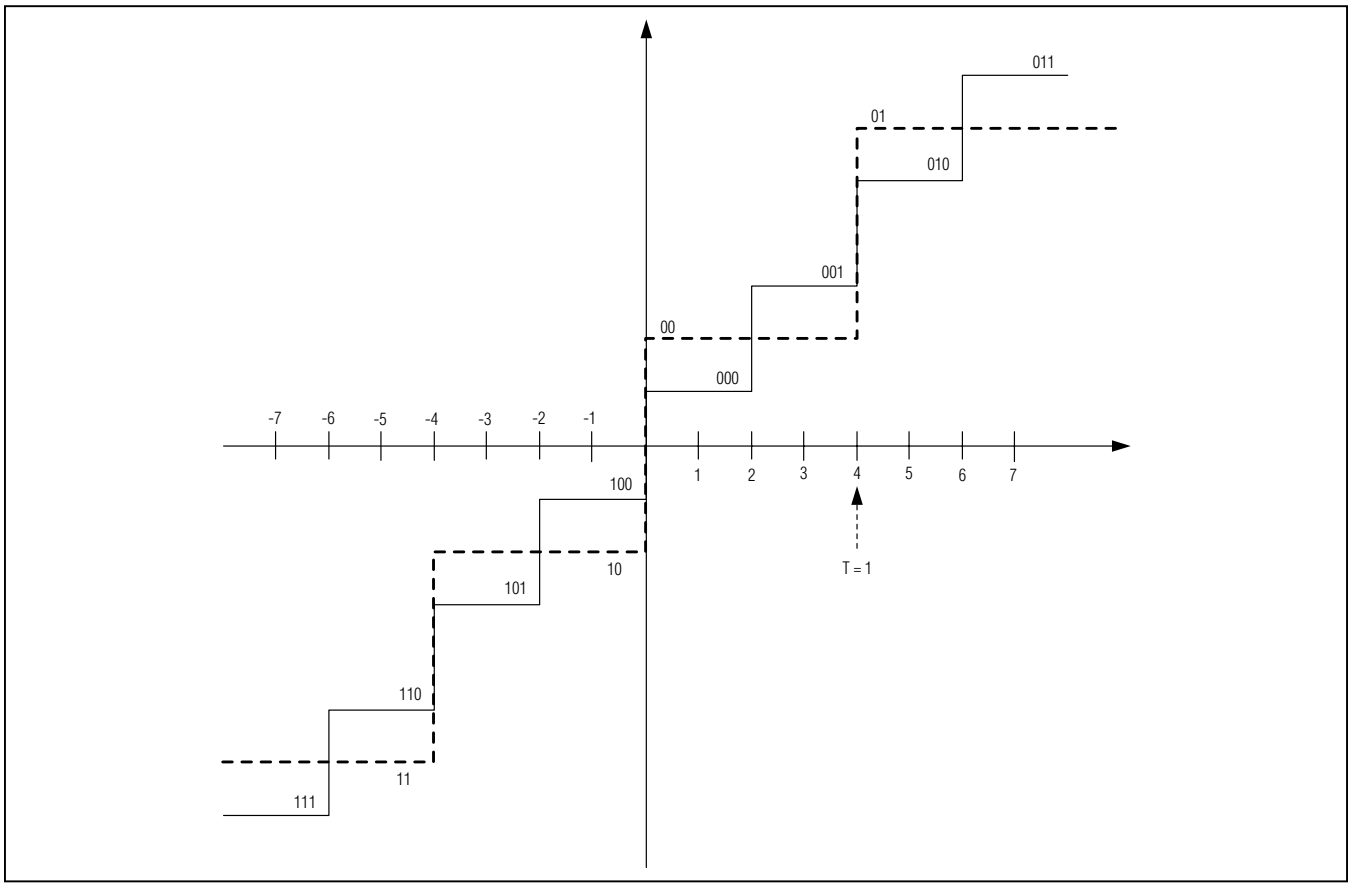


图2. 2位和3位情况下的ADC量化电平

DSP接口

ADC输出的GPS数据为四个逻辑信号(bit_0、bit_1、bit_2和bit_3)，分别表示I (bit_0和bit_1)和Q (bit_2和bit_3)通道的符号/幅值、无符号二进制数或二进制补码数据。ADC的分辨率可设置为最高3位/通道。例如，符号/幅值格式的2位I和Q数据的映射如下：$bit_0 = I_{SIGN}$、$bit_1 = I_{MAG}$、$bit_2 = Q_{SIGN}$和$bit_3 = Q_{MAG}$。数据可以按16位段串行输出，按照bit_0、bit_1、bit_2和bit_3的顺序。串行输出的位数由配置寄存器3中的STRMBITS位控制，可选择bit_0；bit_0和bit_1；bit_0和bit_2；以及bit_0、bit_1、bit_2和bit_3。如果仅串行输出bit_0，则数据流仅包含bit_0数据。如果选择串行输出bit_0和bit_1 (或bit_2)，数据流包括16位的bit_0数据，随后是16位的bit_1 (或bit_2)数据，其后为16位的bit_0数据，以此类推。在这种情况下，串行时钟必须至少为ADC时钟的两倍。如果选择bit_0、bit_1、bit_2和bit_3 4位串行输出，则串行时钟必须至少比ADC时钟快四倍。

ADC数据并行载入四个ADC输出对应的保持寄存器。保持寄存器为16位长，由ADC时钟控制。16位ADC周期结束时，将数据传送至四个移位寄存器，在下一个16位ADC周期串行移至输出。移位寄存器由串行时钟控制，串行时钟必须选得足够快，在从ADC装载下一组数据之前将全部数据移出。输出所有有效的ADC数据码流后，数据后面跟随全零码型。DATASYNC信号用于表示每个有效16位数据码片的开始。此外，每128至16,384个ADC时钟周期输出一个TIME_SYNC信号。

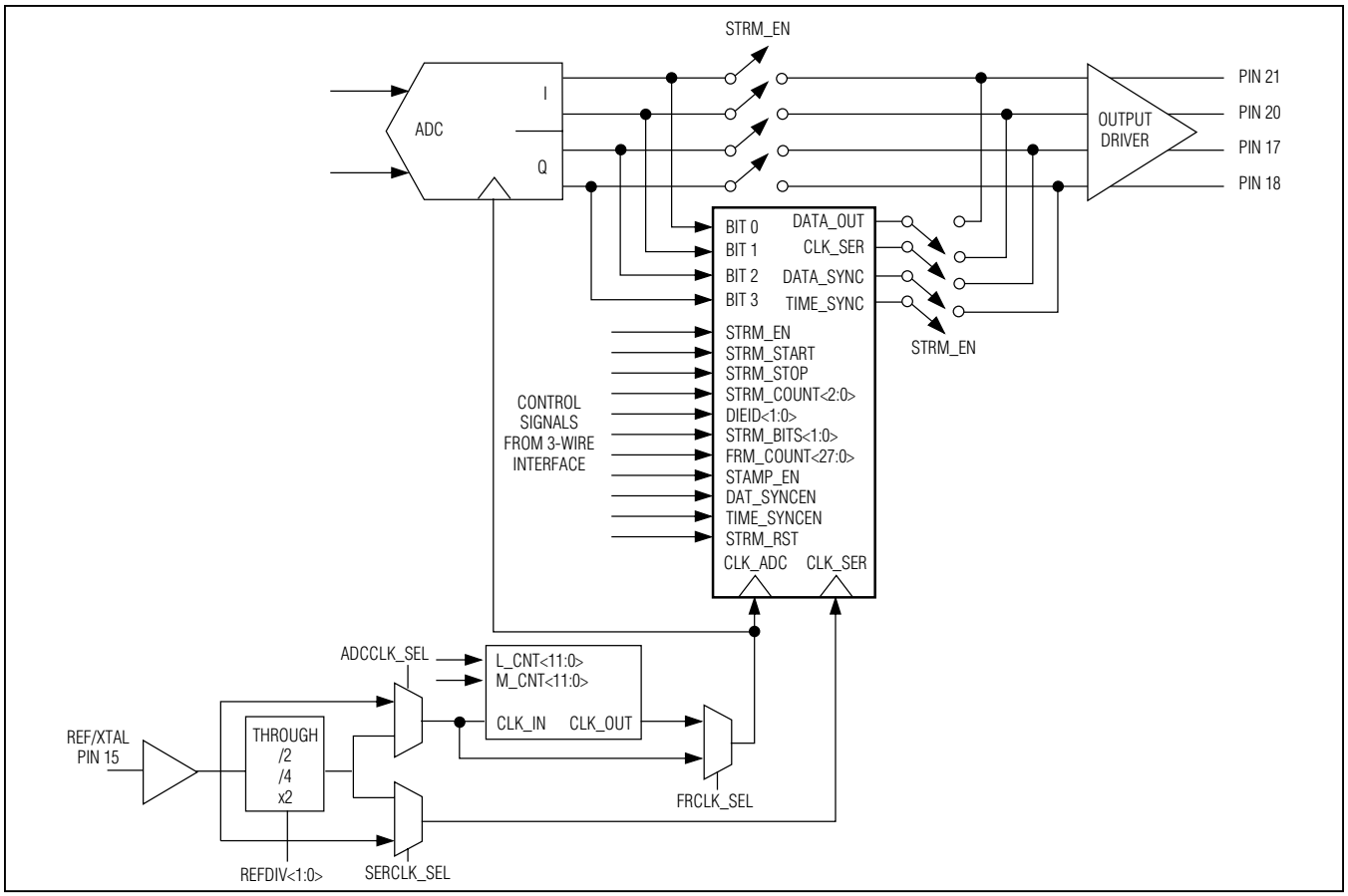


图3. DSP接口顶层连接和控制信号

预置器件状态

如果系统没有可供使用的串口，器件可工作在预置状态，不需要通过串口配置。将PGM引脚连接至逻辑高电平，将SCLK、SDATA和$\overline{CS}$引脚连接至逻辑高或低电平，根据表3设置器件的预置状态。

上电复位(POR)

MAX2769B具有上电复位电路，确保上电时装载寄存器设置。为确保工作正确，$V_{CC_}$达到其稳压标称值的90%之前，不能触发PGM上升沿；详细信息参见图4。

串行接口、地址和位分配

串行接口用于设置MAX2769B，以配置不同的工作模式。

串行接口由三个信号控制：SCLK（串行时钟）、$\overline{CS}$（片选）和SDATA（串行数据）。基带控制器通过串行接口控制PLL、AGC、测试和模块选择。片选信号置为低电平时，32位数据移位至串行移位寄存器，MSB（D27)在前，图5和表4所示为接口信号的时序，以及设置和保持时间要求的典型值。

表3. 预置器件状态

DEVICE STATE	DEVICE ELECTRICAL CHARACTERISTICS									3-WIRE CONTROL PINS		
	REFERENCE FREQUENCY (MHz)	REFERENCE DIVISION RATIO	MAIN DIVISION RATIO	I AND Q OR I ONLY	NUMBER OF IQ BITS	I AND Q LOGIC LEVEL	IF CENTER FREQUENCY (MHz)	IF FILTER BW (MHz)	IF FILTER ORDER	SCLK	DATA	$\overline{CS}$
0	16.368	16	1536	I	1	Differential	4.092	2.5	5th	0	0	0
1	16.368	16	1536	I	1	Differential	4.092	2.5	3rd	0	0	1
2	16.368	16	1536	I	2	CMOS	4.092	2.5	5th	0	1	0
3	32.736	32	1536	I	2	CMOS	4.092	2.5	5th	0	1	1
4	19.2	96	7857	I	2	CMOS	4.092	2.5	5th	1	0	0
5	27.456	26	1488	I	3	CMOS	4.092	4.2	5th	1	0	1
6	16.368	16	1536	I	3	CMOS	4.092	4.2	5th	1	1	0
7	27.456	26	1508	I	3	CMOS	9.27075	9.66	5th	1	1	1

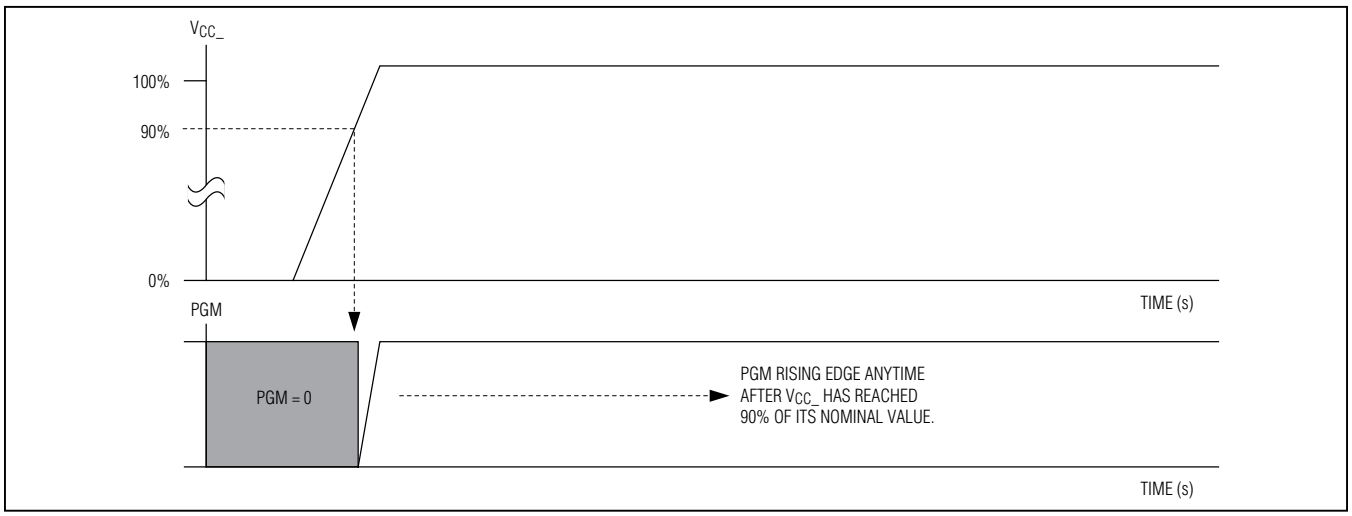


图4. $V_{CC_}$上电复位

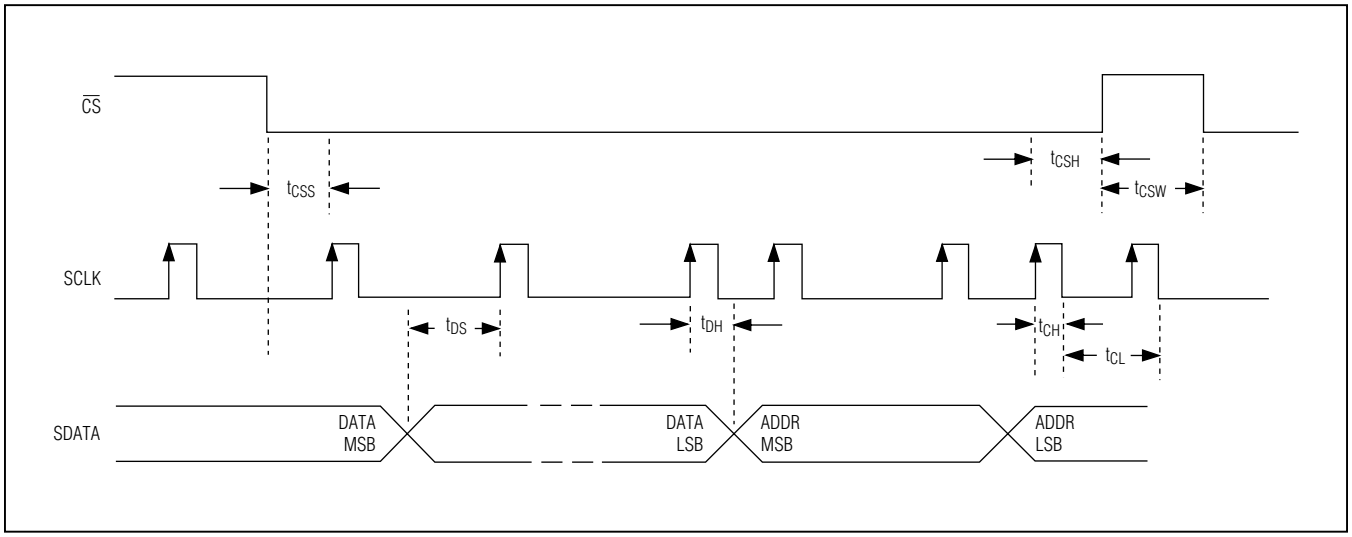


图5. 3线接口时序

表4. 串行接口时序要求

SYMBOL	PARAMETER	TYP VALUE	UNITS
t_{CSS}	Falling edge of $\overline{CS}$ to rising edge of the first SCLK time.	10	ns
t_{DS}	Data to serial-clock setup time.	10	ns
t_{DH}	Data to clock hold time.	10	ns
t_{CH}	Serial clock pulse-width high.	25	ns
t_{CL}	Clock pulse-width low.	25	ns
t_{CSH}	Last SCLK rising edge to rising edge of $\overline{CS}$.	10	ns
t_{CSW}	$\overline{CS}$ high pulse width.	1	clock

表5. 默认寄存器设置汇总

REGISTER NAME	ADDRESS (A3:A0)	DATA
CONF1	0000	Configures RX and IF sections, bias settings for individual blocks.
CONF2	0001	Configures AGC and output sections.
CONF3	0010	Configures support and test functions for IF filter and AGC.
PLLCONF	0011	PLL, VCO, and CLK settings.
DIV	0100	PLL main and reference division ratios, other controls.
FDIV	0101	PLL fractional division ratio, other controls.
STRM	0110	DSP interface number of frames to stream.
CLK	0111	Fractional clock-divider values.
TEST1	1000	Reserved for test mode.
TEST2	1001	Reserved for test mode.

表6. 默认寄存器设置

REGISTER NAME	ADDRESS (A3:A0)	POWER-ON RESET, PGM = 0 (hex)	PRECONFIGURED DEVICE STATE, PGM = 1 (hex)							
			0	1	2	3	4	5	6	7
CONF1	0000	A2919A3	A2919A3	A2919A3	A2919A7	A2919A3	A2919A3	A293573	A293573	A29B26B
CONF2	0001	055028C	055121C	055028C	055121C	055028C	055028C	855030C	855030C	855030C
CONF3	0010	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC
PLLCONF	0011	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008
DIV	0100	0C00080	0C00080	0C00080	0C00080	0C00100	3D62300	0BA00D0	0C00080	0BC80D0
FDIV	0101	8000070	8000070	8000070	8000070	8000070	8000070	8000070	8000070	8000070
STRM	0110	8000000	8000000	8000000	8000000	8000000	8000000	8000000	8000000	8000000
CLK	0111	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2
TEST1	1000	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401
TEST2	1001	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	7CC0403

寄存器详细定义

表7. 配置1 (地址：0000)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
CHIPEN	27	1	Chip enable. Set 1 to enable the device and 0 to disable the entire device except the serial bus.
IDLE	26	0	Idle enable. Set 1 to put the chip in the idle mode and 0 for operating mode.
RESERVED	25:22	1000	—
RESERVED	21:20	10	—
RESERVED	19:18	10	—
RESERVED	17:16	01	—
MIXPOLE	15	0	Mixer pole selection. Set 1 to program the passive filter pole at mixer output at 36MHz, or set 0 to program the pole at 13MHz.
LNAMODE	14:13	00	LNA mode selection, D14:D13 = 00: LNA selection gated by the antenna bias circuit, 01: LNA2 is active; 10: LNA1 is active; 11: both LNA1 and LNA2 are off.
MIXEN	12	1	Mixer enable. Set 1 to enable the mixer and 0 to shut down the mixer.
ANTEN	11	1	Antenna bias enable. Set 1 to enable the antenna bias and 0 to shut down the antenna bias.
FCEN	10:5	001101	IF center frequency programming. Default for f_{CENTER} = 3.092MHz, BW = 2.5MHz. The MSB of FCEN is located in Register Test Mode 2 (Table 16). 001101 = 3.092MHz, 001011 = 4.092MHz, 010011 = 10.0MHz
FBW	4:3	00	IF filter center bandwidth selection. D4:D3 = 00: 2.5MHz; 10: 4.2MHz; 01: 9.66MHz; 11: Reserved.
F3OR5	2	0	Filter order selection. Set 0 to select the 5th-order Butterworth filter. Set 1 to select the 3rd-order Butterworth filter.
FCENX	1	1	Polyphase filter selection. Set 1 to select complex bandpass filter mode. Set 0 to select lowpass filter mode.
FGAIN	0	1	IF filter gain setting. Set 0 to reduce the filter gain by 6dB.

表8. 配置2 (地址：0001)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
IQEN	27	0	I and Q channels enable. Set 1 to enable both I and Q channels and 0 to enable I channel only.
GAINREF	26:15	170d	AGC gain reference value expressed by the number of MSB counts (magnitude bit density). 10101010 = 234 magnitude bit density reference, 1010100 = 84 magnitude bit density reference, 100111010 = 314 magnitude bit density reference.
RESERVED	14:13	00	Reserved.
AGCMODE	12:11	00	AGC mode control. Set D12:D11 = 00: independent I and Q; 01: reserved; 10: gain is set directly from the serial interface by GAININ; 11: reserved.
FORMAT	10:9	01	Output data format. Set D10:D9 = 00: unsigned binary; 01: sign and magnitude; 1X: two's complement binary.
BITS	8:6	010	Number of bits in the ADC. Set D8:D6 = 000: 1 bit, 001: reserved; 010: 2 bits; 011: reserved, 100: 3 bits.
DRVCFG	5:4	00	Output driver configuration. Set D5:D4 = 00: CMOS logic, 01: reserved; 1X: analog outputs.
RESERVED	3	1	—
RESERVED	2	0	—
DIEID	1:0	00	Identifies a version of the IC.

表9. 配置3 (地址：0010)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
GAININ	27:22	111010	PGA gain value programming from the serial interface in steps of dB per LSB. 000000 = PGA gain set to 0dB, 101011 = 42dB, 101100 = 43dB, 101110 = 45dB, 111010 = 57dB, 111111 = 62dB.
RESERVED	21	1	—
HILOADEN	20	0	Set 1 to enable the output driver to drive high loads.
RESERVED	19	1	—
RESERVED	18	1	—
RESERVED	17	1	—
RESERVED	16	1	—
FHIPEN	15	1	Highpass coupling enable. Set 1 to enable the highpass coupling between the filter and PGA, or 0 to disable the coupling.
RESERVED	14	1	—
RESERVED	13	1	—
RESERVED	12	0	—
STRMEN	11	0	DSP interface for serial streaming of data enable. This bit configures the IC such that the DSP interface is inserted in the signal path. Set 1 to enable the interface or 0 to disable the interface.

表9. 配置3 (地址：0010) (续)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
STRMSTART	10	0	The positive edge of this command enables data streaming to the output. It also enables clock, data sync, and frame sync outputs.
STRMSTOP	9	0	The positive edge of this command disables data streaming to the output. It also disables clock, data sync, and frame sync outputs.
RESERVED	8:6	111	—
STRMBITS	5:4	01	Number of bits streamed. D5:D4 = 00: reserved; 01: 1 MSB, 1 LSB; 10: reserved, Q MSB; 11: 1 MSB, 1 LSB, Q MSB, Q LSB.
STAMPEN	3	1	The signal enables the insertion of the frame number at the beginning of each frame. If disabled, only the ADC data is streamed to the output.
TIMESYNCEN	2	1	This signal enables the output of the time sync pulses at all times when streaming is enabled by the STRMEN command. Otherwise, the time sync pulses are available only when data streaming is active at the output, for example, in the time intervals bound by the STRMSTART and STRMSTOP commands.
DATSYNCEN	1	0	This control signal enables the sync pulses at the DATASYNC output. Each pulse is coincident with the beginning of the 16-bit data word that corresponds to a given output bit.
STRMRST	0	0	This command resets all the counters irrespective of the timing within the stream cycle.

表10. PLL配置(地址：0011)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27	1	—
RESERVED	26	0	—
RESERVED	25	0	—
REFOUTEN	24	1	Clock buffer enable. Set 1 to enable the clock buffer or 0 to disable the clock buffer.
RESERVED	23	1	—
REFDIV	22:21	11	Clock output divider ratio. Set D22:D21 = 00: clock frequency = XTAL frequency x 2; 01: clock frequency = XTAL frequency/4; 10: clock frequency = XTAL frequency/2; 11: clock frequency = XTAL.
IXTAL	20:19	01	Current programming for XTAL oscillator/buffer. Set D20:D19 = 00: reserved; 01: buffer normal current; 10: reserved; 11: oscillator high current.
RESERVED	18:14	10000	—
LDMUX	13:10	0000	PLL lock-detect enable.

表10. PLL配置(地址：0011) (续)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
ICP	9	0	Charge-pump current selection. Set 1 for 1mA and 0 for 0.5mA.
PFDEN	8	0	Set 0 for normal operation or 1 to disable the PLL phase frequency detector.
RESERVED	7	0	—
RESERVED	6:4	000	—
INT_PLL	3	1	PLL mode control. Set 1 to enable the integer-N PLL or 0 to enable the fractional-N PLL.
PWRSAV	2	0	PLL power-save mode. Set 1 to enable the power-save mode or 0 to disable.
RESERVED	1	0	—
RESERVED	0	0	—

表11. PLL整数分频比(地址：0100)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
NDIV	27:13	1536d	PLL integer division ratio.
RDIV	12:3	16d	PLL reference division ratio.
RESERVED	2:0	000	—

表12. PLL分频比(地址：0101)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
FDIV	27:8	80000h	PLL fractional divider ratio.
RESERVED	7:0	01110000	—

表13. 保留(地址：0110)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:0	8000000h	—

表14. 时钟小数分频比(地址：0111)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
L_CNT	27:16	256d	Sets the value for the L counter. 000100000000 = 256 fractional clock divider, 100000000000 = 2048 fractional clock divider.
M_CNT	15:4	1563d	Sets the value for the M counter. 011000011011 = 1563 fractional clock divider, 100000000 = 2048 fractional clock divider.
FCLKIN	3	0	Fractional clock divider. Set 1 to select the ADC clock to come from the fractional clock divider, or 0 to bypass the ADC clock from the fractional clock divider.
ADCCLK	2	0	ADC clock selection. Set 0 to select the ADC and fractional divider clocks to come from the reference divider/multiplier.
RESERVED	1	1	—
MODE	0	0	DSP interface mode selection.

表15. 测试模式1 (地址：1000)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:0	1E0F401	—

表16. 测试模式2 (地址：1001)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:1	28C0402	—
FCENMSB	0	0	When combined with FCEN, this bit represents the MSB of a 7-bit FCEN word.

应用信息

LNA和混频器输入匹配至50Ω线路，需要仔细考虑。为确保所有RF电路可靠工作，需要正确的电源旁路、接地和布局。

电路板布局

MAX2769B评估板可以作为布局的起点。为获得最佳性能，应考虑RF、基带和电源PCB线路的接地和走线。使过孔到接地区域的连接尽量短。高阻端口应保持尽量短的走线，将并联寄生电容降至最小，可访问china.maxim-ic.com索取评估板Gerber文件。

电源布局

为最大程度地降低IC不同电路之间的耦合，建议采用星形电源布线方式，并在中心$V_{CC_}$节点使用较大的去耦电容。$V_{CC_}$走线从该节点引出，每个支路连接至电路的不同$V_{CC_}$节点。安装旁路电容时，电容应尽量靠近各个电源引脚。这种布局能够在每个$V_{CC_}$引脚处实现本地去耦。对于低电感接地，每个旁路电容至少使用一个过孔。请勿与任何其它支路共用电容接地过孔。

更多信息请参考Maxim的无线和射频(RF)应用笔记。

芯片信息

PROCESS: SiGe BiCMOS

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2769BETI/V+	-40°C to +85°C	28 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
/V表示汽车级器件。

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
28 TQFN-EP	T2855+3	**21-0140**	**90-0023**

修订历史

修订号	修订日期	说明	修改页
0	5/11	最初版本。	—
1	8/11	修正*定购信息*部分的器件型号。	24

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