数据资料缩写本

219-0017; Rev 2; 1/13

DS2465

DeepCover安全认证器具有SHA-256协处理器和1-Wire主机功能

概述

DeepCover™嵌入式安全方案通过多层高级物理保护为系统提供最安全的密钥存储，有效保护敏感数据。

DS2465是一款SHA-256协处理器，内置1-Wire®主控制器，提供主机系统与1-Wire SHA-256从器件通信及操作所要求的SHA-256和存储器功能。此外，器件执行I²C主控制器与所连接的任何1-Wire SHA-256从器件之间的协议转换。对于1-Wire线驱动，芯片内部用户可调定时器将系统主处理器从繁琐的1-Wire波形时序控制中解放出来，支持标准和高速1-Wire通信。1-Wire总线可通过软件控制关断。强上拉功能通过1-Wire总线为诸如EEPROM等1-Wire器件供电。不使用DS2465时，可将其置于休眠模式，降低功耗。

定购信息在数据资料的最后给出。

特性

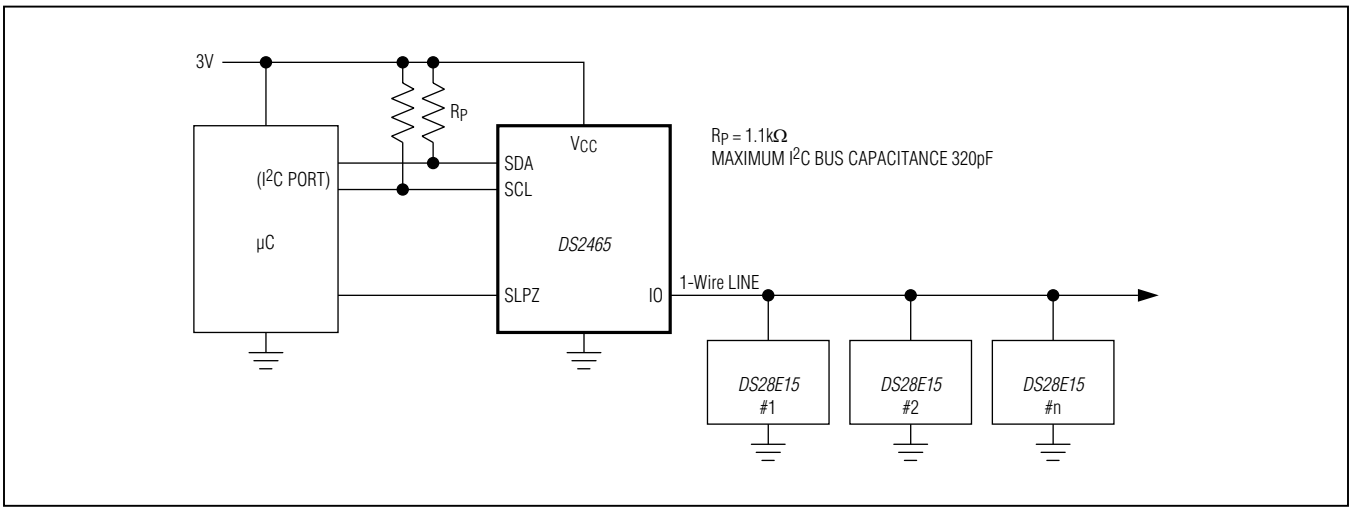
- SHA-256引擎，支持基于对称密匙的双向安全认证模型
- 两个32字节用户EEPROM页，带有多种可编程保护选项
- 1-Wire主控端口，带有可选的有源或无源1-Wire上拉
- 内部低阻信号通路提供1-Wire强上拉
- 1-Wire端口可通过软件控制关断
- I²C工作(上拉)电压：3.3V ±10%
- 工作范围：3.3V ±10%，-40°C至+85°C
- 6引脚TSOC封装

应用

消费类产品安全认证

安全控制

典型工作电路



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to GND .....-0.5V to +4.0V
Maximum Current into Any Pin.....20mA
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.97	3.3	3.63	V
Supply Current	I_{CC}	(Note 2)			750	µA
		Sleep mode (SLPZ pin low), V_{CC} = 3.63V		0.5	1.0	
Power-On Reset Trip Point	V_{POR}	(Note 3)		1.0	1.4	V
1-Wire Input High	V_{IH1}		0.6 x V_{CC}			V
1-Wire Input Low	V_{IL1}				0.2 x V_{CC}	V
1-Wire Weak Pullup Resistor (Notes 3, 4)	R_{WPU}	Low range	375	500	750	Ω
		High range	750	1000	1350	
1-Wire Output Low	V_{OL1}	V_{CC} = 2.97V, 8mA sink current			0.25	
Active Pullup On Threshold	V_{IAPO}	(Note 3)		0.95	1.2	V
Active Pullup On Time (Notes 3, 5)	t_{APU}	1-Wire time slot	Equal to t_{REC0}			µs
		1-Wire reset standard speed	2.375	2.5	2.625	
		1-Wire reset overdrive speed	0.475	0.5	0.525	
Active Pullup Impedance	R_{APU}	V_{CC} = 2.97V, 4mA load (Note 3)			60	Ω
1-Wire Output Fall Time (Note 3)	t_F	Standard	0.25		1	µs
		Overdrive	0.05		0.2	
IO PIN: 1-Wire TIMING (Note 6)						
Reset Low Time	t_{RSTL}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Reset High Time	t_{RSTH}	Standard and overdrive	Equal to t_{RSTL}			µs
Presence-Detect Sample Time	t_{MSP}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Sampling for Short and Interrupt	t_{SI}	Standard	7.6	8	8.72	µs
		Overdrive	1.9	2	2.18	
Write-1/Read Low Time	t_{W1L}	Standard	7.6	8	8.72	µs
		Overdrive	-5%	See Table 6	+9%	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Sample Time	t_{MSR}	Standard	11.4	12	13.1	µs
		Overdrive	1.4	1.5	1.64	
Write-0 Low Time	t_{W0L}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Write-0 Recovery Time	t_{REC0}	Standard and overdrive	-5%	See Table 6	+9%	µs
1-Wire Time Slot	t_{slot}	Standard and overdrive	Equal to t_{W0L} + t_{REC0}			µs
SHA-256 ENGINE						
Computation Current	I_{CSHA}	参见数据资料完整版。				mA
Computation Time	t_{CSHA}					ms
EEPROM						
Programming Current	I_{PROG}	(Notes 3, 7)			2	mA
Programming Time for a 32-Bit Segment	t_{PROG}				10	ms
Write/Erase Cycling Endurance	N_{CY}	T_A = +125°C (Notes 8, 9)	100k			—
Data Retention	t_{DR}	T_A = +125°C (storage) (Notes 10, 11)	10			Years
SLPZ PIN						
Low Level Input Voltage	V_{IL}		-0.5		0.3 x V_{CC}	V
High Level Input Voltage	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.5V	V
Input Leakage Current	I_I	Pin at 3.63V (Note 3)			0.1	µA
Wake-Up Time from Sleep Mode	t_{SWUP}	(Note 12)			200	µs
I²C SCL AND SDA PINS (Note 13)						
Low Level Input Voltage	V_{IL}		-0.5		0.3 x V_{CC}	V
High Level Input Voltage	V_{IH}		0.7 x V_{CC}		$V_{CC(MAX)}$ + 0.5V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	(Note 3)	0.05 x V_{CC}			V
Low Level Output Voltage at 3mA Sink Current	V_{OL}				0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(Note 3)	60		250	ns
Pulse Width of Spikes That Are Suppressed by the Input Filter	t_{SP}	(Note 3)			50	ns
Input Current with an Input Voltage Between 0.1$V_{CC(MAX)}$ and 0.9$V_{CC(MAX)}$	I_I	(Notes 3, 14)	-10		+10	µA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	(Note 3)			10	pF
SCL Clock Frequency	f_{SCL}		0		400	kHz
Hold Time (Repeated) START Condition; After this Period, the First Clock Pulse is Generated	$t_{HD:STA}$	(Note 3)	0.6			µs
Low Period of the SCL Clock	t_{LOW}	(Note 3)	1.3			µs
High Period of the SCL Clock	t_{HIGH}	(Note 3)	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(Note 3)	0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 3, 15, 16)			0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Notes 3, 17)	250			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 3)	0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	(Note 3)	1.3			µs
Capacitive Load for Each Bus Line	C_B	(Notes 3, 18)			400	pF
Oscillator Warmup Time	t_{OSCWUP}	(Note 12)			200	µs

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 2: Operating current with 1-Wire write byte sequence followed by continuous read of 1-Wire Master Status register at 400kHz in overdrive.

Note 3: Guaranteed by design and/or characterization only. Not production tested.

Note 4: Active pullup or resistive pullup and range are configurable.

Note 5: The active pullup does not apply to the rising edge of a presence pulse outside of a 1-Wire Reset Pulse command or during the recovery after a short on the 1-Wire line.

Note 6: All 1-Wire timing specifications are derived from the same timing circuit.

Note 7: Current drawn from V_{CC} during the EEPROM programming interval or SHA-256 computation.

Note 8: Write-cycle endurance is tested in compliance with JESD47G.

Note 9: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 10: Data retention is tested in compliance with JESD47G.

Note 11: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 12: I^2C communication should not take place for the max t_{OSCWUP} or t_{SWUP} time following a power-on reset or a wake-up from sleep mode.

Note 13: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 14: I/O pins of the DS2465 do not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 15: The DS2465 provides a hold time of at least 300ns for the SDA signal (referenced to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 16: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock (I^2C bus specification Rev. 03, 19 June 2007).

Note 17: A fast-mode I^2C bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I^2C bus specification) before the SCL line is released. Also the acknowledge timing must meet this setup time (I^2C bus specification Rev. 03, 19 June 2007).

Note 18: C_B = Total capacitance of one bus line in pF. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application (I^2C bus specification Rev. 03, 19 June 2007).

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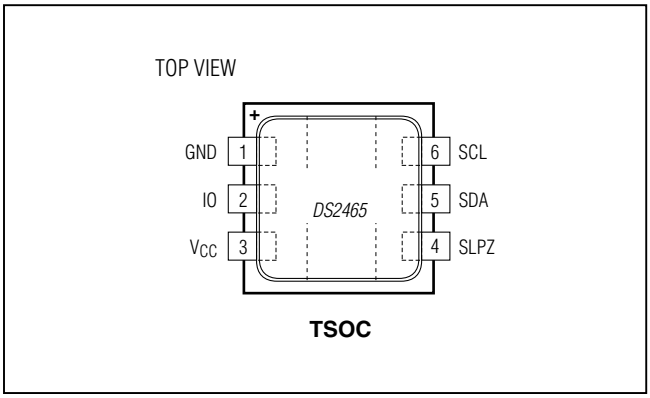
引脚配置



TSOC

引脚说明

引脚	名称	功能
1	GND	地基准。
2	IO	1-Wire总线的I/O驱动器。
3	V_{CC}	电源输入。
4	SLPZ	低电平有效控制输入。激活低功耗休眠模式，并发送SHA协处理器和1-Wire主控制器的器件复位(等效于1-Wire Master Reset命令)。
5	SDA	I^2C串行数据输入/输出。必须通过上拉电阻连接至V_{CC}。
6	SCL	I^2C串行时钟输入。必须通过上拉电阻连接至V_{CC}。

详细说明

DS2465是一款SHA-256协处理器，内置1-Wire主控制器和两个用户存储器页。

详细信息请参见数据资料完整版。

自定时1-Wire主控功能支持高级1-Wire波形发生器，包括标准和高速模式、有源上拉，以及强上拉。有源上拉影响1-Wire侧的上升沿。强上拉功能利用相同的上拉晶体管作为有源上拉，但采用不同的控制机制。DS2465的输入输出控制器收到命令和数据时，执行1-Wire通信功能，例如复位/应答检测、读字节、写字节、单位R/W，以及用于ROM搜索的三合一命令，无需主处理器介入。主机通过1-Wire主控制器状态寄存器获得反馈(完整的1-Wire功能、应答脉冲、1-Wire短路及搜索方向)，通过1-Wire读数据寄存器获得数据。全部寄存器、用户存储器和暂存器位于线性地址空间，用于直接存取。DS2465通过I^2C总线接口以标准模式或高速模式与主机处理器进行通信。方框图请参见图1。

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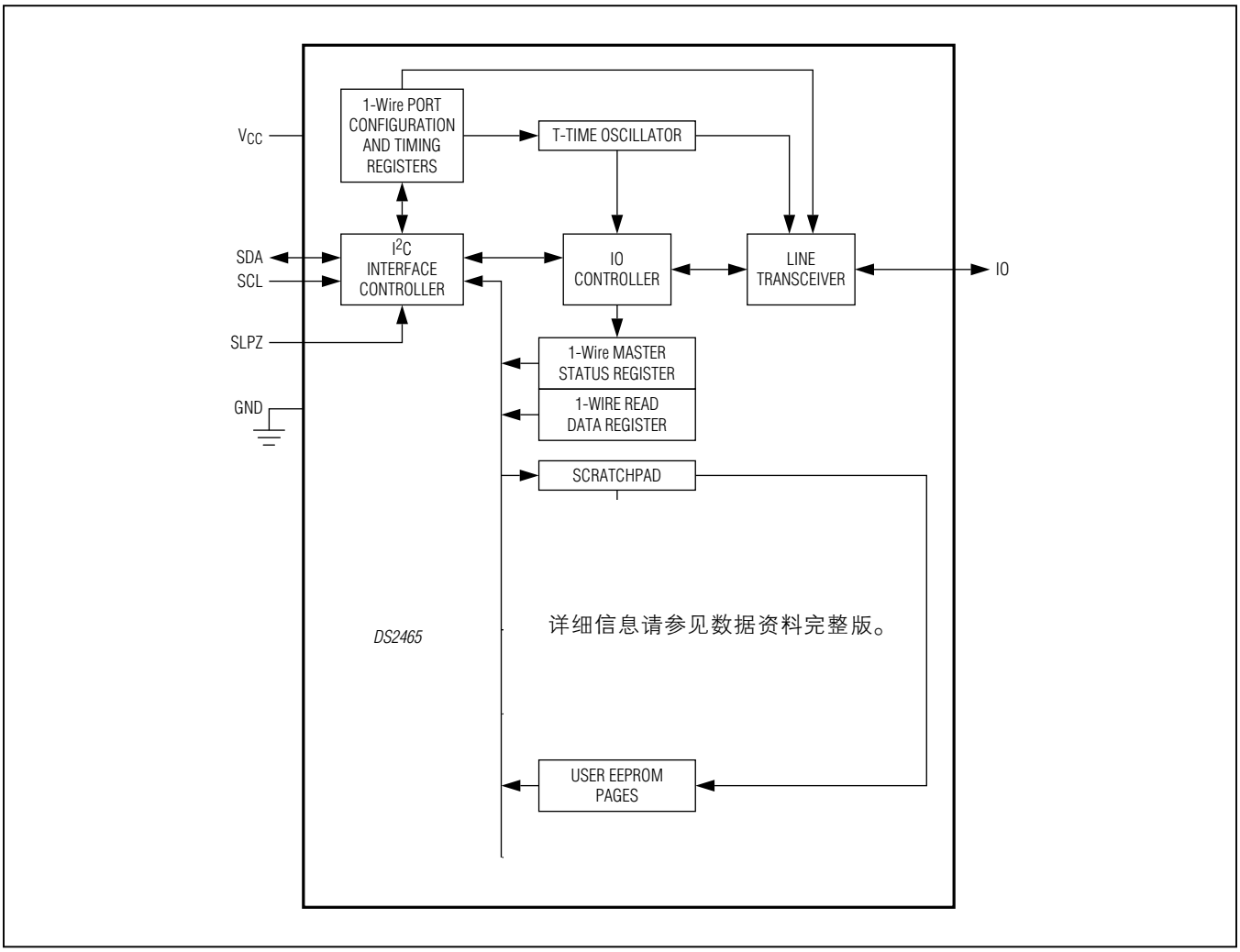

图1. 方框图

存储器

图2所示为DS2465的存储器结构。存储器从地址00h开始，带有输入暂存器。寄存器部分从地址60h开始。地址00至6F全部为易失SRAM。1-Wire端口配置具有默认值，上电期间自动装载。70h及更高地址范围为非易失存储器，包含工厂设置的器件识别数据、个性化字节及用户存储器页。

详细信息请参见数据资料完整版。

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ADDRESS RANGE	TYPE	ACCESS	DESCRIPTION
00h to 4Bh	SRAM	R/W	Input scratchpad
4Ch to 5Fh	—	—	(Reserved)
60h	—	W	Command register
61h	SRAM	R	1-Wire Master Status register
62h	SRAM	R	1-Wire Read Data register
参见数据资料完整版。			
66h	—	—	(Reserved)
67h	SRAM	R/W	1-Wire Master Configuration register
68h	SRAM	R/W	1-Wire Port Configuration t_{RSTL}
69h	SRAM	R/W	1-Wire Port Configuration t_{MSP}
6Ah	SRAM	R/W	1-Wire Port Configuration t_{W0L}
6Bh	SRAM	R/W	1-Wire Port Configuration t_{REC0}
6Ch	SRAM	R/W	1-Wire Port Configuration R_{WPU}
6Dh	SRAM	R/W	1-Wire Port Configuration Overdrive t_{W1L}
6Eh to 6Fh	—	—	(Reserved)
70h	ROM	R	Factory byte
参见数据资料完整版。			
73h	ROM	R	Personality byte
74h to 7Fh	—	—	(Reserved)
80h to 9Fh	EEPROM	(R)/(W)	User memory page 0
A0h to BFh	EEPROM	(R)/(W)	User memory page 1
C0h to FFh	—	—	(Reserved)

图2. 存储器映射

器件寄存器

DS2465的寄存器分为三类：只写、只读和读/写。只写适用于命令寄存器。状态寄存器、1-Wire读数据寄存器为只读。配置寄存器可读、写，也具有确定的上电默认值。工厂字节、制造商ID和个性化字节为只读。

命令寄存器(60h)

为执行1-Wire功能，DS2465需要从I²C主机接收命令。将命令每次一条写入命令寄存器。大多数命令包括命令代码和参数字节。命令代码表示指令的类型，以及下一次I²C读操作的指针位置。详细信息请参见*功能命令*部分。

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1-Wire主控状态寄存器(61h)

1-Wire主控状态寄存器是DS2465向主机处理器报告1-Wire侧的位型数据、1-Wire总线状态及其自身复位状态的通用方式(表1)。全部1-Wire通信命令和1-Wire主控复位命令将读指针定位在状态寄存器，使主机处理器以最小的协议开销进行读操作。状态信息仅在执行特定命令期间更新。详细信息请参见以下不同状态位的说明。

表1. 1-Wire主控状态位分配

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR	TSB	SBR	RST	LL	SD	PPD	1WB

第7位：选择搜索路径(DIR)。无论何时执行1-Wire Triplet命令，该位将向主机处理器报告Triple命令的第三位所选的搜索方向。DIR的上电默认值为0。该位仅根据1-Wire Triplet命令更新，不受其它命令影响。更多信息请参考1-Wire Triplet命令的说明和*应用笔记187：1-Wire搜索算法*。

第6位：Triplet命令第二位(TSB)。TSB位表示1-Wire Triplet命令第二位在t_{MSR}采样时刻有源1-Wire总线的逻辑状态。TSB的上电默认值为0。该位仅根据1-Wire Triplet命令更新，不受其它命令影响。

第5位：单个位结果(SBR)。SBR位表示1-Wire Single Bit命令或1-Wire Triplet命令第一位在t_{MSR}采样时刻有源1-Wire总线的逻辑状态。SBR的上电默认值为0。如果1-Wire Single Bit命令发送0位，SBR应为0。执行1-Wire Triplet命令时，SBR为0还是1，取决于所连接的1-Wire器件的响应。1-Wire Single Bit命令发送1位时，结果与此相同。

第4位：器件复位(RST)。如果RST位为1，则DS2465执行了内部复位周期，可由上电复位引起(SLPZ上的低电平脉冲)，也可由执行Device Reset命令引起。主机处理器更新1-Wire主控配置寄存器时，RST位自动清除。

第3位：逻辑电平(LL)。LL位表示有源1-Wire总线的逻辑状态，不发起任何1-Wire通信。每次读取1-Wire主控状态寄存器时对1-Wire进行采样。如果读指针指向1-Wire主控状态寄存器，主机处理器以读模式寻址DS2465时(应答周期内)，进行采样并更新LL位。

第2位：短路检测(SD)。每次执行1-Wire Reset命令时更新SD位。应答检测周期的t_{SI}时刻，如果DS2465在1-Wire总线上检测到逻辑0，SD位置1。如果短路条件已消除，随后的1-Wire Reset命令使该位返回默认值0。

第1位：应答脉冲检测(PPD)。每次执行1-Wire Reset命令时更新PPD位。应答检测周期的tMSP时刻，如果DS2465在1-Wire器件上检测到应答脉冲，PPD位置1。随后的1-Wire Reset命令期间，如果无应答脉冲或1-Wire总线短路，该位返回至默认值0。

第0位：1-Wire忙(1WB)。1WB位向主机处理器报告1-Wire总线是否处于忙状态。1-Wire通信期间，1WB为1；一旦完成命令，1WB返回至默认值0。关于1WB何时改变状态以及其保持为1的时间，详细信息请参见*功能命令*部分。

1-Wire读数据寄存器(62h)

DS2465完成1-Wire读字节命令后，将从1-Wire从器件读取的数据放入1-Wire读数据寄存器。执行命令时，I^2C主机检查1-Wire主控状态寄存器中的1WB位。1-Wire总线不再忙时，I^2C主机对地址62h执行虚拟写操作，然后以读模式访问DS2465，读取数据字节。

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1-Wire主控配置寄存器(67h)

DS2465支持四种1-Wire功能，通过1-Wire主控配置寄存器使能或选中(表3)。这些功能为：有源上拉(APU)、1-Wire关断(PDN)、强上拉(SPU)、1-Wire速率(1WS)。APU、SPU和1WS能够以任意组合选中。APU和1WS维持其状态时，只要强上拉结束，SPU返回至非激活状态。

器件复位后(电源开/关、SLPZ上的低电平脉冲，或由1-Wire主控复位命令发起)后，1-Wire主控配置寄存器为00h。写寄存器时，只有上半字节(位7至4)为下半字节(位3至0)的补码时，才接受新数据。读操作时，上半字节总为0h。

表3. 1-Wire主控配置位分配

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{1WS}$	$\overline{SPU}$	$\overline{PDN}$	$\overline{APU}$	1WS	SPU	PDN	APU

第3位：1-Wire速率(1WS)。1WS位决定DS2465产生的所有1-Wire通信的时序。许多1-Wire从器件支持标准速率(1WS = 0)。许多1-Wire器件也能以较高数据率通信，称为高速模式。部分1-Wire器件(包括DeepCover SHA-256系列从器件)，仅支持过驱动，对于这些器件1WS应始终设置为高电平。为从标准速率切换至高速模式，1-Wire器件需要接Overdrive-Skip ROM或Overdrive-Match ROM命令，如1-Wire器件数据资料中所述。1-Wire器件接收到速率改变命令编码后，立即改变速率。DS2465必须参与这种速率变化，以保持同步。在改变1-Wire器件速率的1-Wire字节命令之后，立即将1-Wire主控配置寄存器的1WS位置1，实现1-Wire器件速率的改变。将1-Wire主控配置寄存器的1WS位置0，后边跟1-Wire复位命令，则将有源1-Wire总线上的DS2465及全部1-Wire器件改回标准速率。

第2位：强上拉(SPU)。SPU位用于在1-Wire Write Byte、1-Wire Read Byte或1-Wire Single Bit命令之前激活强上拉功能。将暂存器数据复制到主存储器或执行SHA计算时，1-Wire EEPROM器件通常使用强上拉。相应器件的数据资料中规定了通信协议中启用强上拉的位置。对于那些将1-Wire器件置于要求额外电源状态的命令，必须在发送命令之前立即将SPU位置位。强上拉与有源上拉功能使用相同的内部上拉晶体管。根据*Electrical Characteristics*表中给出的R_{APU}参数，判断电压降是否低至足以维持给定负载电流和供电电压下要求的1-Wire电压。

如果SPU为1，DS2465将在强上拉开始的那个时隙的上升沿施加有源上拉。然而，与有源上拉相比，强上拉(例如内部上拉晶体管)保持导通，如图3所示，直到发生以下四种事件之一：DS2465接收产生1-Wire通信的命令(典型情况)；1-Wire主控配置寄存器中的SPU位置0；1-Wire主控配置寄存器中的SPU位置1；DS2465接收1-Wire Master Reset命令。强上拉结束时，SPU位自动复位至0。使用强上拉功能不改变1-Wire主控配置寄存器中APU位的状态。

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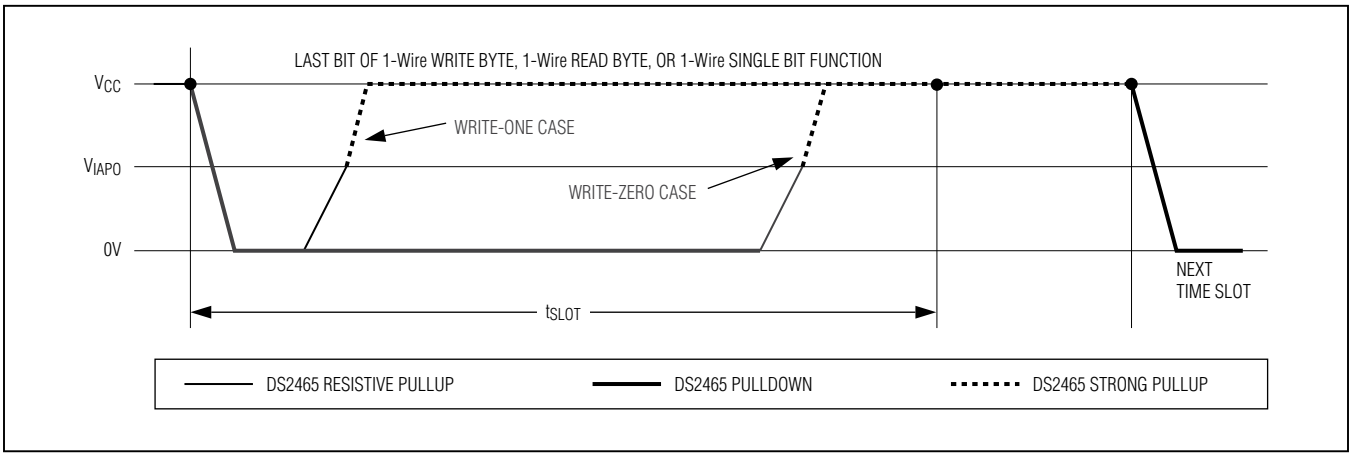

图3. 低阻上拉时序

第1位：1-Wire关断(PDN)。PDN位用于从1-Wire端口断开电源，例如，强制1-Wire从器件执行上电复位。PDN与休眠模式相互影响，由SLPZ引脚控制(表4)。PDN的默认状态为0，使能正常工作。PDN引脚改为1时，不能进行1-Wire通信。为结束1-Wire关断状态，PDN位需要改为0。为使DS2465退出休眠模式，将SLPZ引脚的状态从0改为1。这强制DS2465执行上电复位，并将PDN清0，实现正常工作。

表4. PDN和SLPZ的影响

	SLPZ PIN IS AT LOGIC 0	SLPZ PIN IS AT LOGIC 1
PDN is 0	• R_{WPU} is disconnected; IO is at 0V, causing the slaves to lose power. • The DS2465 is powered down (sleep mode).	• R_{WPU} is connected; IO is at V_{CC}, keeping the slaves powered. • The DS2465 is powered up (normal operation).
PDN is 1		• R_{WPU} is disconnected; IO is at 0V, causing the slaves to lose power. • The DS2465 is powered up.

第0位：有源上拉(APU)。APU位控制是使用有源上拉(低阻晶体管)还是使用无源上拉(R_{WPU}电阻)来将驱动1-Wire总线从低电平至高电平。APU = 0时，禁止有源上拉(电阻模式)。为实现最佳1-Wire性能，通常建议使能有源上拉。有源上拉不作用于1-Wire总线上短路之后恢复的上升沿。如果使能，固定周期的有源上拉(标准速率下为2.5µs，高速下为0.5µs)也作用于t_{RSTL}和t_{PDL}之后上升沿上的复位/应答检测周期。

控制上升沿的电路(图4)工作如下：在t_1时刻，下拉(从DS2465或1-Wire从器件)结束。从这一刻开始，通过DS2465内部的R_{WPU}将1-Wire总线拉高。斜率由V_{CC}和1-Wire总线上的电容负载决定。如果禁止有源上拉(APU = 0)，电阻继续拉高，如实线所示。使能有源上拉时(APU = 1)，当电压在t_2时刻达到V_{IAPO}门限时，DS2465激活低阻上拉晶体管，如虚线所示。有源上拉保持有效，直到时隙结束(t_3)，此后保持电阻上拉。写0时隙中，有源上拉的最短持续时间为t_{REC0}；写1时隙中，最长持续时间为$t_{W0L} + t_{REC0} - t_{W1L}$。读数据时隙中，有源上拉持续时间与从器件有关。关于保持上拉晶体管超出t_3时刻后导通的方法，请参见强上拉(SPU)部分。

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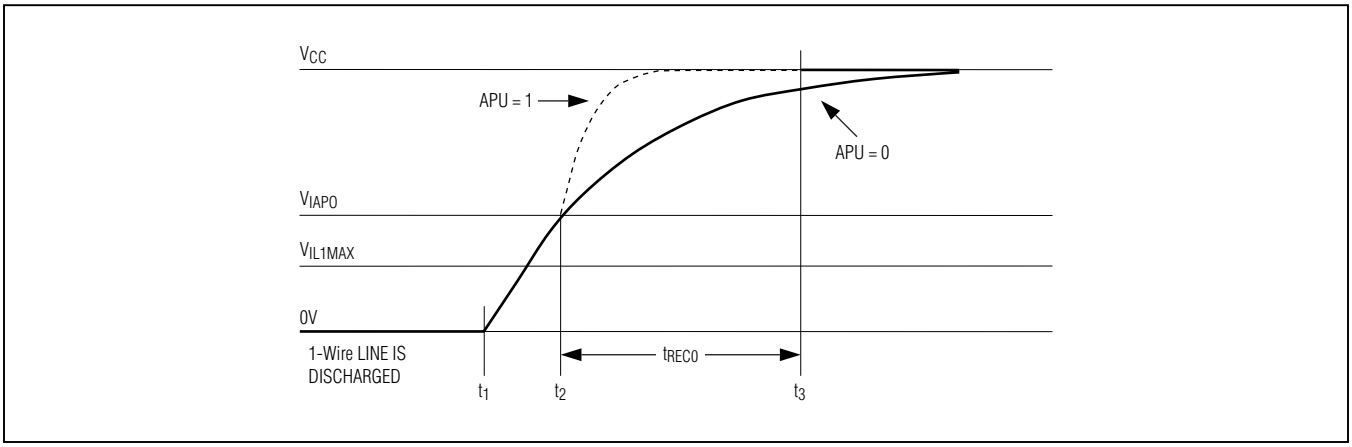

图4. 时隙期间的上升沿上拉

1-Wire端口配置

DS2465允许多种定时参数和上拉电阻自适应应用的需求。其中每个参数具有自身的1-Wire端口配置寄存器，位于68h至6Dh地址范围(表5)。对于标准和高速模式，t_{RSTL}、t_{MSP}和t_{W0L}的值可独立调整。下半字节适用于标准速率，上半字节适用于高速。t_{RECO}和R_{WPU}设置适用于两种1-Wire速率。参数t_{W1L}只可针对高速进行调整；标准速率下为固定us值。对于t_{RECO}、R_{WPU}和t_{W1L}，上半字节无作用。关于二进制编码和参数值之间的转换，请参见表6。

器件复位后(电源开/关、SLPZ上的低电平脉冲，或由1-Wire主控复位命令发起)后，1-Wire端口配置寄存器被初始化为默认值。为改变端口配置，在I^2C写模式下访问相应的寄存器，并提供新编码作为数据字节。从地址68h开始，全部端口配置均可以单次写操作进行调整。如果1-Wire总线不忙(1WB = 0)，新设置在数据字节应答位的SCL上升沿生效。6Bh至6Dh寄存器的高4位不使用，可对其执行写操作，但其值对器件工作无影响。

表5. 1-Wire端口配置地址

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
68h	t_{RSTL} Overdrive Speed (OD)				t_{RSTL} Standard Speed (STD)			
69h	t_{MSP} Overdrive Speed (OD)				t_{MSP} Standard Speed (STD)			
6Ah	t_{W0L} Overdrive Speed (OD)				t_{W0L} Standard Speed (STD)			
6Bh	(not used, default 0000b)				t_{RECO} (speed independent)			
6Ch	(not used, default 0000b)				R_{WPU} (speed independent)			
6Dh	(not used, default 0000b)				t_{W1L} Overdrive Speed (OD)			

表6. 参数编码与典型参数之间的转换

PARAMETER VALUE CODE	t_{RSTL} VALUE IN µs		t_{MSP} VALUE IN µs		t_{W0L} VALUE IN µs		t_{REC0} VALUE IN µs	R_{WPU} VALUE IN Ω	t_{W1L} VALUE IN µs
	STD	OD	STD	OD	STD	OD	STD, OD	STD, OD	OD
0000b	440	44	58	5.5	52	5.0	2.5	500	do not use
0001b	460	46	58	5.5	54	5.5	2.5	500	0.25
0010b	480	48	60	6.0	56	6.0	2.5	500	0.50
0011b	500	50	62	6.5	58	6.5	2.5	500	0.75
0100b	520	52	64	7.0	60	7.0	2.5	500	**1.00**
0101b	540	54	66	7.5	62	7.5	2.5	500	1.25
0110b	**560**	**56**	**68**	**8.0**	**64**	**8.0**	**5.0**	**1000**	1.50
0111b	580	58	70	8.5	66	8.5	7.5	1000	1.75
1000b	600	60	72	9.0	68	9.0	10.0	1000	2.00
1001b	620	62	74	9.5	70	9.5	12.5	1000	2.25
1010b	640	64	76	10.0	70	10	15.0	1000	2.50
1011b	660	66	76	10.5	70	10	17.5	1000	2.75
1100b	680	68	76	11.0	70	10	20.0	1000	3.00
1101b	700	70	76	11.0	70	10	22.5	1000	3.25
1110b	720	72	76	11.0	70	10	25.0	1000	3.50
1111b	740	74	76	11.0	70	10	25.0	1000	3.75

***注：粗体字**为上电默认值。*

工厂字节(70h)

该字节为55h。

请参见数据资料完整版。

个性化字节(73h)

该字节为00h。

功能命令

DS2465支持 功能命令。至主机的反馈路径由读指针控制，由每条功能命令自动设置，使主机高效率访问相关信息。主机处理器通过I²C接口将这些命令和应用参数作为一个或两个字节的串发送。I²C协议要求接收方应答每个字节，以确认接收，或者不应答，表示错误条件(无效编码或参数)或结束通信。关于包括应答的I²C协议的详细信息，请参见*I²C接口*部分。

详细信息参见数据资料完整版。

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详细信息参见数据资料完整版。

下文中以表格方式简要介绍功能命令。

Copy Scratchpad	
Command Code	5Ah
Parameter Byte	Data destination, segment number (Table 7)
Usage	Transferring scratchpad data to user EEPROM pages; installing the master secret in the device
Other Notes	If the target memory is write-protected, this command cannot not complete successfully. Data is taken from the scratchpad location that corresponds to the segment number. Example: segment 0 corresponds to SP+0 to SP+3, addresses 00h to 03h.
Command Restrictions	The data must first be written to the scratchpad. The target memory must not be write-protected (locked).
Error Conditions (Error Response)	If the target memory is write protected, the memory write cycles do not take place. In that case the device is not busy and acknowledges its I^2C address immediately when accessed.
MAC Notes	详细信息参见数据资料完整版。
I^2C Busy Duration	For 1 x t_{PROG} or 8 x t_{PROG} depending on the parameter byte, counted from the rising SCL edge of the parameter byte acknowledge bit.
Command Duration	I^2C busy duration + 1.09µs
1-Wire Activity	None
Read Pointer Position	1-Wire Master Status register
Master Status Bits Affected	None
Master Configurations Affected	None
1-Wire Port Configurations Affected	None
Memory Protection Status Affected	The current protection settings apply.

表7. 参数字节位映射

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S/U	X	TT		F/S	SEG#		

X = 无关。

参见数据资料完整版。

第5至4位：目标(TT)。这些位指定将暂存器数据复制到的用户存储器页号(S/U = 1)。如果S/U = 0，TT必须为00。

如果S/U = 1，分配如下：

00 用户页0

01 用户页1

10 (保留)

11 (保留)

第3位：全部或段复制(F/S)。只有S/U = 1时，该位才生效。该位指定是编程整个存储器页还是仅编程SEG#所选定的段。如果F/S = 0，编程整个存储器页；如果F/S = 1，则仅编程选定的段。如果目标页之一具有写保护，那么F/S位强制为1。

第2至0位：段号(SEG#)。只有(S/U = 1)且(F/S = 1)时，这些位才有效。这些位指定用暂存器数据编程所选用户存储器段。全部编码有效。编码000b指存储器页的前4个字节，依此类推。

1-Wire Master Reset	
Command Code	F0h
Parameter Byte	N/A
Usage	Device initialization after power-up; re-initialization (reset) as desired.
Other Notes	Performs a global reset of device state machine logic. Terminates any ongoing 1-Wire communication.
Command Restrictions	The command must be followed by a 1-Wire Reset Pulse command.
Error Conditions (Error Response)	None
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	Maximum 1.635µs. Counted from rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Ends maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	(N/A)
Master Status Bits Affected	RST set to 1; 1WB, PPD, SD, SBR, TSB, DIR set to 0.
Master Configurations Affected	1WS, APU, PDN, SPU set to 0.
1-Wire Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} are reset to their default values.

1-Wire Reset Pulse	
Command Code	B4h
Parameter Byte	N/A
Usage	To initiate or end any 1-Wire communication sequence. To finish a 1-Wire Master Reset command.
Other Notes	Generates a 1-Wire reset/presence-detect cycle (Figure 5) at the 1-Wire line. The state of the 1-Wire line is sampled at t_{SI} and t_{MSP} and the result is reported to the host processor through the 1-Wire Master Status Register, bits PPD and SD.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	2 x t_{RSTL} + maximum 1.09µs, counted from the rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 2 x t_{RSTL}), PPD is updated at t_{RSTL} + t_{MSP}, SD is updated at t_{RSTL} + t_{SI}.
Master Configurations Affected	1WS and APU apply.
1-Wire Port Configurations Affected	t_{RSTL}, t_{MSP}, and R_{WPU} current values apply.

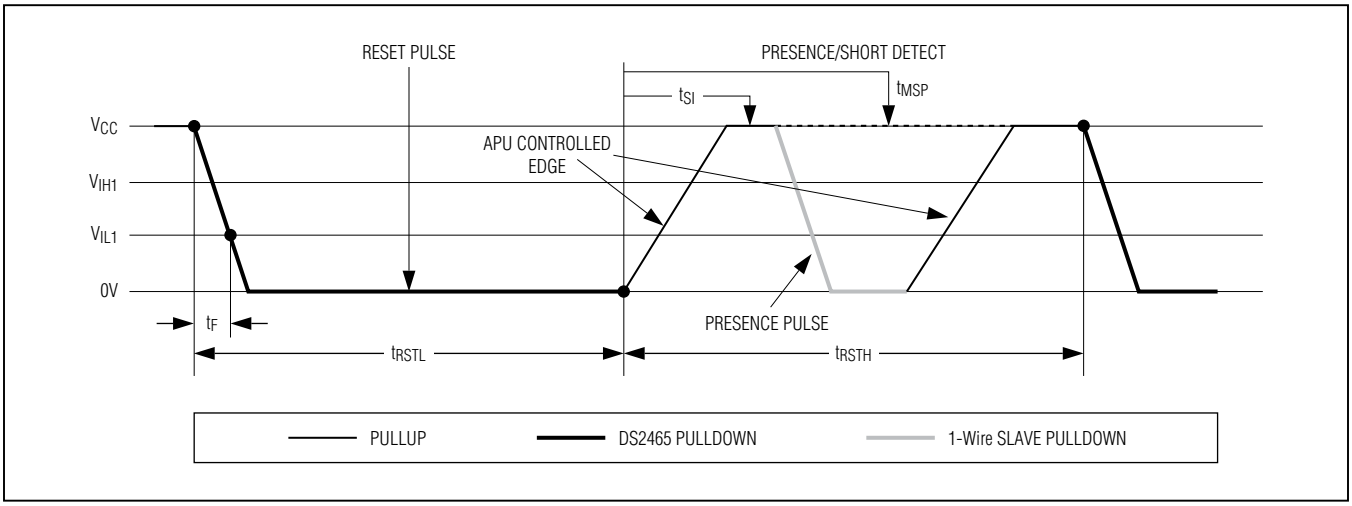


图5. 1-Wire复位/应答检测周期

1-Wire Single Bit	
Command Code	87h
Parameter Byte	Type of time slot (Table 21)
Usage	To perform single-bit writes or reads at the 1-Wire line when single bit communication is necessary (the exception).
Other Notes	Generates a single 1-Wire time slot as specified by the parameter byte at the 1-Wire line; reads the logic level at the 1-Wire line at t_{MSR} and updates SBR accordingly.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling and data reading).
Master Status Bits Affected	1WB (set to 1 for t_{SLOT}), SBR is updated at t_{MSR}, DIR (may change its state).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

表21. 参数字节位映射

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = 无关。

第7位：位值(V)。该位指定产生的时隙类型。如果V = 0，产生写0时隙(图6)。如果V = 1，产生写1时隙(图7)，该时隙也作为读数据时隙。

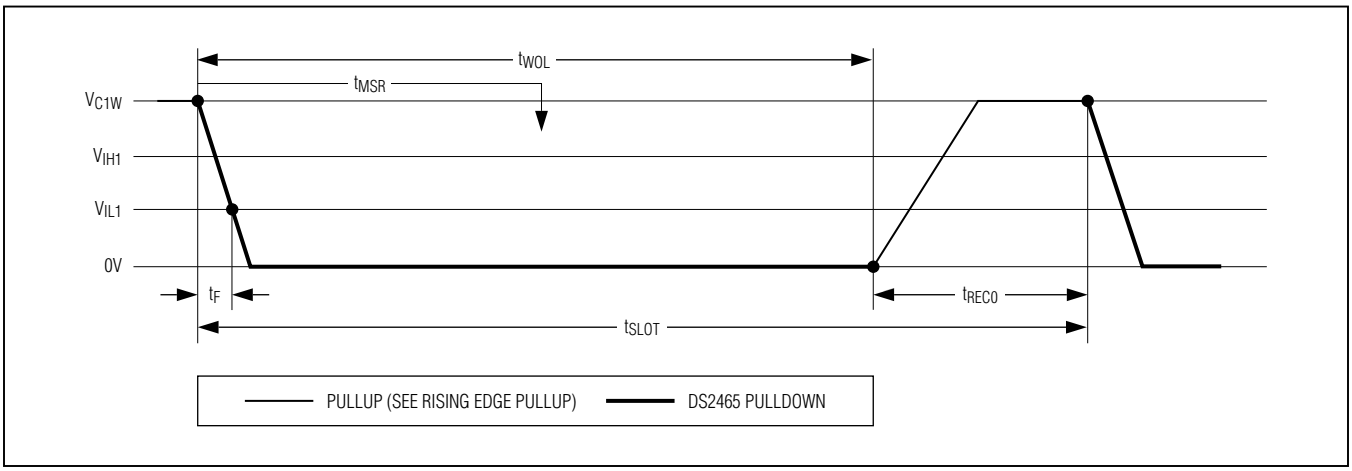
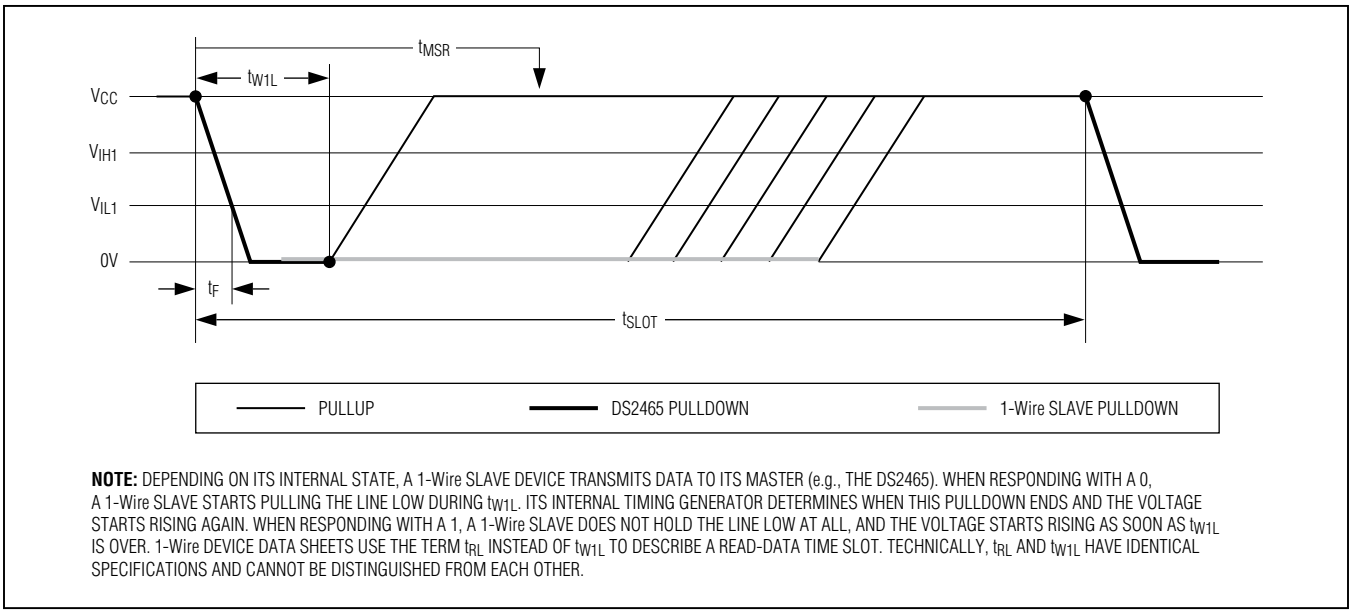


图6. 写零时隙



NOTE: DEPENDING ON ITS INTERNAL STATE, A 1-Wire SLAVE DEVICE TRANSMITS DATA TO ITS MASTER (e.g., THE DS2465). WHEN RESPONDING WITH A 0, A 1-Wire SLAVE STARTS PULLING THE LINE LOW DURING t_{W1L}. ITS INTERNAL TIMING GENERATOR DETERMINES WHEN THIS PULLDOWN ENDS AND THE VOLTAGE STARTS RISING AGAIN. WHEN RESPONDING WITH A 1, A 1-Wire SLAVE DOES NOT HOLD THE LINE LOW AT ALL, AND THE VOLTAGE STARTS RISING AS SOON AS t_{W1L} IS OVER. 1-Wire DEVICE DATA SHEETS USE THE TERM t_{RL} INSTEAD OF t_{W1L} TO DESCRIBE A READ-DATA TIME SLOT. TECHNICALLY, t_{RL} AND t_{W1L} HAVE IDENTICAL SPECIFICATIONS AND CANNOT BE DISTINGUISHED FROM EACH OTHER.

图7. 写1时隙和读数据时隙

1-Wire Write Byte	
Command Code	A5h
Parameter Byte	Data byte (Table 22)
Usage	To write commands or data to the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands, but faster due to less I^2C traffic.
Other Notes	Writes a single data byte to the 1-Wire line.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	8 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit. **Note:** The bit order on the I^2C bus and the 1-Wire line is different (1-Wire: LSB first; I^2C: MSB first). Therefore, 1-Wire activity cannot begin before the DS2465 has received the full data byte.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

表22. 参数字节位映射

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA							

第7至0位：数据字节(DATA)。这些位指定写至1-Wire总线的数据。先产生第0位的时隙。

1-Wire Read Byte	
Command Code	96h
Parameter Byte	N/A
Usage	To read data from the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands with V = 1 (write-one time slot), but faster due to less I^2C traffic.
Other Notes	Generates eight read-data time slots on the 1-Wire line and stores result in the 1-Wire Read Data Register.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	8 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling). **Note:** To read the data byte received from the 1-Wire line, issue a dummy write to memory address of the 1-Wire Read Data register. Then access the DS2465 in read mode.
Master Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{REC0}, t_{W1L}, and R_{WPU} current values apply.

1-Wire Triplet	
Command Code	78h
Parameter Byte	Branch Direction (Table 23)
Usage	To perform a 1-Wire Search ROM sequence; a full sequence requires this command to be executed 64 times to identify and address one device.
Other Notes	Generates three time slots: two read time slots and one write time slot at the 1-Wire line. The type of write time slot depends on the result of the read time slots and the direction byte. • If the read time slots are 0 and 1, they are followed by a write-zero time slot. • If the read time slots are 1 and 0, they are followed by a write-one time slot. • If the read time slots are both 1 (error case), the subsequent write time slot is a write-one. • If the read time slots are both 0, the parameter byte determines the type of the subsequent write time slot.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	3 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling and data reading).
Master Status Bits Affected	1WB (set to 1 for 3 x t_{SLOT}), SBR is updated at the first t_{MSR}, TSB and DIR are updated at the second t_{MSR} (i.e., at t_{SLOT} + t_{MSR}).
Master Configurations Affected	1WS, APU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

表23. 参数字节位映射

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = 无关。

第7位：位值(V)。该位指定第1和第2个读时隙均为0时选择的搜索方向。如果V = 0，产生写0时隙。如果V = 1，产生写1时隙。

1-Wire Receive Block	
Command Code	E1h
Parameter Byte	Block size (Table 25)
Usage	To read memory data from a secure 1-Wire memory device.
Other Notes	Reads 1 to 63 bytes from the 1-Wire line and makes them accessible from the scratchpad.
Command Restrictions	1-Wire activity must have ended before this command can be processed.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	None
I^2C Busy Duration	None
Command Duration	(1 to 63) x 8 x t_{SLOT} + maximum 1.09µs, counted from rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 8 x BS x t_{SLOT}).
Master Configurations Affected	1WS, APU apply
1-Wire Port Configurations Affected	t_{REC0}, t_{W1L}, and R_{WPU} current values apply.

表25. 参数字节位映射

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	BS					

X = 无关。

第5至0位：块大小(BS)。这些位指定接收和写入至输入暂存器的字节数量，从00h开始。如果BS = 000000b，接收一个字节。

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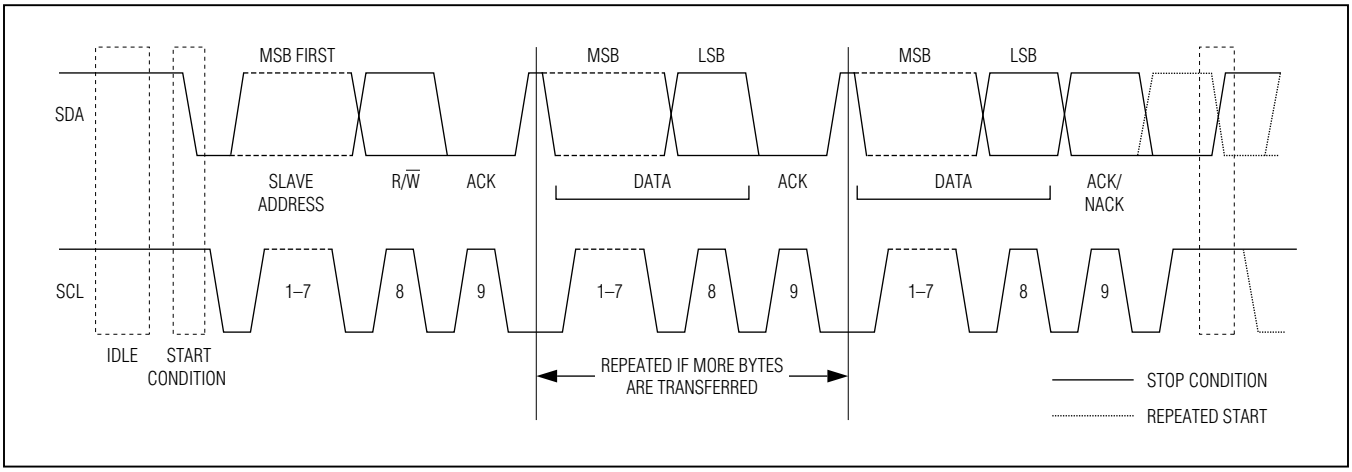

图8. I²C协议概览

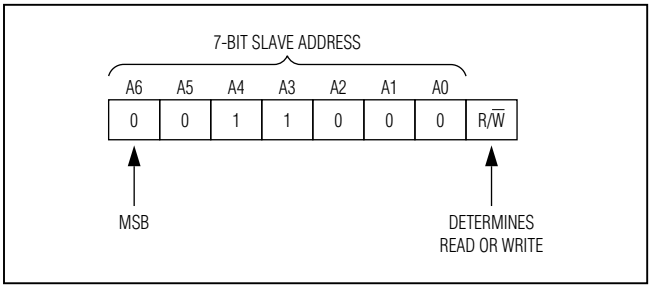

图9. DS2465从地址

I²C接口

一般特性

I²C总线通过一根数据线(SDA)和一根时钟信号线(SCL)进行通信。SDA和SCL是双向传输线，通过上拉电阻连接到正电源电压。不进行通信时SDA和SCL均为高电平。连接到总线的器件输出级必须是漏级开路或集电极开路，以满足线与功能。标准模式下I²C总线数据的传输速率可达100kbps，高速模式下可达400kbps。DS2465可工作在两种模式下。

总线上发送数据的器件被定义为发送器，接收数据的器件定义为接收器。控制通信的器件称为“主控制器”。由主控制器控制的器件是“从器件”。为了实现单独访问，各器件必须有一个从地址，且不和总线上其它器件相冲突。

当总线空闲时才能进行数据传输。主机产生串行时钟(SCL)，控制总线访问，发出启动和停止条件，并决定在启动和停止条件之间传输的数据字节的个数(图8)。数据传输时首先传送的是最高有效位。每个字节之后跟着的是应答位，以实现主控制器和从器件之间的同步。

从地址

DS2465响应的从地址见图9。从地址是从地址/控制字节的一部分。从地址/控制字节的最后一位(R/$\overline{W}$)定义数据方向。设置为0时，随后数据将从主控制器发至从器件(写操作模式)；设置为1时，数据将由从器件到主控制器(读操作模式)。

I²C定义

下面列出通常用来描述I²C数据传输的一些术语。时序基准如图10定义。

总线空闲或非忙状态：SDA和SCL空闲，此时逻辑状态为高电平。

START条件：为了与从器件进行通信，主控制器必须产生START条件。SCL保持高电平时，SDA从高电平跳变为低电平将产生一个START条件。

STOP条件：为了终止与从器件之间的通信，主控制器必须产生STOP条件。SCL保持高电平时，SDA从低电平跳变为高电平将产生一个STOP条件。

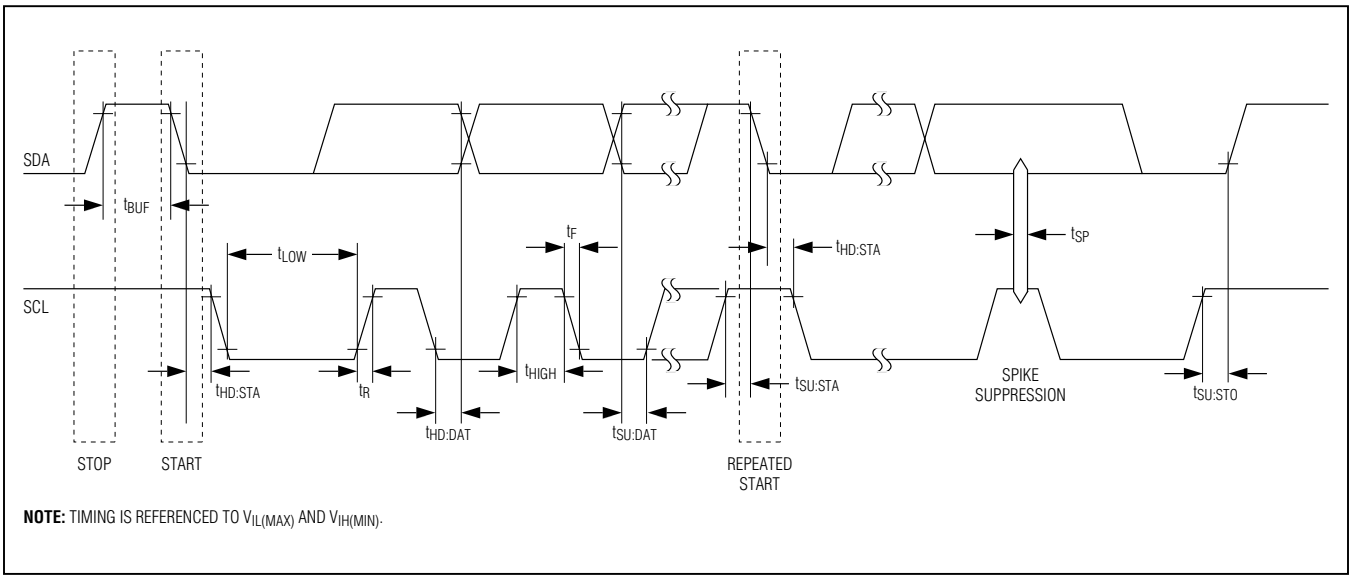

图10. I²C时序图

Repeated START条件：之前的写操作指定被读取的存储器地址后，Repeated START常用于执行读操作。在一次数据传输结束后，主控制器可以使用重复启动条件，在当前传输结束后立即启动一次新的数据传输。重复启动条件的产生与通常的启动条件一样，只是在停止条件之后，总线不会处于空闲状态而已。

数据有效：除START和STOP条件之外，SDA的跳变必须发生在SCL低电平期间。在整个SCL高电平期间、并在建立时间和保持时间(SCL下降沿后$t_{HD:DAT}$，SCL上升沿前$t_{SU:DAT}$，参见图10)要求的范围内，SDA数据须保持稳定有效。每位数据对应一个时钟脉冲，在SCL脉冲的上升沿将数据移入接收器件。

写操作完成后，主控制器必须释放SDA线，以保证在下一个SCL上升沿之前有充足的建立时间(最小值$t_{SU:DAT}$ + t_R，见图10)启动读操作。在SDA总线的前一个SCL脉冲下降沿，从器件逐位移出数据，数据位在当前SCL脉冲的上升沿时有效。主控制器产生所有的SCL时钟脉冲，包括那些读从器件数据所需的时钟。

从器件应答：通常，寻址的从器件收到每一个字节后，必须生成一个应答信号。主控制器必须为每个应答位产生时钟脉冲。应答时钟脉冲期间，应答器件必须拉低SDA，使其在时钟脉冲的高电平期间稳定为低电平。必须考虑建立和保持时间$t_{SU:DAT}$和$t_{HD:DAT}$。

主控制器应答：为继续从从器件进行读取，主控制器在收到每个字节后，必须生成一个应答信号。主控制器必须为每个应答位产生时钟脉冲。应答时钟脉冲期间，应答的主控制器必须拉低SDA，使其在时钟脉冲的高电平期间稳定为低电平。必须考虑SCL上升沿之前$t_{SU:DAT}$和SCL下降沿之后$t_{HD:DAT}$的建立和保持时间。

从器件未应答：当从器件忙于执行一个实时功能，如MAC计算或EEPROM写周期时，或者处于休眠模式时，从器件也许无法接收或传送数据。在这种情况下，从器件不会应答其从地址，SDA线为高电平。准备好通信的从器件至少会对其从地址做出应答。但是，有时从器件也许会拒绝接收数据，可能由于无效命令编码或意外数据。在这种情况下，从器件对其所拒绝接收的任何字节不进行应答，并使SDA为高电平。无论如何，在从器件应答失败之后，主控制器首先需要生成重复START条件，或在STOP条件后跟一个START条件以开始新的数据传送。

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主控制器未应答：有时当接收数据时，主控制器必须向从器件发送一个数据终止信号。为了获得这一信号，主控制器不应答它从从器件接收到数据的最后一个字节。作为响应，从器件释放SDA，允许主机发出停止条件。

读和写

为了写DS2465，主控制器必须以写操作模式访问器件，即必须将方向位设置为0发送从地址。写操作模式中发送的下一个字节为选择被写寄存器或存储器地址的地址字节，或者设置随后读操作的地址(虚拟写)。

为了读DS2465，主控制器必须以读操作模式访问器件，即必须将方向位设置为1来发送从地址。读地址由之前的写操作决定或由功能命令决定。

DS2465具有不同类型的存储器。有些区域允许不受限读/写操作[R/W]，其它区域为只写[W]、只读[R]，或具有用户可编程的存取限制[(R)/(W)]。

所以，读和写行为与地址有关。详细信息请参见图11。

1类行为

常见的I²C随机存取读/写协议，带有数据应答和地址自动递增功能。

2类行为

这种行为适用于命令寄存器、命令和参数字节被写入的地址，例如，激活SHA引擎或在1-Wire端口上开始任何行为。以写模式访问时，地址不递增。随后的读位置由主控制器所写的命令编码决定。以读模式访问时，从较低的地址开始，所读数据不确定，但地址递增。

ADDRESS RANGE	ACCESS	READ/WRITE BEHAVIOR	NOTES
00h to 4Bh	R/W	Type 1	Scratchpad.
4Ch to 5Fh	—	Type 1	Reserved. Data written is not stored. Data read is indeterminate.
60h	W	Type 2	Command register.
61h	R	Type 3	1-Wire Master Status.
62h	R	Type 4	1-Wire Read Data.
参见数据资料完整版。			
66h	—	Type 1	Reserved
67h to 6Dh	R/W	Type 1	1-Wire Configuration.
6Eh to 6Fh	—	Type 1	Reserved. Data written is not stored. Data read is indeterminate.
70h to 73h	R	Type 4	Factory-programmed data.
74h to 7Fh	—	Type 4	Reserved. Data read is indeterminate.
80h to BFh	(R)/(W)	Type 4	User memory.
C0h to FFh	—	Type 4	Reserved. Data written is not stored. Data read is indeterminate.

图11. 指定地址的读和写行为

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3类行为

这类行为适用于 1-Wire主控状态寄存器通过写模式操作为随后的读操作设置地址(虚拟写)，不应答数据字节。以读模式访问时，地址不递增。

4类行为

这类行为类似于1类行为，但数据字节被丢弃，适用于EEPROM位置和部分只读地址。通过写模式操作为随后的读操作设置地址(虚拟写)，应答数据字节后递增地址。以读模式访问时，在发送一个字节后地址递增。

I²C通信示例

关于I²C通信图例和数据方向编码的信息，请参见表26和表27。

表26. I²C通信—图例

SYMBOL	DESCRIPTION
S	START Condition
AD, 0	Select DS2465 for Write Access
AD, 1	Select DS2465 for Read Access
Sr	Repeated START Condition
P	STOP Condition
A	Acknowledged
A\	Not Acknowledged
(Idle)	Bus Not Busy
<byte>	Transfer of One Byte
CPS	Command “Copy Scratchpad”, 5Ah
参见数据资料完整版。	
1WMR	Command “1-Wire Master Reset”, F0h
1WRS	Command “1-Wire Reset Pulse”, B4h
1WSB	Command “1-Wire Single Bit”, 87h
1WWB	Command “1-Wire Write Byte”, A5h
1WRB	Command “1-Wire Read Byte”, 96h
1WT	Command “1-Wire Triplet”, 78h
参见数据资料完整版。	
1WRB	Command “1-Wire Receive Block”, E1h

表27. 数据方向编码

Master-to-Slave	Slave-to-Master	(DS2465 busy)

I²C通信示例(续)

Copy Scratchpad, e.g., to Write Data to the User Memory

S	AD,0	A	60h	A	CPS	A	<byte>	A	P	Programming

详细信息参见数据资料完整版。

详细信息参见数据资料完整版。

1-Wire Master Reset, e.g., After Power-Up

S	AD,0	A	60h	A	1WMR	A	Sr	AD,0	A	60h	A	1WRS	A	P

The 1-Wire Master Reset must be followed by a 1-Wire Reset Pulse command.

1-Wire Reset Pulse, e.g., to Begin or End 1-Wire Communication

Case A: 1-Wire Idle (1WB = 0), No Busy Polling to Read the Result

S	AD,0	A	60h	A	1WRS	A	P	(Idle)	S	AD,1	A	<byte>	A\	P

In the first cycle, the master sends the command; then the master waits (Idle) for the 1-Wire Reset to complete. In the second cycle the DS2465 is accessed to read the result of the 1-Wire Reset from the 1-Wire Master Status register.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed, then Read the Result

S	AD,0	A	60h	A	1WRS	A	Sr	AD,1	A	<byte>	A	<byte>	A\	P

Repeat until the 1WB bit has changed to 0.

Case C: 1-Wire Busy (1WB = 1)

S	AD,0	A	60h	A	1WRS	A\	P

The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

1-Wire Single Bit, e.g., to Generate a Single Time Slot on the 1-Wire Line

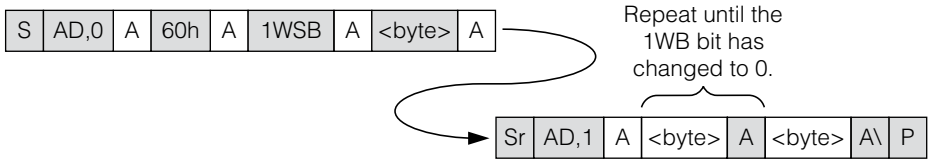
Case A: 1-Wire Idle (1WB = 0), No Busy Polling

S	AD,0	A	60h	A	1WSB	A	<byte>	A	P	(Idle)

S	AD,1	A	<byte>	A\	P

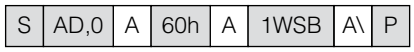
The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire single-bit command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the 1-Wire Master Status register holds the valid result of the 1-Wire Single Bit command.

Case C: 1-Wire Busy (1WB = 1)



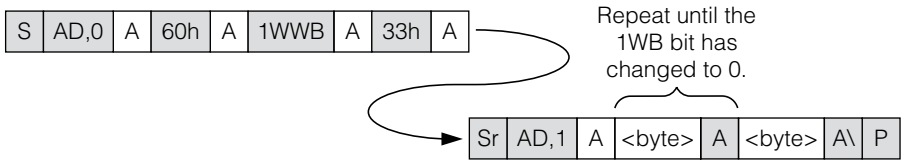
The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

1-Wire Write Byte, e.g., to Send a Command Code to the 1-Wire Line

Case A: 1-Wire idle (1WB = 0), No Busy Polling

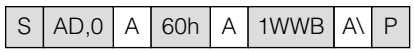
33h is the valid 1-Wire ROM function command for Read ROM. The idle time is needed for the 1-Wire function to complete. There is no data read back from the 1-Wire line with this command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed.



When 1WB has changed from 1 to 0, the 1-Wire Write Byte command is completed.

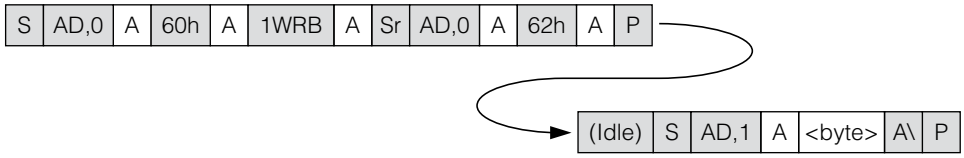
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

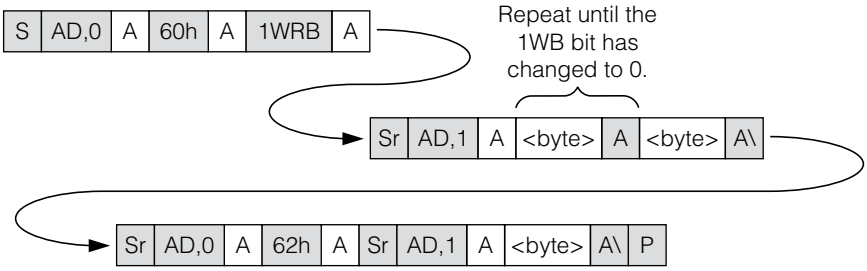
1-Wire Read Byte, e.g., to Read a Byte from the 1-Wire Line

Case A: 1-Wire Idle (1WB = 0), No Busy Polling, Set read address before Idle Time



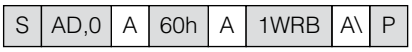
The read address is set to the 1-Wire Read Data register while the 1-Wire Read Byte command is still in progress. Then, after the 1-Wire function is completed, the device is accessed to read the data byte that was obtained from the 1-Wire line.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



Poll the Status register until the 1WB bit has changed from 1 to 0. Then set the read address to the 1-Wire Read Data register and access the device again to read the data byte that was obtained from the 1-Wire line.

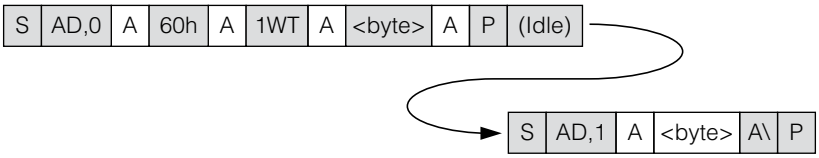
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

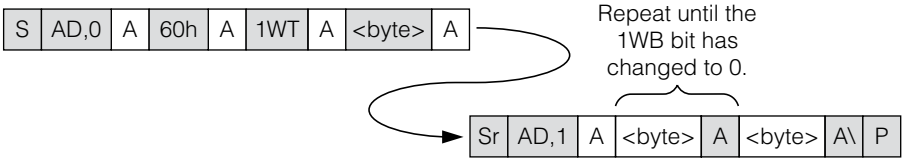
1-Wire Triplet, e.g., to Perform a Search ROM Function on the 1-Wire Line

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



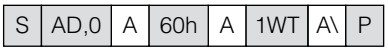
The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Triplet command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the 1-Wire Master Status register holds the valid result of the 1-Wire Triplet command.

Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

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I^2C通信示例(续)

详细信息参见数据资料完整版。

1-Wire Receive Block, e.g., to Read a MAC from the 1-Wire Slave

Case A: 1-Wire Idle (1WB = 0)

S	AD,0	A	60h	A	1WRB	A	<byte>	A	P	(Idle)

The parameter byte is always acknowledged, regardless of its value (is always valid).

Case B: 1-Wire Busy (1WB = 1)

S	AD,0	A	60h	A	1WRB	A\	P

The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

定购信息

器件	温度范围	引脚-封装
DS2465P+	-40°C to +85°C	6 TSOC
DS2465P+T	-40°C to +85°C	6 TSOC (4k pieces)

+表示无铅(Pb)/符合RoHS标准的封装。
T = 卷带包装。

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询china.maximintegrated.com/packages。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
6 TSOC	D6+1	21-0382	90-0321