REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
PAGE																				
REV																				
PAGE	18																			

REV STATUS OF PAGES	**REV**																	
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY MM DD 19-07-24	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, 4-CHANNEL, LOW NOISE, LOW POWER, 24-BIT, SIGMA-DELTA ADC WITH PGA AND REFERENCE, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/19614**
	REV	**PAGE** 1 **OF** 18

AMSC N/A

5962-V102-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7124-4–EP	4-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-153-AD	Thin Shrink Small Outline Package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

AV_{DD} to AV_{SS}	-0.3 V to +3.96 V
IOV_{DD} to DGND	-0.3 V to +3.96 V
IOV_{DD} to AV_{SS}	-0.3 V to +5.94 V
AVV_{SS} to DGND	-1.98 V to +0.3 V
Analog Input Voltage to AV_{SS}	-0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AV_{SS}	-0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	-0.3 V to IOV_{DD} + 0.3 V
Digital Output Voltage to DGND	-0.3 V to IOV_{DD} + 0.3 V
AINx/Digital Input Current	10 mA
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Maximum Junction temperature	150°C
Lead temperature, Soldering Reflow	260°C
ESD Ratings:	
Human Body Model (HBM)	4 kV
Field-Induced Charged Device Model (FICDM)	1250 V
Machine Model	400 V

1.4 Thermal characteristics.

Thermal resistance

Case outline 2/	θ_{JA}	θ_{JC}	Unit
Case X	128	42	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices
JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org)

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ 3/	Limits Min	Typ	Max	Unit
ADC						
Output Data Rate,	fADC					
Low Power Mode			1.17		2400	SPS
Mid Power Mode			2.34		4800	SPS
Full Power Mode			9.38		19200	SPS
No Missing Codes 4/		FS 5/ > 2, sinc 6/ 4 filter	24			Bits
		FS 5/ > 8, sinc 5/ filter	24			
Resolution						
RMS Noise and Update Rates						
Integral Nonlinearity (INL)		Gain = 1 4/	-4	±1	+4	ppm of FSR
		Gain > 1 6/	-15	±2	+15	ppm of FSR
Offset Error 7/						
Before Calibration		Gain = 1 to 8		±15		µV
		Gain = 16 to 128		200/gain		µV
After Internal Calibration/System Calibration				In order of noise		
Offset Error Drift vs. Temperature 8/						
Low Power Mode		Gain = 1 or gain > 16		10		nV/°C
		Gain = 2 to 8		80		nV/°C
		Gain = 16		40		nV/°C
Mid Power Mode		Gain = 1 or gain > 16		10		nV/°C
		Gain = 2 to 8		40		nV/°C
		Gain = 16		20		nV/°C
Full Power Mode				10		nV/°C
Gain Error 7/ 9/						
Before Internal Calibration		Gain = 1, TA = 25°C	−0.0025		+0.0025	%
		Gain > 1		-0.3		%
After Internal Calibration		Gain = 2 to 8, TA = 25°C	−0.016	+0.004	+0.016	%
		Gain = 16 to 128		±0.025		%
After System Calibration				In order of noise		
Gain Error Drift vs. Temperature				1	2	ppm/°C
Power Supply Rejection		AIN = 1 V/gain, external reference				
Low Power Mode			87			dB
		Gain = 2 to 16	96			dB
… Mid Power Mode 4/		Gain = 1 or gain > 16	92			dB
		Gain = 2 to 16	100			dB
Full Power Mode		Gain = 1 or gain > 16	99			dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
ADC – Continued.					
Common-Mode Rejection 10/					
At DC 4/	AIN = 1 V, gain = 1	85	90		dB
	AIN = 1 V/gain, gain 2 or 4	105	115		dB
	AIN = 1 V/gain, gain 2 or 4	102 11/ 4/			dB
	AIN = 1 V/gain, gain ≥ 8	115	120		dB
	AIN = 1 V/gain, gain ≥ 8	105 11/ 4/			dB
Sinc 5/, Sinc 6/ Filter 4/					
At 50 Hz, 60 Hz	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	120			dB
At 50 Hz	50 SPS, 50 Hz ± 1 Hz	120			dB
At 60 Hz	60 SPS, 60 Hz ± 1 Hz	120			dB
Fast Settling Filters 4/					
At 50 Hz	First notch at 50 Hz, 50 Hz ± 1 Hz	115			dB
At 60 Hz	First notch at 60 Hz, 60 Hz ± 1 Hz	115			dB
Post Filters 4/					
At 50 Hz, 60 Hz	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	130			dB
	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	130			dB
Normal Mode Rejection 4/					
Sinc 6/ Filter					
External Clock					
At 50 Hz, 60 Hz	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	120			dB
	50 SPS, REJ60 = 1 12/ , 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	80			dB
At 50 Hz	50 SPS, 50 Hz ± 1 Hz	120			dB
At 60 Hz	60 SPS, 60 Hz ± 1 Hz	120			dB
Internal Clock					
At 50 Hz, 60 Hz	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	98			dB
	50 SPS, REJ6010 = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	66			dB
At 50 Hz	50 SPS, 50 Hz ± 1 Hz	92			dB
At 60 Hz	60 SPS, 60 Hz ± 1 Hz	92			dB
Sinc 5/ Filter					
External Clock					
At 50 Hz, 60 Hz	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	100			dB
	50 SPS, REJ60 = 1 12/ , 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	65			dB
At 50 Hz	50 SPS, 50 Hz ± 1 Hz	100			dB
At 60 Hz	60 SPS, 60 Hz ± 1 Hz	100			dB
Internal Clock					
At 50 Hz, 60 Hz	10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	73			dB
	50 SPS, REJ6010 = 1, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	52			dB
At 50 Hz	50 SPS, 50 Hz ± 1 Hz	68			dB
At 60 Hz	60 SPS, 60 Hz ± 1 Hz	68			dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
ADC – Continued.					
Normal Mode Rejection - Continued 4/					
Fast Settling Filters					
External Clock					
At 50 Hz	First notch at 50 Hz, 50 Hz ± 0.5 Hz	40			dB
At 60 Hz	First notch at 60 Hz, 60 Hz ± 0.5 Hz	40			dB
Internal Clock					
At 50 Hz	First notch at 50 Hz, 50 Hz ± 0.5 Hz	24.5			dB
At 60 Hz	First notch at 60 Hz, 60 Hz ± 0.5 Hz	24.5			dB
Post Filters					
External Clock					
At 50 Hz, 60 Hz	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	86			dB
	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	62			dB
Internal Clock					
At 50 Hz, 60 Hz	20 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	67			dB
	25 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz	50			dB
ANALOG INPUTS 13/					
Differential Input Voltage Ranges 14/	V_{REF} = REFINx(+) − REFINx(−), or internal reference		±VREF/gain		
Absolute A_{IN} Voltage Limits 4/					
Gain = 1 (Unbuffered)		AV_{SS} − 0.05		AV_{DD} + 0.05	V
Gain = 1 (Buffered)		AV_{SS} + 0.1		AV_{DD} − 0.1	V
Gain > 1		AV_{SS} − 0.05		AV_{DD} + 0.05	V
Analog Input Current					
Gain > 1 or Gain = 1 (Buffered)					
Low Power Mode					
Absolute Input Current			±1		nA
Differential Input Current			±0.2		nA
Analog Input Current Drift			25		pA/°C
Mid Power Mode					
Absolute Input Current			±1.2		nA
Differential Input Current			±0.4		nA
Analog Input Current Drift			25		pA/°C
Full Power Mode					
Absolute Input Current			±3.3		nA
Differential Input Current			±1.5		nA
Analog Input Current Drift			25		pA/°C
Gain = 1 (Unbuffered)	Current varies with input voltage				
Absolute Input Current			±2.65		µA/V
Analog Input Current Drift			1.1		nA/V/°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
REFERENCE INPUT					
Internal Reference					
Initial Accuracy	TA = 25°C	2.5 − 0.2%	2.5	2.5 + 0.2%	V
Drift			2	10	ppm/°C
Output Current				10	mA
Load Regulation			50		μV/mA
Power Supply Rejection			85		dB
External Reference					
External REFIN Voltage 4/	REFIN = REFINx(+) − REFINx(−)	0.5	2.5	AV_{DD}	V
Absolute REFIN Voltage Limits 4/	Unbuffered	AV_{SS} − 0.05		AV_{DD} + 0.05	V
	Buffered	AV_{SS} + 0.1		AV_{DD} − 0.1	V
Reference Input Current					
Buffered					
Low Power Mode					
Absolute Input Current			±0.5		nA
Reference Input Current Drift			10		pA/°C
Mid Power Mode					
Absolute Input Current			±1		nA
Reference Input Current Drift			10		pA/°C
Full Power Mode					
Absolute Input Current			±3		nA
Reference Input Current Drift			10		pA/°C
Unbuffered					
Absolute Input Current			±12		nA
Reference Input Current Drift			6		pA/°C
Normal Mode Rejection	Same as for analog inputs				
Common-Mode Rejection			100		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
EXCITATION CURRENT SOURCES (IOUT0/IOUT1) (Available on any analog input pin)					
Output Current			50/100/250/ 500/750/1000		µA
Initial Tolerance			±4		%
Drift			50		ppm/°C
Current Matching	Matching between IOUT0 and IOUT1, V_{OUT} = 0 V		±0.5		%
Drift Matching 4/			5	30	ppm/°C
Line Regulation (AVDD)	AVDD = 3 V ± 5%		2		%/V
Load Regulation			0.2		%/V
Output Compliance 4/	50 µA/100 µA/250 µA/500 µA current sources, 2% accuracy	AV_{SS} − 0.05		AV_{DD} − 0.37	V
	750 µA and 1000 µA current sources, 2% accuracy	AV_{SS} − 0.05		AV_{DD} − 0.48	V
BIAS VOLTAGE (V_{BIAS}) GENERATOR (Available on any analog input pin)					
V_{BIAS}			AV_{SS} + (AV_{DD} − AV_{SS})/2		V
V_{BIAS} Generator Start-Up Time	Dependent on the capacitance connected to AI		6.7		µs/nF
TEMPERATURE SENSOR					
Accuracy			±0.5		°C
Sensitivity			13,584		Codes/°C
LOW-SIDE POWER SWITCH					
On Resistance			7	10	Ω
Allowable Current 4/	Continuous current			30	mA
BURNOUT CURRENTS					
A_{IN} Current	Analog inputs must be buffered		0.5/2/4		µA
DIGITAL OUTPUTS (P1 AND P2)					
Output Voltage					
High, V_{OH}	I_{SOURCE} = 100 µA	AV_{DD} − 0.6			V
Low, V_{OL}	I_{SINK} = 100 µA			0.4	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
DIAGNOSTICS					
Power Supply Monitor Detect Level					
Analog Low Dropout Regulator (ALDO)	$AV_{DD} - AV_{SS} \geq 2.7$ V			1.6	V
Digital LDO (DLDO)	$IOV_{DD} \geq 1.75$ V			1.55	V
Reference Detect Level	REF_DET_ERR bit active if VREF < 0.7 V	0.7		1	V
AINM/AINP Overvoltage Detect Level		AV_{DD} + 0.04			V
AINM/AINP Undervoltage Detect Level				AV_{SS} − 0.04	V
INTERNAL/EXTERNAL CLOCK					
Internal Clock					
Frequency		614.4 − 5%	614.4	614.4 + 5%	kHz
Duty Cycle			50:50		%
External Clock					
Frequency	Internal divide by 4		2.4576		MHz
Duty Cycle			45:55 to 55:45		%
LOGIC INPUTS 4/					
Input Voltage					
Low, V_{INL}	1.65 V ≤ IOV_{DD} < 1.9 V			0.3 × IOV_{DD}	V
	1.9 V ≤ IOV_{DD} < 2.3 V			0.35 × IOV_{DD}	V
	2.3 V ≤ IOV_{DD} ≤ 3.6 V			0.7	V
High, V_{INH}	1.65 V ≤ IOV_{DD} < 1.9 V	0.7 × IOV_{DD}			V
	1.9 V ≤ IOV_{DD} < 2.3 V	0.65 × IOV_{DD}			V
	2.3 V ≤ IOV_{DD} ≤ 2.7 V	1.7			V
	2.7 V ≤ IOV_{DD} ≤ 3.6 V	2			V
Hysteresis	1.65 V ≤ IOV_{DD} ≤ 3.6 V	0.2		0.6	V
Input Currents	VI_N = IOV_{DD} or GND	-1		+1	µA
Input Capacitance	All digital inputs		10		pF
LOGIC OUTPUTS (INCLUDING CLK)					
Output Voltage 4/					
High, V_{OH}	I_{SOURCE} = 100 µA	IOV_{DD} − 0.35			V
Low, V_{OL}	I_{SINK} = 100 µA			0.4	V
Floating State Leakage Current		-1		+1	µA
Floating State Output Capacitance			10		pF
Data Output Coding			Offset binary		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
SYSTEM CALIBRATION 4,					
Calibration Limit Full Scale (FS) Zero Scale		 −1.05 × FS		 1.05 × FS	 V V
Input Span		0.8 × FS		2.1 × FS	V
POWER SUPPLY VOLTAGES FOR ALL POWER MODES					
AVDD to AVSS Low Power Mode Mid Power Mode Full Power Mode		 2.7 2.7 2.9		 3.6 3.6 3.6	 V V V
IOV_{DD} to GND		1.65		3.6	V
AV_{SS} to GND		-1.8		0	V
IOV_{DD} to AV_{SS}				5.4	V
POWER SUPPLY CURRENTS 13/ 15/					
I_{AVDD}, External Reference Low Power Mode Gain = 1[2] Gain = 1 I_{AVDD} Increase per AINx Buffer 4/ ……Gain = 2 to 8 Gain = 16 to 128 IA_{VDD} Increase per Reference Buffer 4/ Mid Power Mode Gain = 1[2] Gain = 1 I_{AVDD} Increase per AINx Buffer 4/ ……Gain = 2 to 8 Gain = 16 to 128 IA_{VDD} Increase per Reference Buffer 4/ Full Power Mode Gain = 1[2] Gain = 1 I_{AVDD} Increase per AINx Buffer 4/ ……Gain = 2 to 8 Gain = 16 to 128 IA_{VDD} Increase per Reference Buffer 4/ I_{AVDD} Increase Due to Internal Reference 4/ Due to V_{BIAS} 4/ Due to Diagnostics 4/	 All buffers off All gains All buffers off All gains All buffers off All gains Independent of power mode; the reference buffers are not required when using this reference Independent of power mode		 125 15 205 235 10 150 30 275 330 20 315 90 660 875 85 50 15 4	 140 25 250 300 20 170 40 345 430 30 350 135 830 1200 120 70 20 5	 µA µA µA µA µA µA µA µA µA µA µA µA µA µA µA µA µA µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions	Limits			Unit
		Min	Typ	Max	
POWER SUPPLY CURRENTS - Continued 13/ 15/					
I_{AVDD}, External Reference					
I_{IOVDD}					
Low Power Mode			20	35	µA
Mid Power Mode			25	40	µA
Full Power Mode			55	80	µA
POWER-DOWN CURRENTS 15/ (Independent of power mode)					
Standby Current					
I_{AVDD}	LDOs on only		7	15	µA
I_{IOVDD}			8	20	µA
Power-Down Current					
I_{AVDD}			1	3	µA
I_{IOVDD}			1	2	µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ AV_{DD} = 2.9 V to 3.6 V (full power mode), 2.7 V to 3.6 V (mid and low power mode), IOV_{DD} = 1.65 V to 3.6 V, A_{VSS} = DGND = 0 V, REFINx(+) = 2.5 V, REFINx(−) = AV_{SS}, master clock = 614.4 kHz, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

3/ Temperature range = −55°C to +125°C.

4/ These specifications are not production tested but are supported by characterization data at the initial product release.

5/ FS is the decimal equivalent of the FS[10:0] bits in the filter registers.

6/ The integral nonlinearity is production tested in full power mode only. For other power modes, the specification is supported by characterization data at the initial product release.

7/ Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full- scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.

8/ Recalibration at any temperature removes these errors.

9/ Gain error applies to both positive and negative full-scale. A factory calibration is performed at gain = 1, TA = 25°C.

10/ When gain > 1, the common-mode voltage is between (AVSS + 0.1 + 0.5/gain) and (AVDD − 0.1 − 0.5/gain).

11/ Specification is for a wider common-mode voltage between (AVSS − 0.05 + 0.5/gain) and (AVDD − 0.1 − 0.5/gain).

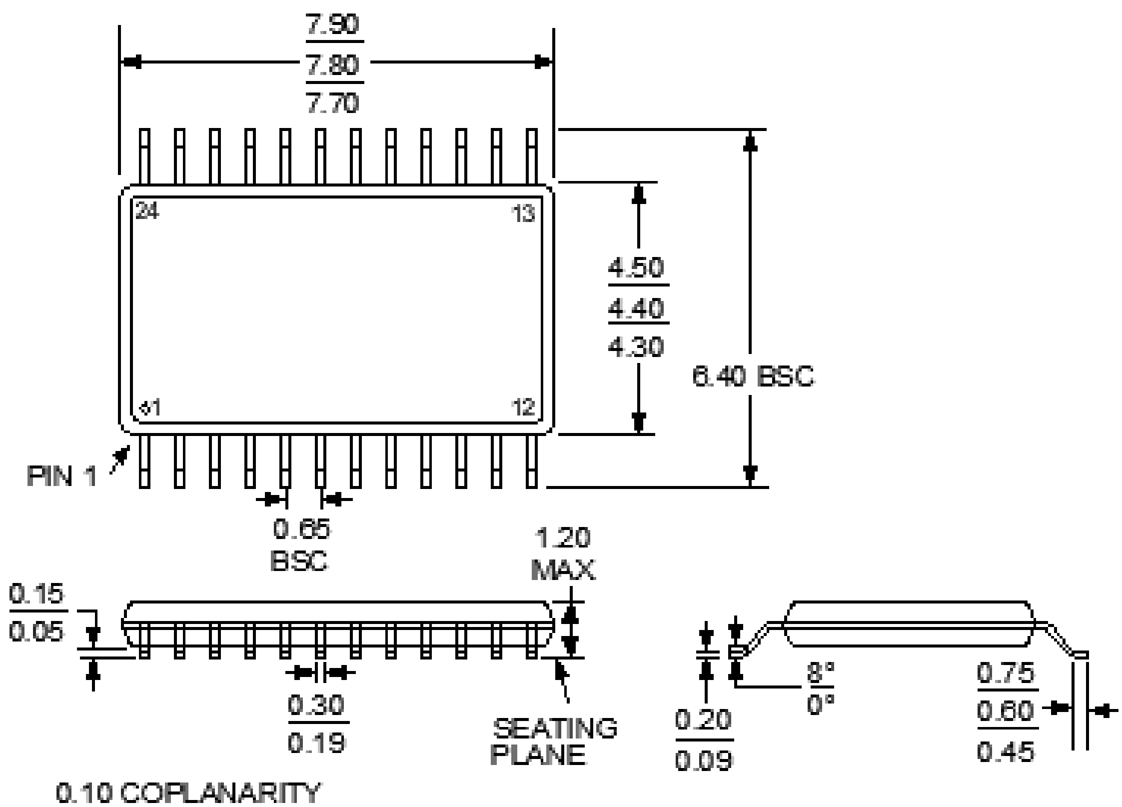
12/ REJ60 is a bit in the filter registers. When the first notch of the sinc filter is at 50 Hz, a notch is placed at 60 Hz when REJ60 is set to 1. This gives simultaneous 50 Hz and 60 Hz rejection.

13/ When the gain is greater than 1, the analog input buffers are enabled automatically. The buffers can only be disabled when the gain equals 1.

14/ When V_{REF} = (AV_{DD} − AV_{SS}), the typical differential input equals 0.92 × V_{REF}/gain for the low and mid power modes and 0.86 × V_{REF}/gain for full power mode when gain > 1.

15/ The digital inputs are equal to IOV_{DD} or DGND with excitation currents and bias voltage generator disabled.

Case X



NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AD.

FIGURE 1. Case outline.

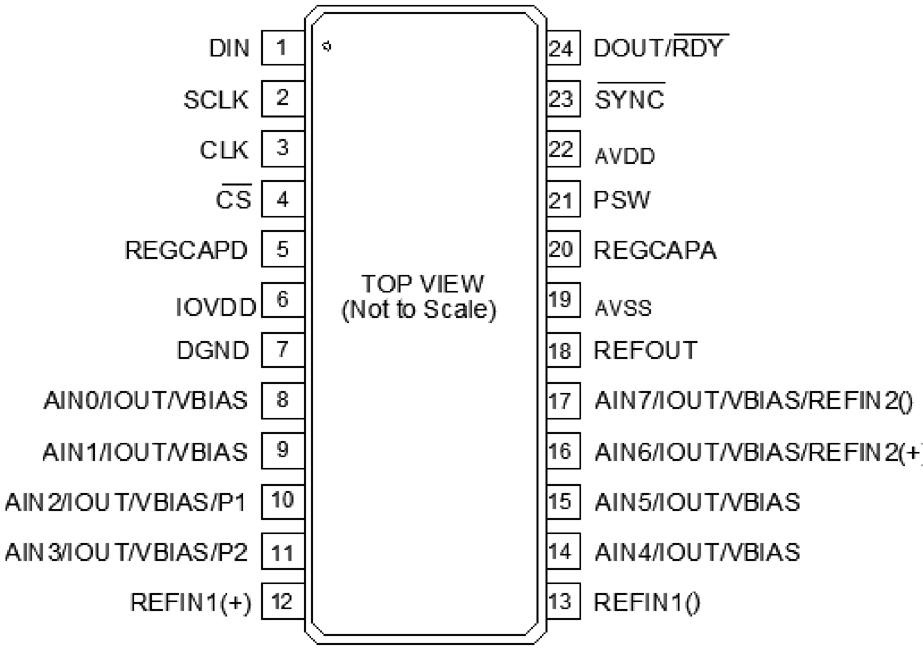


FIGURE 2. Terminal connections.

Terminal No.	Mnemonic	Description
1	DN	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers within the ADC, with the register selection bits of the communications register identifying the appropriate register
2	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK pin has a Schmitt- triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
3	CLK	Clock Input/Clock Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. This allows several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed.
4	$\overline{CS}$	Chip Select Input. This is an active low logic input that selects the ADC. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low if the serial peripheral interface (SPI) diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device.
5	REGCAPD	Digital LDO Regulator Output. Decouple this pin to DGND with a 0.1 μF capacitor.

FIGURE 3. Terminal function.

Terminal No.	Mnemonic	Description
6	IOV_{DD}	Serial Interface Supply Voltage, 1.65 V to 3.6 V. IOVDD is independent of AVDD. Therefore, the serial interface can operate at 1.65 V with AVDD at 3.6 V, for example.
7	DGND	Digital Ground Reference Point.
8	AIN0/IOUT/VBIAS	Analog Input 0/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
9	AIN1/IOUT/VBIAS	Analog Input 1/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
10	AIN2/IOUT/VBIAS/P1	Analog Input 2/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 1. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
11	AIN3/IOUT/VBIAS/P2	Analog Input 3/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 2. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin can also be configured as a general-purpose output bit, referenced between AV_{SS} and AV_{DD}.
12	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The nominal reference voltage (REFIN1(+) − REFIN1(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AV_{DD}.
13	REFIN1(−)	Negative Reference Input. This reference input can be anywhere between AV_{SS} and AV_{DD} – 0.5 V.
14	AIN4/IOUT/VBIAS	Analog Input 4/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.
15	AIN5/IOUT/VBIAS	Analog Input 5/Output of Internal Excitation Current Source/Bias Voltage. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin.

FIGURE 3. Terminal function – Continued..

Terminal No.	Mnemonic	Description
16	AIN6/IOUT/VBIAS/ REFIN2(+)	Analog Input 6/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as a positive reference input for REFIN2(±). REFIN2(+) can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AV_{DD}.
17	AIN7/IOUT/VBIAS/ REFIN2(−)	Analog Input 7/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. This input pin is configured via the configuration registers to be the positive or negative terminal of a differential or pseudo differential input. Alternatively, the internal programmable excitation current source can be made available at this pin. Either IOUT0 or IOUT1 can be switched to this output. A bias voltage midway between the analog power supply rails can be generated at this pin. This pin also functions as the negative reference input for REFIN2(±). This reference input can be anywhere between AV_{SS} and AV_{DD} – 0.5 V.
18	REFOUT	Internal Reference Output. The buffered output of the internal 2.5 V voltage reference is available on this pin.
19	AV_{SS}	Analog Supply Voltage. The voltage on AV_{DD} is referenced to AV_{SS}. The differential between AV_{DD} and AV_{SS} must be between 2.7 V and 3.6 V in mid or low power mode and between 2.9 V and 3.6 V in full power mode. AV_{SS} can be taken below 0 V to provide a dual power supply to the AD7124-4-EP. For example, AV_{SS} can be tied to −1.8 V and AV_{DD} can be tied to +1.8 V, providing a ±1.8 V supply to the ADC.
20	REGCAPA	Analog LDO Regulator Output. Decouple this pin to AV_{SS} with a 0.1 µF capacitor.
21	PSW	Low-Side Power Switch to AV_{SS}.
22	AV_{DD}	Analog Supply Voltage, Relative to AV_{SS}
23	$\overline{SYNC}$	Synchronization Input. This pin is a logic input that allows synchronization of the digital filters and analog modulators when using a number of AD7124-4-EP devices. When $\overline{SYNC}$ is low, the nodes of the digital filter, the filter control logic, and the calibration control logic are reset, and the analog modulator is held in a reset state. $\overline{SYNC}$ does not affect the digital interface but does reset $\overline{RDY}$ to a high state if it is low.
24	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. When $\overline{CS}$ is low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.

FIGURE 3. Terminal function – Continued..

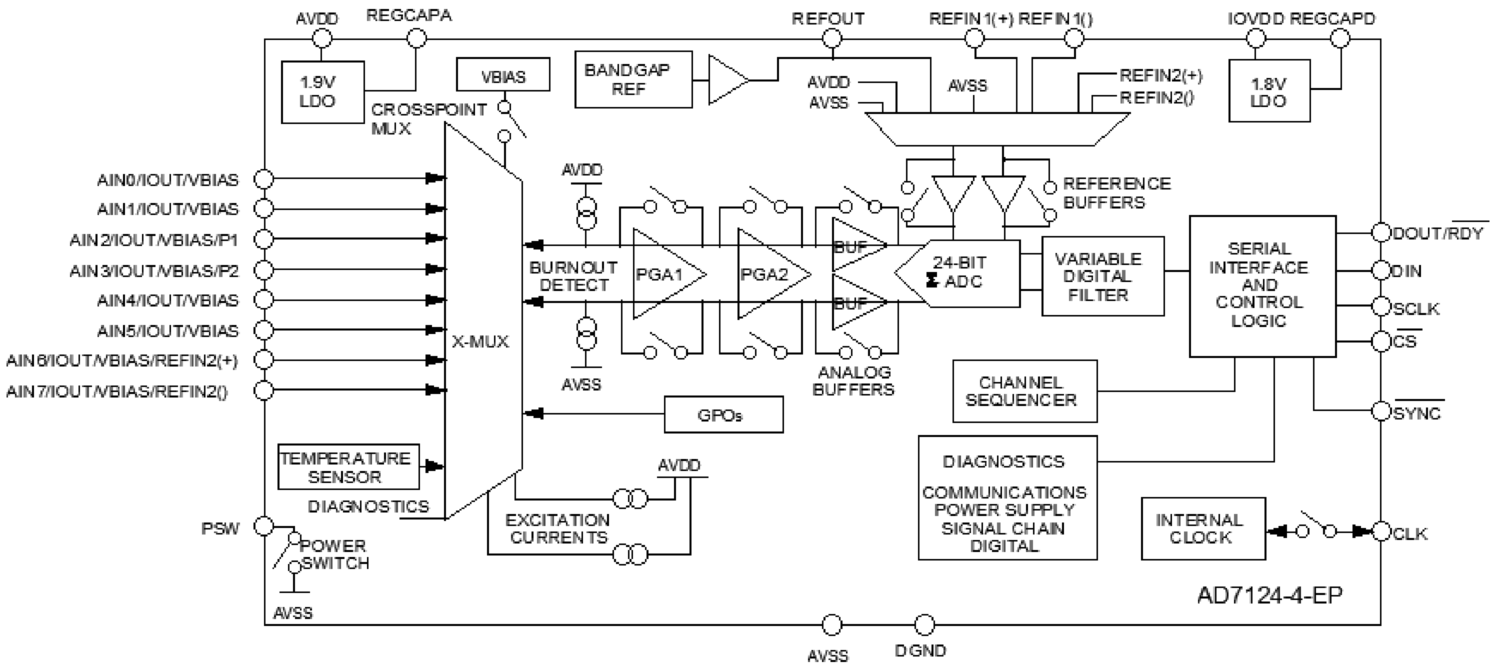


FIGURE 4. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/19614-01XE	24355	Tube units = 62	AD7124-4TRUZ-EP
		Reel units = 1000	AD7124-4TRUZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106