REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 19-05-24	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, 5.7 kV RMS, SIGNAL ISOLATED, BASIC CAN FD TRANSCEIVER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/19605**
	REV	**PAGE** 1 **OF** 16

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AMSC N/A

5962-V050-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 5.7 kV rms, signal isolated basic controlled area network flexible data rate (CAN FD) transceiver, microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/19605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADM3050E-EP	5.7 kV rms, signal isolated basic CAN FD transceiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-013-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD1}/V_{DD2}) ..... -0.5 V to +6 V
Logic side input/output: TXD, RXD ..... -0.5 V to V_{DD1} + 0.5 V
CANH, CANL ..... -40 V to +40 V
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Junction temperature range (TJ) ..... 150°C maximum
Electrostatic discharge (ESD) rating:
IEC 61000-4-2, CANH/CANL
Across isolation barrier with respect to GND_1 ..... ±8 kV
Contact discharge with respect to to GND_2 ..... ±8 kV typical
Air discharge with respect to GND_2 ..... ±15 kV
Human body model (HDM) all pins, 1.5 kΩ, 100 pF ..... ±4 kV
Moisture sensitivity level (MSL) MSL3
Thermal resistance, junction to ambient (θ_{JA}) ..... 60°C/W

1.4 Recommended operating conditions. 3/

Supply voltage range:
(V_{DD1}) ..... 1.7 V to 5.5 V
(V_{DD2}) ..... 4.5 V to 5.5 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Package characteristics.

Resistance (input to output) (R_{I-O}) ..... 10^{13} Ω typical 4/
Capacitance (input to output) (C_{I-O}) with f = 1 MHz ..... 1.1 pF typical 4/
Input capacitance (C_I) ..... 4.0 pF typical 5/

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise specified, pin voltage with respect to GND_1/GND_2 are on the same side.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ The device is considered a 2-terminal device: pin 1 through pin 8 are shorted together, and pin 9 through pin 16 are shorted together.
5/ Input capacitance is from any input data pin to ground.

2. APPLICABLE DOCUMENTS

International Electrotechnical Commission

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) - Part 4-2:
Testing and measurement techniques - Electrostatic discharge immunity test

(Copies of these documents are available online at https://www.iec.ch.)

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4 through 8.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Supply current							
Bus side	I_{DD2}						
Recessive state		TXD high, load resistance (R_L) = 60 Ω	+25°C	01	5.3 typical		mA
			-55°C to +125°C			7	
Dominant state		Limited by transmit dominant timeout (t_{DT}), R_L = 60 Ω	+25°C	01	63 typical		mA
			-55°C to +125°C			75	
		Limited by (t_{DT}), R_L = 60 Ω, 4.75 V ≤ V_{DD2} ≤ 5.25 V	-55°C to +125°C			73	
70% dominant / 30% recessive		1 Mbps, worst case, R_L = 60 Ω	+25°C	01	45 typical		mA
			-55°C to +125°C			58	
		5 Mbps, worst case, R_L = 60 Ω	+25°C		49 typical		
			-55°C to +125°C			60	
		12 Mbps, worst case, R_L = 60 Ω	+25°C		58 typical		
			-55°C to +125°C			65	
Logic side icoupler current	I_{DD1}	TXD high, low, or switching	-55°C to +125°C	01		5.5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver							
Differential outputs		See figure 4					
Recessive state voltage.		TXD high, R_L and common mode filter capacitor (C_F) open					
CANH, CANL voltage	V_{CANL}, V_{CANH}		-55°C to +125°C	01	2.0	3.0	V
Differential output voltage	V_{OD}		-55°C to +125°C	01	-500	+50	mV
Dominant state voltage.		TXD low, C_F open					
CANH voltage	V_{CANH}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +125°C	01	2.75	4.5	V
CANL voltage	V_{CANL}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +125°C	01	0.5	2.0	V
Differential output voltage	V_{OD}	50 Ω ≤ R_L ≤ 65 Ω	-55°C to +125°C	01	1.5	3.0	V
		45 Ω ≤ R_L ≤ 70 Ω			1.4	3.3	
		R_L = 2240 Ω			1.5	5.0	
Output symmetry (V_{DD2} – V_{CANH} to V_{CANL})	V_{SYM}	R_L = 60 Ω, C_F = 4.7 nF	-55°C to +125°C	01	-0.55	+0.55	V
Short circuit current	$\|I_{SC}\|$	R_L open					
Absolute CANH		V_{CANH} = -3 V	-55°C to +125°C	01		115	mA
Absolute CANL		V_{CANL} = 18 V	-55°C to +125°C	01		115	mA
Steady state CANH		V_{CANH} = -24 V	-55°C to +125°C	01		115	mA
Steady state CANL		V_{CANL} = 24 V	-55°C to +125°C	01		115	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver - continued							
Logic inputs (TXD)							
Input voltage, high	V_{IH}		-55°C to +125°C	01	0.65 x V_{DD1}		V
Input voltage, low	V_{IL}		-55°C to +125°C	01		0.35 x V_{DD1}	V
Complementary metal oxide semiconductor (CMOS) logic input currents	$\|I_{IH}\|$, $\|I_{IL}\|$	Input high or low	-55°C to +125°C	01		10	µA
Receiver							
Differential inputs							
Differential input voltage range	V_{ID}	RXD capacitance (C_{RXD}) open, see figure 5, -25 V < V_{CANL}, V_{CANH} < +25 V					
Recessive			-55°C to +125°C	01	-1.0	+0.5	V
Dominant			-55°C to +125°C	01	0.9	5.0	V
Input voltage hysteresis	V_{HYS}		+25°C	01	150 typical		mV
Unpowered input leakage current	$\|I_{IN(OFF)}\|$	V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V	-55°C to +125°C	01		10	µA
Input resistance, CANH, CANL	R_{INH}, R_{INL}		-55°C to +125°C	01	6	25	kΩ
Input resistance, differential	R_{DIFF}		-55°C to +125°C	01	20	100	kΩ
Input resistance, matching	m_R	$m_R = 2 \times (R_{INH} - R_{INL}) / (R_{INH} + R_{INL})$	-55°C to +125°C	01	-0.03	+0.03	Ω/Ω
Input capacitance, CANH, CANL	C_{INH}, CR_{INL}		+25°C	01	35 typical		pF
Differential input capacitance	C_{DIFF}		+25°C	01	12 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver – continued.							
Logic outputs (RXD)							
Output voltage , low	V_{OL}	Output impedance (I_{OUT}) = 2 mA	+25°C	01	0.2 typical		V
			-55°C to +125°			0.4	
Output voltage, high RXD	V_{OH}	I_{OUT} = -2 mA	-55°C to +125°C	01	V_{DD1} – 0.2		V
Short circuit current RXD	I_{OS}	Output voltage (V_{OUT}) = GND_1 or V_{DD1}	-55°C to +125°C	01	7	85	mA
Common mode transient immunity. 3/ Common mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V							
Input high, recessive	$\|CM_H\|$	Input voltage (V_{IN}) = V_{DD1}(TXD) or CANH/CANL recessive	+25°C	01	100 typical		kV/μs
			-55°C to +125°		75		
Input low, dominant	$\|CM_L\|$	V_{IN} = 0 V (TXD) or CANH/CANL dominant	+25°C	01	100 typical		kV/μs
			-55°C to +125°		75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications							
Driver	See figure 4 and figure 6, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, load capacitance (C_L) = 100 pF						
Maximum data rate			-55°C to +125°	01	12		Mbps
Propagation delay from TXD to bus (Recessive to Dominant)	t_{TXD_DOM}		+25°C	01	35 typical		ns
			-55°C to +125°			60	
Propagation delay from TXD to bus (Dominant to Recessive)	t_{TXD_REC}		+25°C	01	45 typical		ns
			-55°C to +1205°			70	
Transmit dominant timeout	t_{DT}	TXD low, see figure 7	-55°C to +125°	01	1175	4000	µs
Receiver	See figure 6 and figure 8, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF						
Falling edge loop propagation delay (TXD to RXD)	t_{LOOP_FALL}		-55°C to +125°	01		145	ns
Falling edge loop propagation delay (TXD to RXD)	t_{LOOP_RISE}		-55°C to +125°	01		145	ns
Loop delay symmetry (minimum recessive bit width)	t_{BIT_RXD}	2 Mbps, t_{BIT_TXD} = 500 ns	-55°C to +125°	01	450	550	ns
		5 Mbps, t_{BIT_TXD} = 200 ns			160	220	
		8 Mbps, t_{BIT_TXD} = 125 ns			85	140	
		12 Mbps, t_{BIT_TXD} = 83.3 ns			50	91.6	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, all voltages are relative to their respective ground. 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −55°C ≤ T_A ≤ +125°C, and STBY low. Unless otherwise specified, typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C.

3/ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL recessive, or RXD ≥ V_{DD1} − 0.2 V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Case X

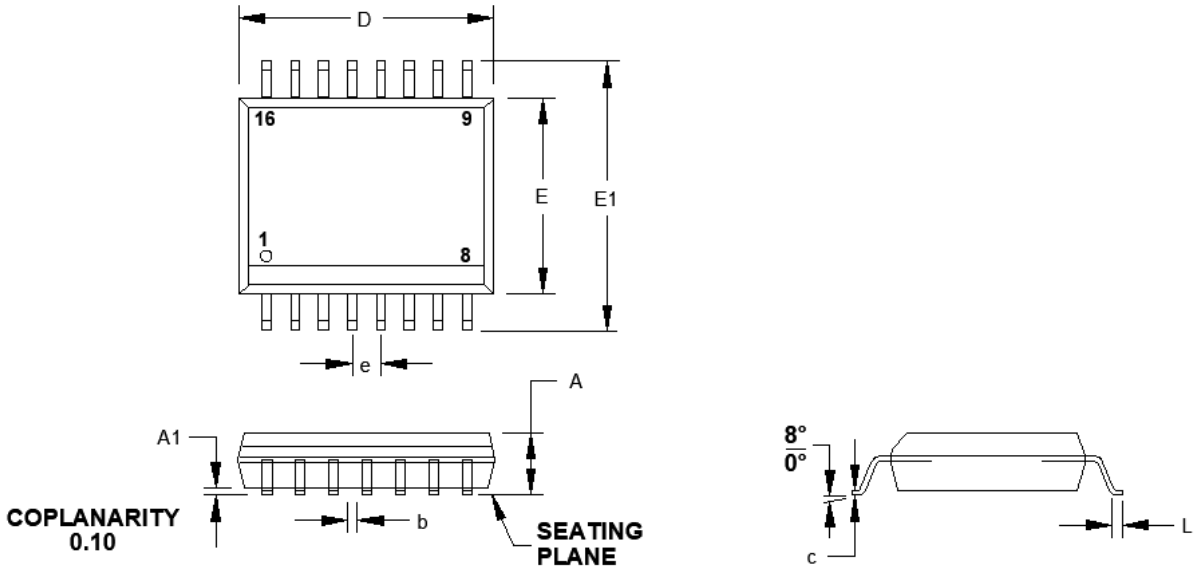

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.0925	.1043	2.35	2.65
A1	.0039	.0118	0.10	0.30
b	.0122	.0201	0.31	0.51
c	.0079	.0130	0.20	0.33
D	.3976	.4134	10.10	10.50
E	.2913	.2992	7.40	7.60
E1	.3937	.4193	10.00	10.65
e	.0500 BSC		1.27 BSC	
L	.0157	.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-013-AA.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD1}	Power supply, logic side, 1.7 V to 5.5 V. This pin requires 0.1 μF decoupling capacitor.
2	GND1	Ground, logic side.
3	RXD	Receiver output data
4	NC	No connect. No internal connection to integrated circuit (IC).
5	NC	No connect. No internal connection to integrated circuit (IC).
6	TXD	Driver input data.
7	GND_1	Ground, logic side.
8	GND_1	Ground, logic side.
9	GND_2	Ground, bus side.
10	GND_2	Ground, bus side.
11	NC	No connect. No internal connection to integrated circuit (IC).
12	CANL	CAN low input and output.
13	CANH	CAN high input and output.
14	NC	No connect. No internal connection to integrated circuit (IC).
15	GND_2	Ground, bus side.
16	VDD_2	Power supply, bus side, 4.5 V to 5.5 V. This pin requires 0.1 μF decoupling capacitor.

FIGURE 2. Terminal connections.

V_{DD1}	V_{DD2}	TXD	Mode	RXD	CANH/CANL
On	On	Low	Normal	Low	Dominant (limited by t_{DT})
On	On	High	Normal	High per bus	Recessive and set by bus
Off	On	Don't care	Normal	Indeterminate	Recessive and set by bus
On	Off	Don't care	Transceiver off	High	High-Z

FIGURE 3. Truth table.

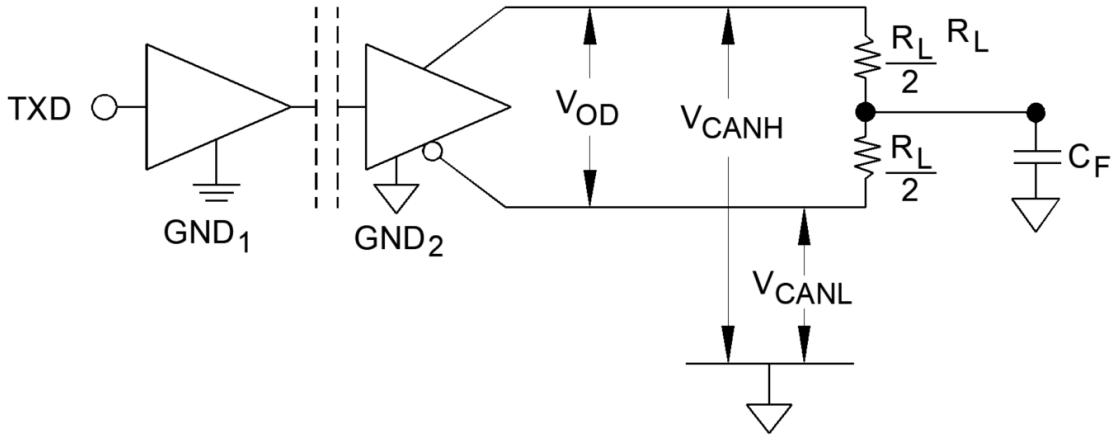

FIGURE 4. Driver voltage measurement.

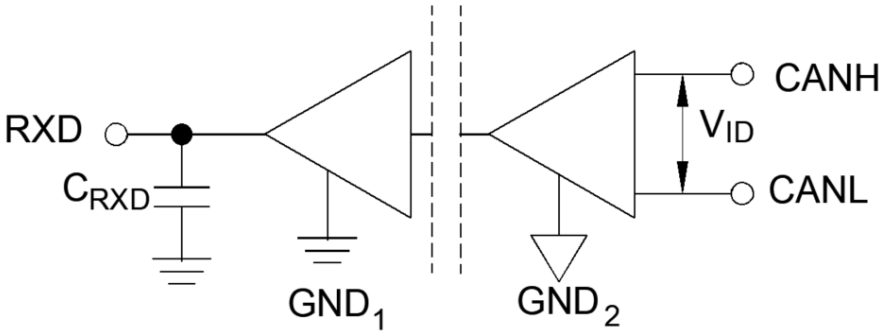

FIGURE 5. Receiver voltage measurement.

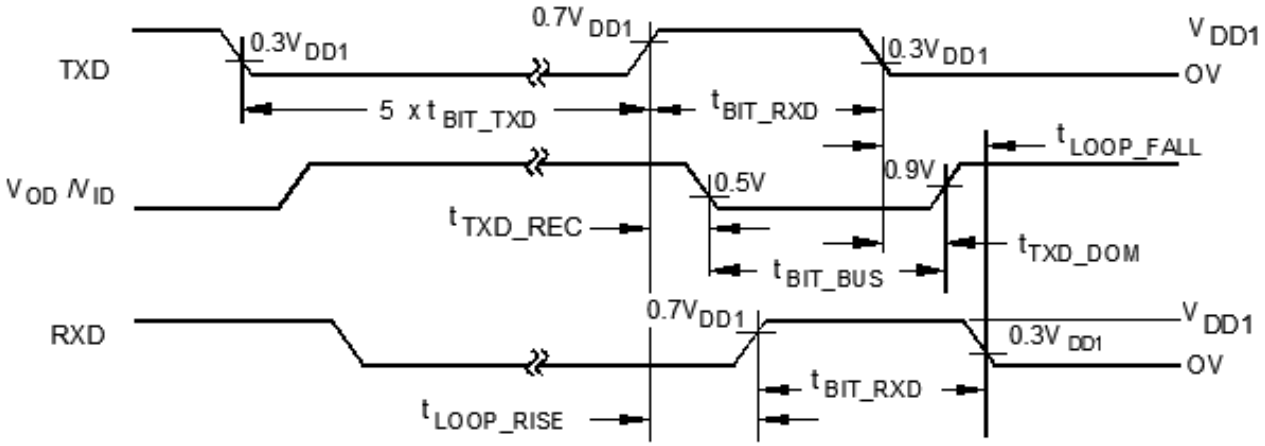

FIGURE 6. Transceiver timing diagram.

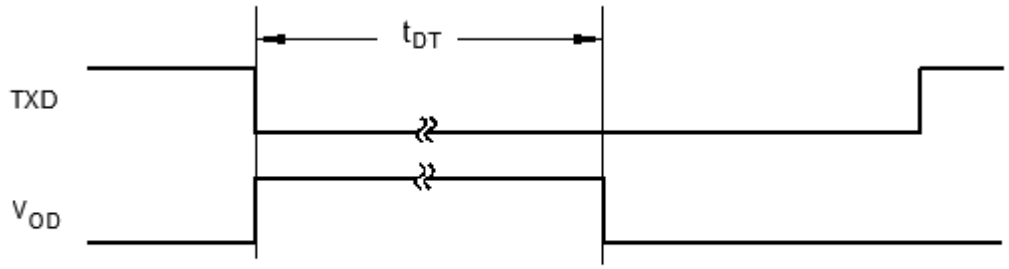

FIGURE 7. Dominant timeout tDT.

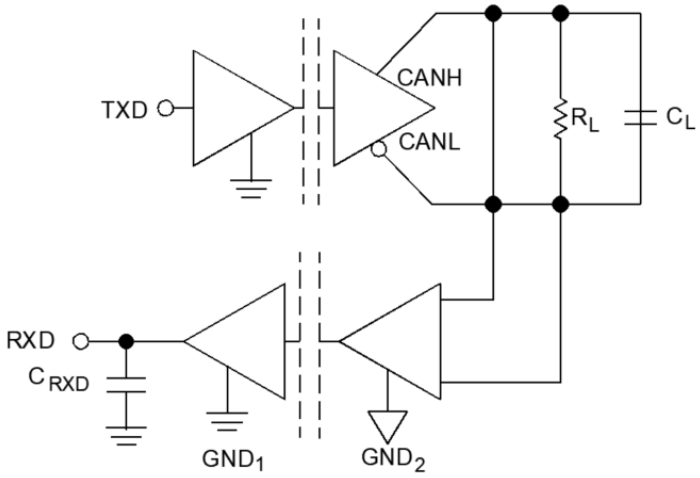

FIGURE 8. Switching characteristics measurements.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/19605-01XE	24355	Tube, 47 units	ADM3050ETRWZ-EP
	24355	Reel, 1000 units	ADM3050ETRWZ-EP-RL

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Chelmsford, MA 01824