MAX25200

36V HV Automotive Boost/SEPIC/Flyback Controller

General Description

The MAX25200 is a high-performance, current-mode PWM controller with 1.5µA (typ) shutdown current for boost converters with a wide input voltage range. The 4.5V to 36V input operating voltage range makes these devices ideal in automotive applications, such as front-end preboost or general-purpose SEPIC or flyback power supplies. An internal low-dropout regulator with a 5V output voltage enables the MAX25200 to operate directly from an automotive battery input. The input operating range can be extended to as low as 1.8V after startup.

The MAX25200's switching frequency operation (up to 2.2MHz) reduces output ripple, avoids AM band interference, and allows for the use of smaller external components. The switching frequency is resistor adjustable from 220kHz to 2.2MHz; Alternatively, the frequency can be synchronized to an external clock. A spread spectrum option is available to improve system EMI performance.

The device features a power-OK monitor and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX25200 operates over the -40°C to +125°C automotive temperature range.

Applications

Infotainment Systems

Cluster Systems

E-call

Benefits and Features

● Meets Stringent OEM Module Power Consumption and Performance Specifications

- 20µA Quiescent Current in Skip Mode
- ±1.5% FB Voltage Accuracy
- Output Voltage Range: Fixed or Adjustable Between 3.5V and 60V

● Enables Crank-Ready Designs

- Operates Down to 1.8V after Startup
- Wide Input Supply Range from 4.5V to 36V

● EMI Reduction Features Reduce Interference with Sensitive Radio Bands without Sacrificing Wide Input Voltage Range

- Spread-Spectrum Option
- Frequency-Synchronization Input
- Resistor-Programmable Frequency Between 220kHz and 2.2MHz

● Integration and Thermally Enhanced Packages Save Board Space and Cost

- Current-Mode Controllers with Forced-Continuous and Skip Modes
- Thermally Enhanced 16-Pin TQFN-EP Package

● Protection Features Improve System Reliability

- Supply Undervoltage Lockout
- Overtemperature and Short-Circuit Protection

Ordering Information appears at end of data sheet.

19-100635; Rev 1; 1/20

ANALOG DEVICES

Simplified Block Diagram

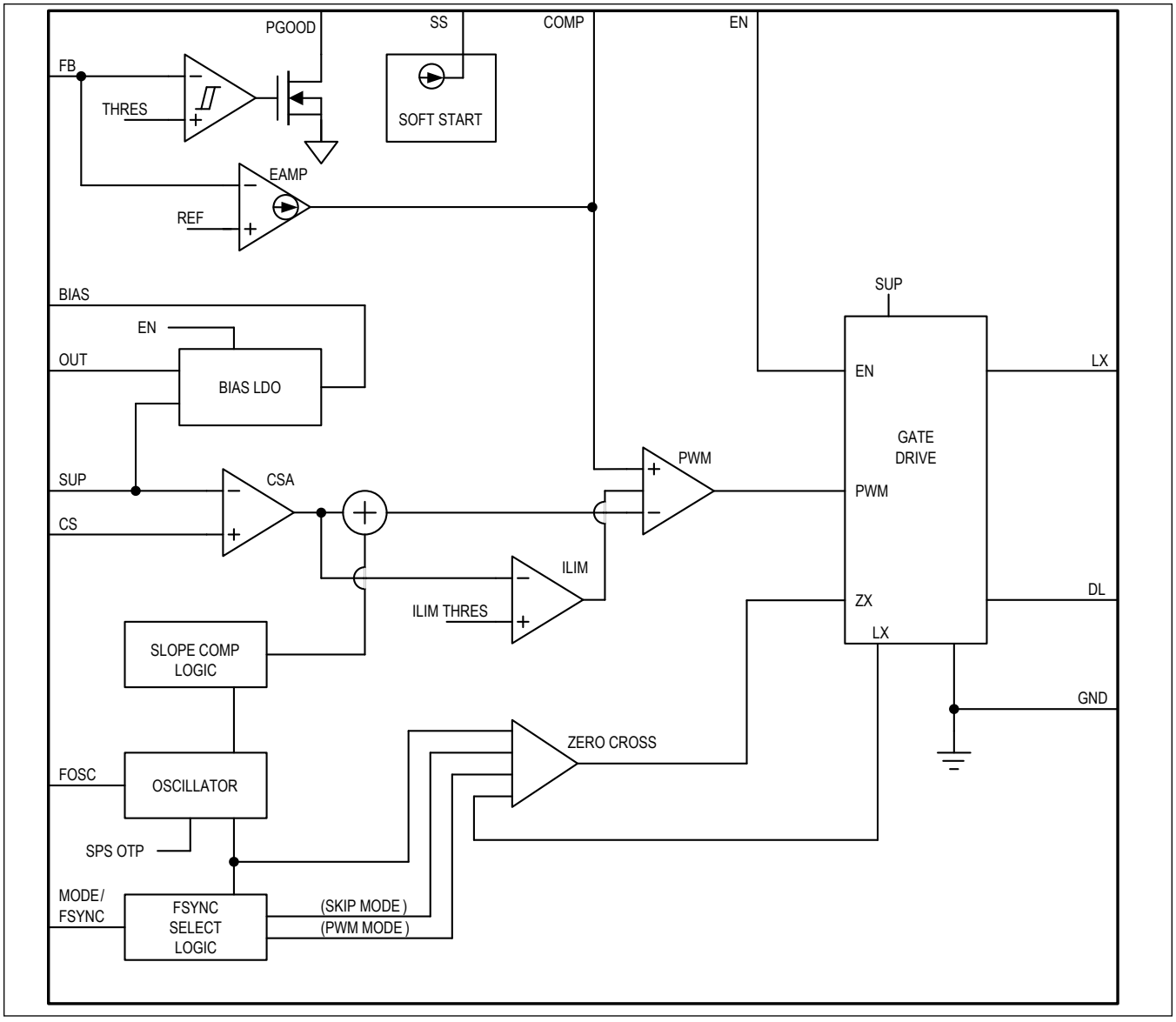


TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Simplified Block Diagram . . . 2
Absolute Maximum Ratings . . . 6
Recommended Operating Conditions . . . 6
Package Information . . . 6
TQFN . . . 6
Electrical Characteristics . . . 6
Typical Operating Characteristics . . . 9
Pin Configuration . . . 13
MAX25200 . . . 13
Pin Description . . . 13
Detailed Description . . . 15
Current-Mode Control Loop . . . 15
Fixed 5V Linear Regulator (BIAS) . . . 15
Startup Operation/UVLO/EN . . . 15
Soft-Start . . . 15
Oscillator Frequency/External Synchronization . . . 15
Light-Load Efficiency Skip Mode . . . 16
Forced-PWM Mode . . . 16
Forced-PWM Mode . . . 16
Spread Spectrum . . . 16
MOSFET Driver (DL) . . . 16
Current Limiting and Current Sense Inputs (SUP and CS) . . . 16
Voltage Monitoring (PGOOD) . . . 17
Protection Features . . . 17
Overcurrent Protection . . . 17
Thermal Overload Protection . . . 17
Slope Compensation . . . 17
Applications Information . . . 18
Setting the Output Voltage . . . 18
Inductor Selection . . . 18
Input Capacitor Selection . . . 19
Output Capacitor Selection . . . 19
Current-Sense Resistor Selection . . . 19
Current Sense Configurations . . . 20
Inductor DCR Current Sense . . . 20

TABLE OF CONTENTS (CONTINUED)

Boost Converter Compensation . . . 20
MOSFET Selection . . . 22
Threshold Voltage . . . 22
Maximum Drain-to-Source Voltage (VDS(MAX)) . . . 22
Current Capability . . . 22
Low Voltage Operation . . . 22
Flyback Converter . . . 22
Transformer Design . . . 23
MOSFET Selection in Flyback Configuration . . . 24
Output Filter Design in Flyback Configuration . . . 25
SEPIC Converter . . . 25
Inductor Selection in SEPIC Converter . . . 25
MOSFET, Diode, and Series Capacitor Selection in a SEPIC Converter . . . 26
Layout Recommendations . . . 26
Typical Application Circuits . . . 27
Boost Application Circuit . . . 27
SEPIC Application Circuit . . . 28
Ordering Information . . . 28
Revision History . . . 29

LIST OF FIGURES

Figure 1. Current Sense Configurations 20
Figure 2. Booster Application Circuit 27
Figure 3. SEPIC Application Circuit 28

Absolute Maximum Ratings

SUP, EN to GND ..... -0.3V to 42V
OUT, FB to GND ..... -0.3V to 65V
SUP to CS ..... -0.3V to 0.3V
BIAS, MODE/FSYNC, PGOOD, SS to GND ..... -0.3V to 6V
DL, FOSC, COMP to GND ..... -0.3V to BIAS + 0.3V
Package Thermal Characteristics
T1633Y+5C
Continuous Power Dissipation
TQFN (derate 28.8mW/°C* above +70°C)..... 1666mW
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 5°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})..... 44.5°C/W
Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Soldering Temperature (reflow).....+260°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to 125	ºC

Note: These limits are not guaranteed.

Package Information

TQFN

Package Code	T1633Y+5C
Outline Number	21-100150
Land Pattern Number	90-100064
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	44.5
Junction to Case (θ_{JC})	5

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = 14V, V_{EN} = 14V, C_{BIAS} = 1µF, T_A = -40°C to +125°C unless otherwise noted, T_J = -40°C to +150°C unless otherwise noted, Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP UP CONTROLLER						
Supply Voltage Range		Initial startup, V_{OUT} = V_{BATT}	4.5		36	V
	V_{SUP}	Operation after initial start-up condition is satisfied	1.8		36	
Output Over-Voltage Threshold		Detected with respect to V_{FB} Rising	102.0	105	107.5	%

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{EN} = 14V, C_{BIAS} = 1µF, T_A = -40°C to +125°C unless otherwise noted, T_J = -40°C to +150°C unless otherwise noted, Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{IN}	V_{EN} = V_{SUP}, V_{FB} = V_{BIAS} (fixed output voltage), V_{SUP} > V_{OUT}, No load		25		µA
		V_{EN} = V_{SUP}, V_{SUP} > V_{OUT}, adjustable output, no load. Excludes current through external FB divider.		20		
		Shutdown, V_{EN} = 0V, fixed output voltage		1.5	3	
		Shutdown, V_{EN} = 0V, adjustable output, excludes current through external FB divider		1.5	3	
Fixed Output Voltage	V_{OUT}	V_{FB} = V_{BIAS}, PWM mode, MAX25200ATEA/VY+ and MAX25200ATEB/VY+ only	5.023	5.125	5.228	V
		V_{FB} = V_{BIAS}, skip mode, MAX25200ATEA/VY+ and MAX25200ATEB/VY+ only	4.97	5.125	5.28	
Output Voltage Adjustable Range		MAX25200ATEA/VY+ and MAX25200ATEB/VY+	3.5		36	V
		MAX25200ATEC/VY+ and MAX25200ATED/VY+	20		60	
Regulated Feedback Voltage	V_{FB}		0.99	1.005	1.02	V
Feedback Leakage Current	I_{FB}	T_A = 25°C		0.01	1	µA
Feedback Line Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.01		%/V
Transconductance (from FB to COMP)	gm_boost	V_{FB} = 1V, V_{BIAS} = 5V (Note 2)	165	250	345	µS
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		1.5	2.8	Ω
DL Pulldown resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1	2	Ω
Minimum Off Time	T_{OFFBST}			80		ns
PWM Switching Frequency Range		Programmable with R_{FOSC}	0.22		2.2	MHz
Switching Frequency Accuracy		R_{FOSC} = 70kΩ, V_{BIAS} = 5V, 3.3V	380	400	420	kHz
CS Current-Limit Voltage Threshold	V_{LIMIT}	V_{SUP} – V_{CS}; V_{BIAS} = 5V, V_{SUP} > 2.5V	40	50	60	mV
Soft-Start Current Source	I_{SS}	V_{BIAS} = 5V	8	10	12	µA
LX Leakage Current		V_{LX} = V_{PGND} or V_{SUP}, T_A = 25°C		0.001	5	µA
PGOOD Threshold	PGOOD_H	% of V_{FB}, rising	92.5	94.5	96.5	%
	PGOOD_F	% of V_{FB}, falling	90.5	92.5	94.5	
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = 25°C			1	µA

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{EN} = 14V, C_{BIAS} = 1µF, T_A = -40°C to +125°C unless otherwise noted, T_J = -40°C to +150°C unless otherwise noted, Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Output Low Voltage		I_{PGOOD} = 1mA			0.2	V
PGOOD Debounce Time		Fault Detection, rising and falling		150		µs
PGOOD Timeout		Output in regulation to PGOOD high		1.5		ms
FSYNC INPUT						
FSYNC Frequency Range		Minimum sync pulse of 100ns, F_{OSC} = 2.2MHz	1.8		2.6	MHz
		Minimum sync pulse of 100ns, F_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High threshold	1.4			V
		Low threshold			0.4	
INTERNAL LDO BIAS						
Internal BIAS Voltage		V_{IN} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.25	V
		V_{BIAS} falling	2.4	2.6		
Minimum Current Capability		V_{BIAS} = 5V		150		mA
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 2)		170		°C
Thermal Shutdown Hysteresis		(Note 2)		20		°C
EN LOGIC INPUT						
High Threshold			1.8			V
Low Threshold					0.8	V
EN Input Bias Current		EN logic inputs only, T_A = 25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		MAX25200ATEB/VY+, MAX25200ATED/VY+		F_{OSC} +/- 6%		

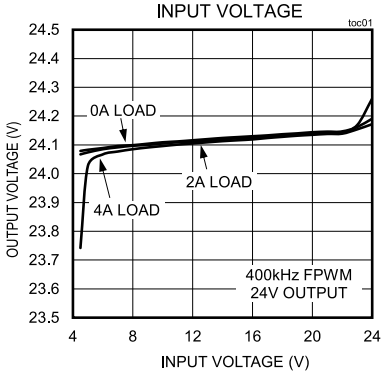
Note 1: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 2: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

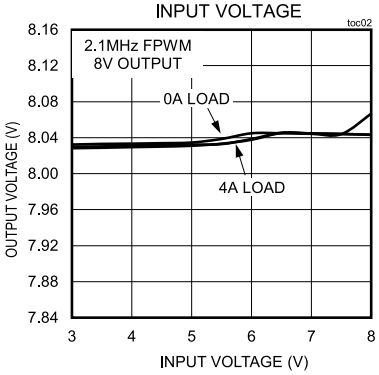
Typical Operating Characteristics

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

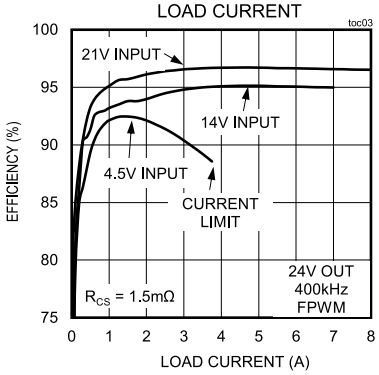
OUTPUT VOLTAGE vs. INPUT VOLTAGE



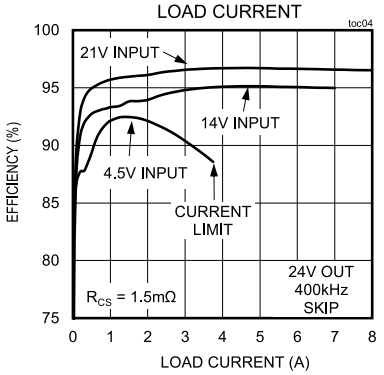
OUTPUT VOLTAGE vs. INPUT VOLTAGE



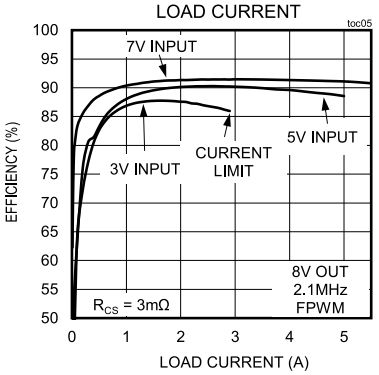
MAX25200 EFFICIENCY vs. LOAD CURRENT



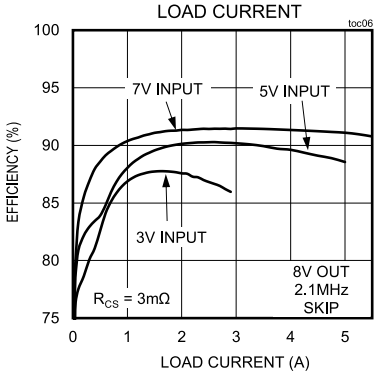
MAX25200 EFFICIENCY vs. LOAD CURRENT



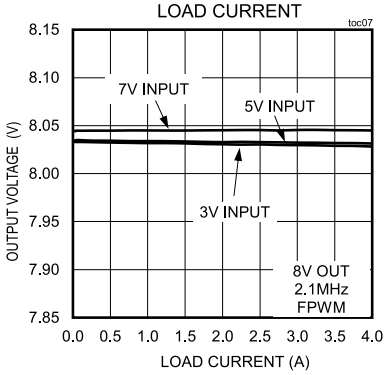
MAX25200 EFFICIENCY vs. LOAD CURRENT



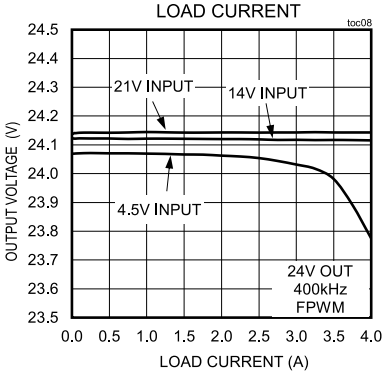
MAX25200 EFFICIENCY vs. LOAD CURRENT



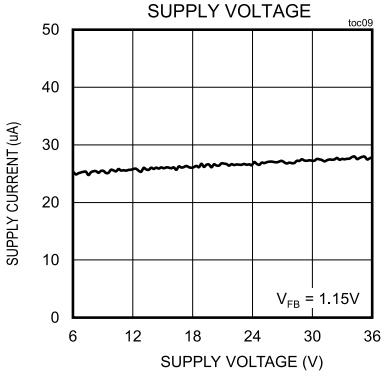
OUTPUT VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT



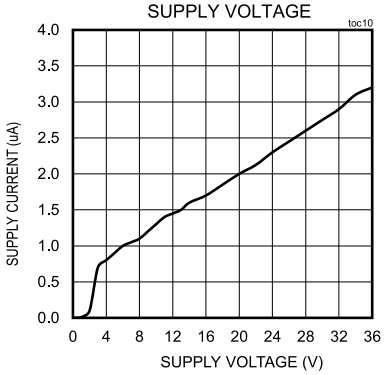
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



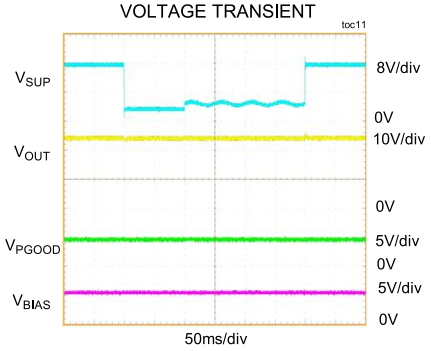
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

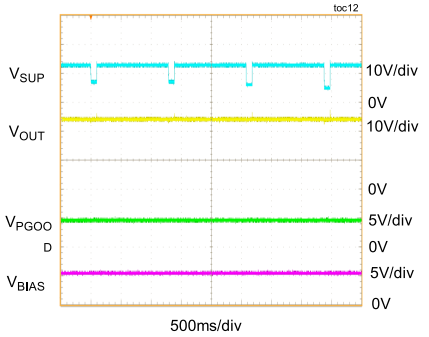
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



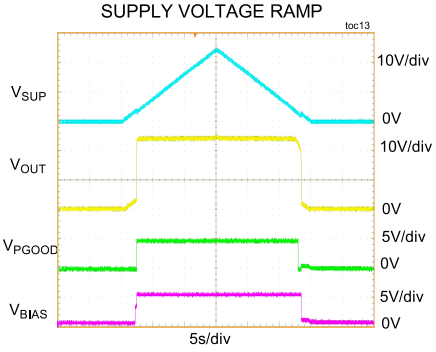
COLD-CRANK INPUT VOLTAGE TRANSIENT



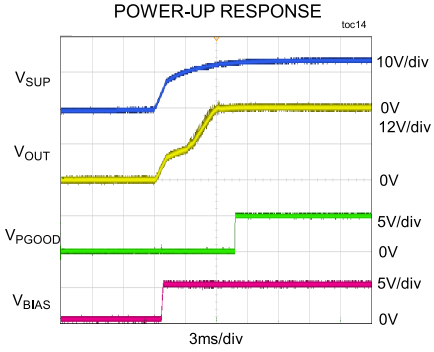
INPUT UNDERVOLTAGE PULSE



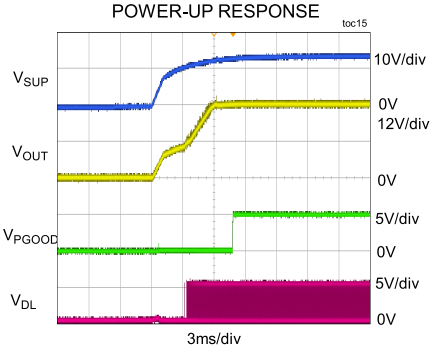
SUPPLY VOLTAGE RAMP



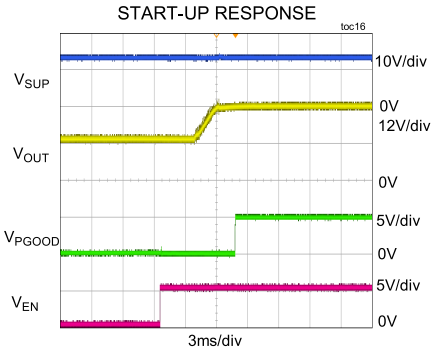
POWER-UP RESPONSE



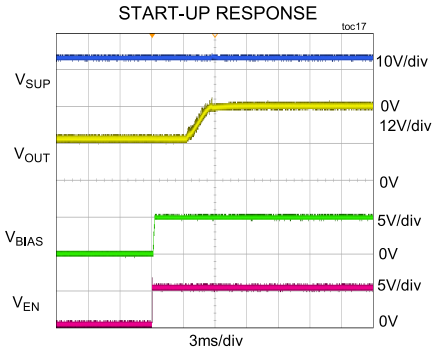
POWER-UP RESPONSE



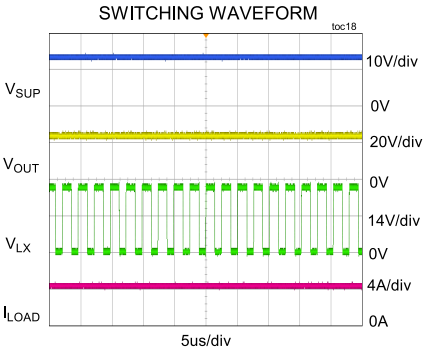
START-UP RESPONSE



START-UP RESPONSE



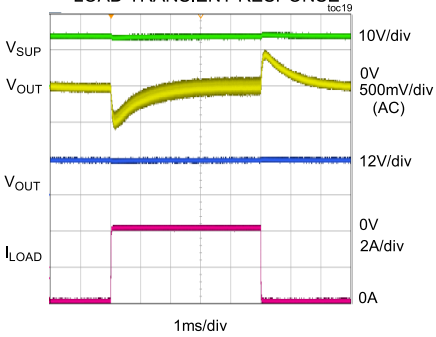
SWITCHING WAVEFORM



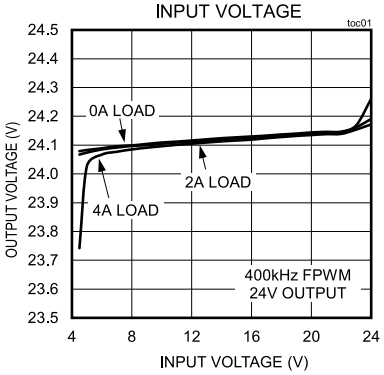
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

LOAD TRANSIENT RESPONSE



OUTPUT VOLTAGE vs. INPUT VOLTAGE



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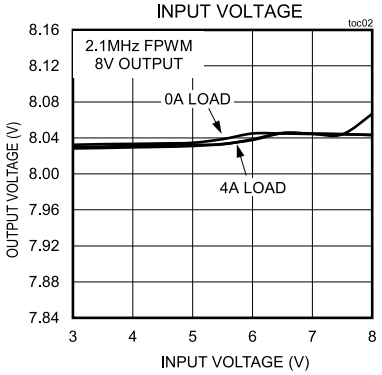
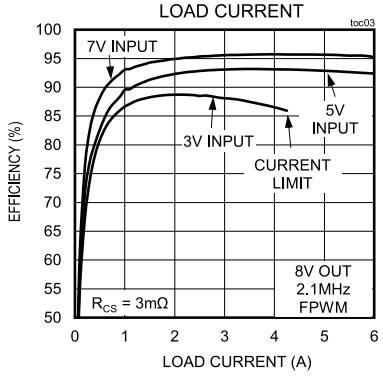
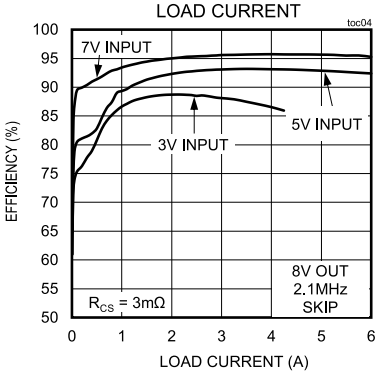


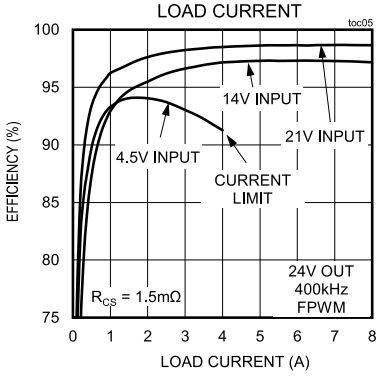
MAX25201 EFFICIENCY vs. LOAD CURRENT



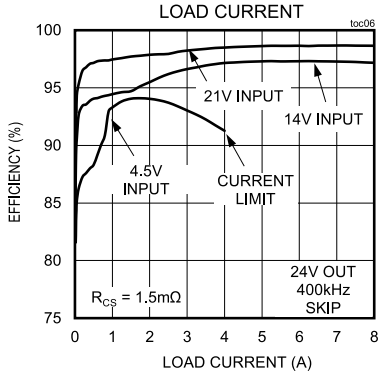
MAX25201 EFFICIENCY vs. LOAD CURRENT



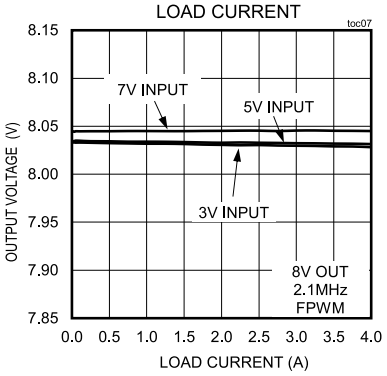
MAX25201 EFFICIENCY vs. LOAD CURRENT



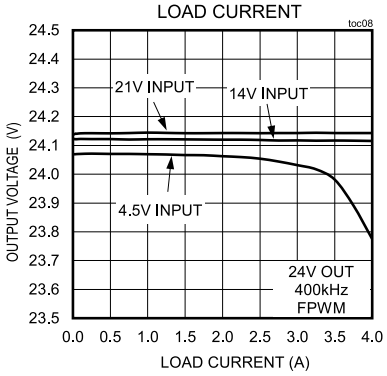
MAX25201 EFFICIENCY vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT



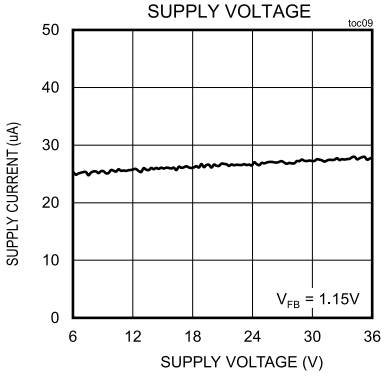
OUTPUT VOLTAGE vs. LOAD CURRENT



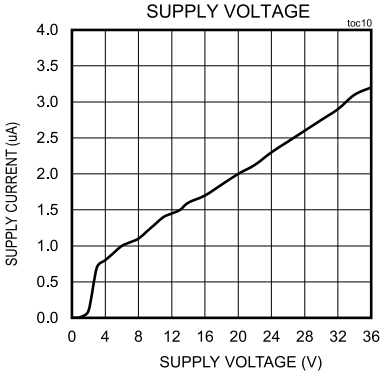
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

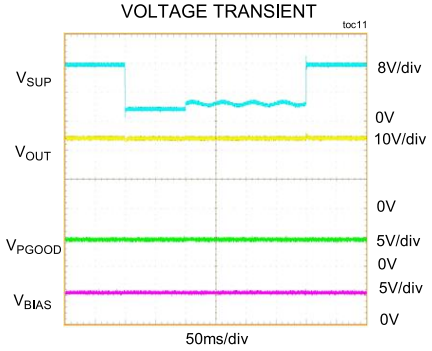
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



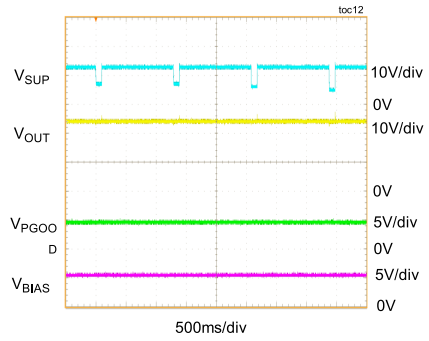
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



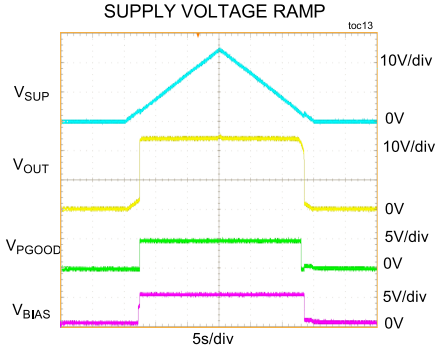
COLD-CRANK INPUT VOLTAGE TRANSIENT



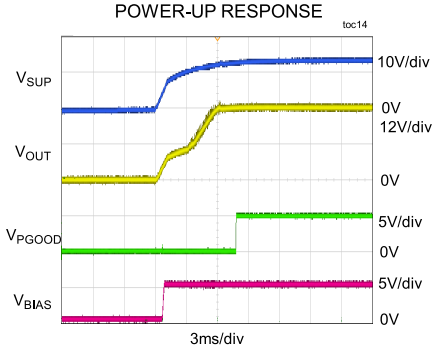
INPUT UNDERVOLTAGE PULSE



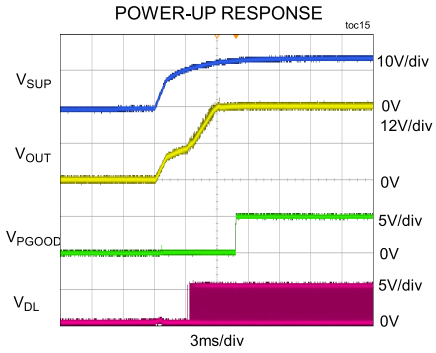
SUPPLY VOLTAGE RAMP



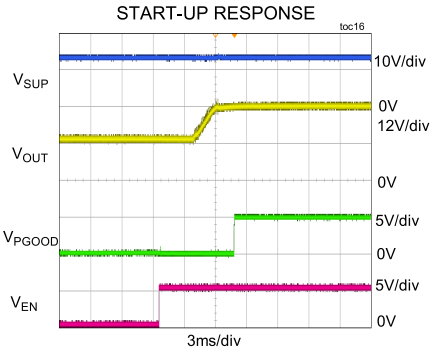
POWER-UP RESPONSE



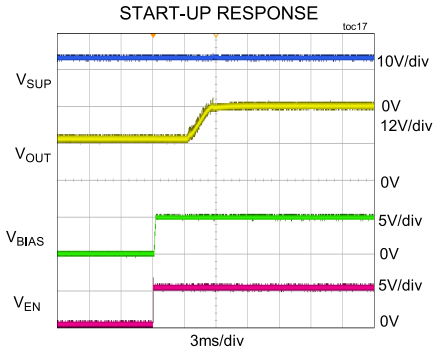
POWER-UP RESPONSE



START-UP RESPONSE

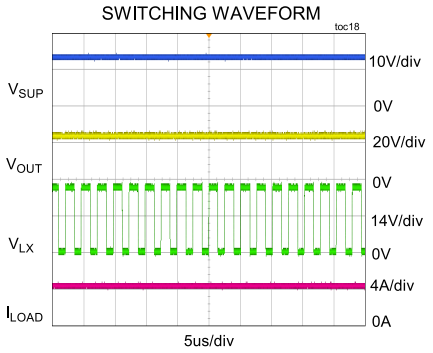


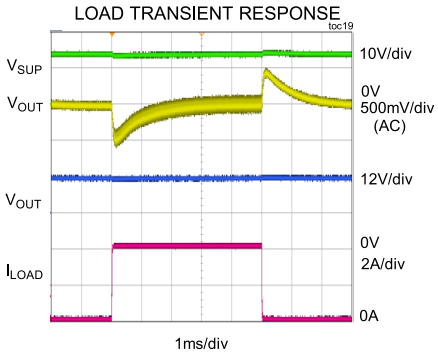
START-UP RESPONSE



Typical Operating Characteristics (continued)

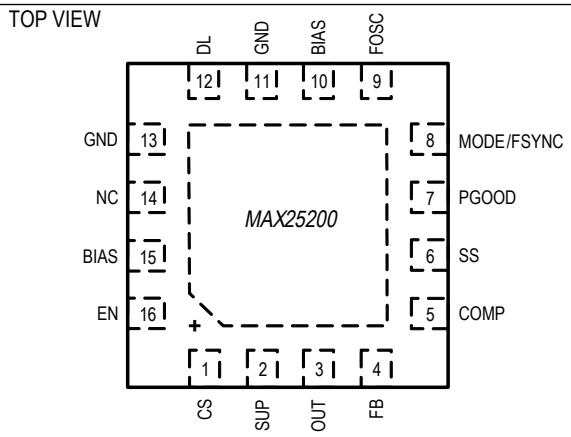
(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)





Pin Configuration

MAX25200



SW TQFN
3mm x 3mm

Pin Description

PIN	NAME	FUNCTION
1	CS	Negative Current-Sense Input for Boost Controller. Connect CS to the negative side of the current-sense element. See Current Limiting and Current Sense Inputs and Current Sense Measurement sections.
2	SUP	Supply Input and Positive Current-Sense Input for Boost Controller. Connect SUP to the positive terminal of the current-sense element. See Current Limiting and Current Sense Inputs and Current Sense Measurement sections.
3	OUT	Input for the BIAS LDO. Connect OUT to the boost output when the output voltage is set at 24V or below. For V_{OUT} greater than 24V, connect OUT to the input supply.

Pin Description (continued)

PIN	NAME	FUNCTION
4	FB	Boost Converter Feedback Input. To set the output voltage between 3.5V and 60V, connect FB to the center tap of a resistive divider between the boost regulator output. FB regulates to 1V (typ). To use the factory set fixed output voltage on applicable parts (see Ordering Information), connect FB to BIAS and connect OUT to the output. For more information see Setting the Output Voltage.
5	COMP	Boost Controller Error Amplifier Output. Connect a RC network to COMP to compensate boost converter.
6	SS	Programmable soft start. Connect a capacitor from SS to GND to set the soft-start time. To select the value see Typical Operating Characteristics.
7	PGOOD	Open Drain Power-Good Output for Buck Controller One. PGOOD goes low if OUT drops below 92.5% (typ falling) of the normal regulation point. PGOOD asserts low during soft-start and in shutdown. PGOOD becomes high impedance when OUT is in regulation. To obtain a logic signal, pull up PGOOD with an external resistor connected to a positive voltage lower than 5.5V.
8	MODE/ FSYNC	External Clock Synchronization Input. To use the internal oscillator connect MODE/FSYNC high for forced-PWM or low for skip-mode operation. To synchronize with an external clock, connect the clock to MODE/FSYNC. See Switching Frequency/External Synchronization section.
9	FOSC	Frequency Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC converters.
14	NC	Do not connect.
10,15	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 1µF minimum value. BIAS provides the power to the internal circuitry and external loads. See Fixed 5V Linear Regulator (BIAS) section.
11,13	GND	Ground.
12	DL	Low-side N-Channel MOSFET Gate Driver Output.
16	EN	High-Voltage Tolerant, Active High Digital Enable Input for Controller.
EP	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX25200 is a high-performance, current-mode PWM controller with 1.5µA (typ) shutdown current for boost converters with a wide input voltage range. The 4.5V to 36V input operating voltage range makes these devices ideal in automotive applications, such as front-end preboost or general-purpose boost power supply, for the first boost stage in high-power LED lighting applications or to generate audio amplifier voltages. An internal low-dropout regulator with a 5V output voltage enables the MAX25200 to operate directly from an automotive battery input. The input operating range can be extended to as low as 1.8V after startup.

Current-Mode Control Loop

Peak current-mode control operation provides excellent load step performance and simple compensation. The inherent feed-forward characteristic is useful especially in automotive applications where the input voltage changes quickly during cold-crank and load dump conditions. To avoid premature turn-off at the beginning of the on cycle the current-limit and PWM comparator inputs have leading-edge blanking.

Fixed 5V Linear Regulator (BIAS)

An internal 5V linear regulator (BIAS) is used to power the controller's internal circuitry. Connect a 1µF or greater ceramic capacitor from BIAS to GND as close to the IC pins as possible to guarantee stability under the full-load condition. The internal linear regulator can provide up to 150mA (typ) total. The internal bias current requirements can be estimated as follows:

$I_{BIAS} = I_{CC} + f_{SW} \times Q_G$

where

I_{CC} = the internal supply current

f_{SW} = the switching frequency

Q_G = the MOSFET total gate charge (specification limits at V_{GS} = 5V).

To reduce the internal power dissipation, BIAS can optionally be connected to an external 5V rail, bypassing the internal linear regulator.

The OUT pin is the input to the linear regulator. OUT is typically connected to the boost output for applications with the output voltage set to 24V or less and applications that require operation with a supply voltage below 5.2V. To reduce power dissipation in applications with higher output voltages, OUT should be connected to SUP. Bypass OUT with a 1µF or greater ceramic capacitor to GND.

Startup Operation/UVLO/EN

The BIAS undervoltage lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.6V (typ) UVLO falling threshold. Once BIAS rises above its UVLO rising threshold and EN is high, the boost controller starts switching and the output voltage begins to ramp up using soft-start. Driving EN low disables the device and reduces the standby current to less than 10µA.

Soft-Start

Soft-start ramps up the internal reference during startup to reduce input surge current. Connect a capacitor from SS to GND to set the soft-start time. Select the capacitor value as follows:

C_{SS} [nF] = 10 × t_{ss} [ms]

Soft-start begins when EN is logic high and V_{BIAS} is above the undervoltage lockout threshold.

Oscillator Frequency/External Synchronization

The MAX25200's internal oscillator is set by a resistor connected from FOSC to GND with an adjustment range of 220kHz to 2.2MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to

higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space.

$$F_{SW} = \frac{24500 + \sqrt{\frac{R_{FOSC}}{0.006}}}{R_{FOSC}}$$

The device can also be synchronized to an external clock by connecting the external clock signal to MODE/FSYNC. The internal oscillator is synchronized on the rising edge of the external clock. See *Electrical Characteristics* for the FSYNC frequency range and voltage levels.

Light-Load Efficiency Skip Mode

The skip mode feature of the MAX25200 is used to improve light-load efficiency. Drive MODE/FSYNC low to enable skip mode.

In skip mode, once the output reaches regulation, the MAX25200 stops switching until the FB voltage drops below the reference voltage. Once the FB voltage has dropped below the reference voltage, the device resumes switching until the inductor current reaches 30% (skip threshold) of the maximum current set by the inductor DCR or current sense resistor.

Forced-PWM Mode

Drive MODE/FSYNC of the MAX25200 high (connect to BIAS) for forced-PWM operation. This prevents the device from entering skip mode by disabling the zero-crossing detection of the inductor current. Under light-load the inductor current reverses, discharging the output capacitor. The benefit of forced-PWM mode is that it keeps the switching frequency constant under all load conditions. This reduces ripple and makes it predictable and easier to filter. Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands. The disadvantage with forced-PWM operation is that it reduces light-load efficiency.

Forced-PWM is always used when synchronizing to an external clock.

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Forced-PWM is always used when synchronizing to an external clock.

Spread Spectrum

Spread spectrum reduces peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent EMI limits. This is done by dithering the switching frequency +/-6%. Using an external clock source (i.e. driving the MODE/FSYNC input with an external clock) disables spread spectrum.

Spread spectrum is a factory set option. See Ordering Information to determine which part numbers have spread spectrum enabled.

MOSFET Driver (DL)

DL drives the gate of an external n-channel MOSFET. The driver is powered from the internal 5V regulator (BIAS), making the device suitable for use with logic-level MOSFETs. The average current sourced by DL depends on the switching frequency and total gate charge of the external MOSFET.

Current Limiting and Current Sense Inputs (SUP and CS)

The current-limit circuit uses differential current-sense inputs (SUP and CS) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (V_{LIMIT} > 50mV (typ)), the PWM controller

turns off the high-side MOSFET.

For the most accurate current sensing, use a current-sense resistor between the inductor and the input capacitor. Connect CS to the inductor side of R_{CS} and SUP to the capacitor side. See

Current Sense Resistor Selection

to determine the resistor value.

To improve efficiency, the current can also be measured directly across the inductor, eliminating the power loss from the sense resistor. However, this method is significantly less accurate and requires a filter network in the current-sense circuit. See

DCR Current Sense

for more information.

Voltage Monitoring (PGOOD)

PGOOD is the open-drain output of the output voltage monitor. PGOOD is high impedance when the output voltage is in regulation. PGOOD pulls low when the output voltage drops below the PGOOD threshold (see Electrical Characteristics). Typically, a pullup resistor is connected from PGOOD to the relevant logic rail to provide a logic-level output. PGOOD asserts low during soft-start and when disabled (EN is low).

Protection Features

Overcurrent Protection

If the inductor current exceeds the maximum current limit set by R_{CS} or inductor DCR sensing, the respective MOSFET driver turns off. Increasing the output current further results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. When required, choose components that can withstand the short-circuit current.

Thermal Overload Protection

Thermal-overload protection limits total power dissipation in the MAX25200. When the junction temperature exceeds +170°C (typ), an internal thermal sensor shuts the device off, allowing it to cool down. The thermal sensor turns the device on again after the junction temperature cools by 20°C (typ).

Slope Compensation

The device uses an internal current-ramp generator for slope compensation. The slope compensation for the MAX25200A and MAX25200B is optimized for operation with output voltage set to 36V or lower. The MAX25200C and MAX25200D are optimized for output voltages between 20V and 60V.

Applications Information

Setting the Output Voltage

All versions of the MAX25200 support an adjustable output voltage. See Ordering Information for the adjustable output voltage range. To set the output voltage, connect FB to the center a resistor divider from the output to ground. Calculate the resistor values as follows:

$$R1 = R2\left[\frac{V_{OUT}}{V_{FB}} - 1\right]$$

where R1 is the resistor connected from FB to the output, R2 is the resistor connected from FB to ground, V_{OUT} is the desired output voltage, and V_{FB} is the regulated feedback voltage (1.005V typ).

Parts with a fixed output voltage option (see Ordering Information) can also be used without the external FB divider. To use the preset output voltage, connect FB to BIAS, and connect OUT to the regulator output.

Inductor Selection

Duty cycle and frequency are important when calculating the inductor size, because the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are used as the input filter components during non-boost operation, a low frequency is advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{SUP(MIN)}}{V_{OUT(MAX)}}$$

or including losses from the inductor DC resistance (R_{DC}) and the boost diode forward voltage drop (V_D):

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{SUP(MIN)} + \left(I_{OUT} \times R_{DC}\right) + V_D}{V_{OUT(MAX)}}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input

voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{SUP} \times D}{f_{SW}[MHz] \times LIR}$$

where

$D = (V_{OUT}\text{-}V_{SUP})/V_{OUT}$

V_{SUP} = Typical input voltage

V_{OUT} = Typical output voltage

$LIR = 0.3 \times I_{OUT}/(1\text{-}D)$

Select the inductor with a saturation current rating higher than the peak switch current limit of the converter:

$$I_{L\_PEAK} > I_{L\_MAX} + \frac{\Delta I_{L\_RIP\_MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half plane zero into the transfer function. To avoid the effect of this right-half plane zero, the crossover frequency for the control loop should be ≤ 1/3 x f_{RHP_ZERO}. If faster bandwith is required, a smaller inductor and higher switching frequency is recommended.

Input Capacitor Selection

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor (C_{SUP}) value and the maximum ESR using the following equations:

$$C_{SUP} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where

$$\Delta I_L = \frac{\left(V_{SUP} - V_{DS}\right) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at high output-to-input differential.

Output Capacitor Selection

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I_{OUT} is the load current in A, f_{SW} is in MHz, C_{OUT} is in µF, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Current-Sense Resistor Selection

The current-sense resistor (R_{CS}), connected between the battery and the inductor, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 50mV (typ).

Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{SUP(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{SUP(MAX)} = \frac{I_{LOAD(MAX)}}{1 - D_{MAX}}$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

Current Sense Configurations

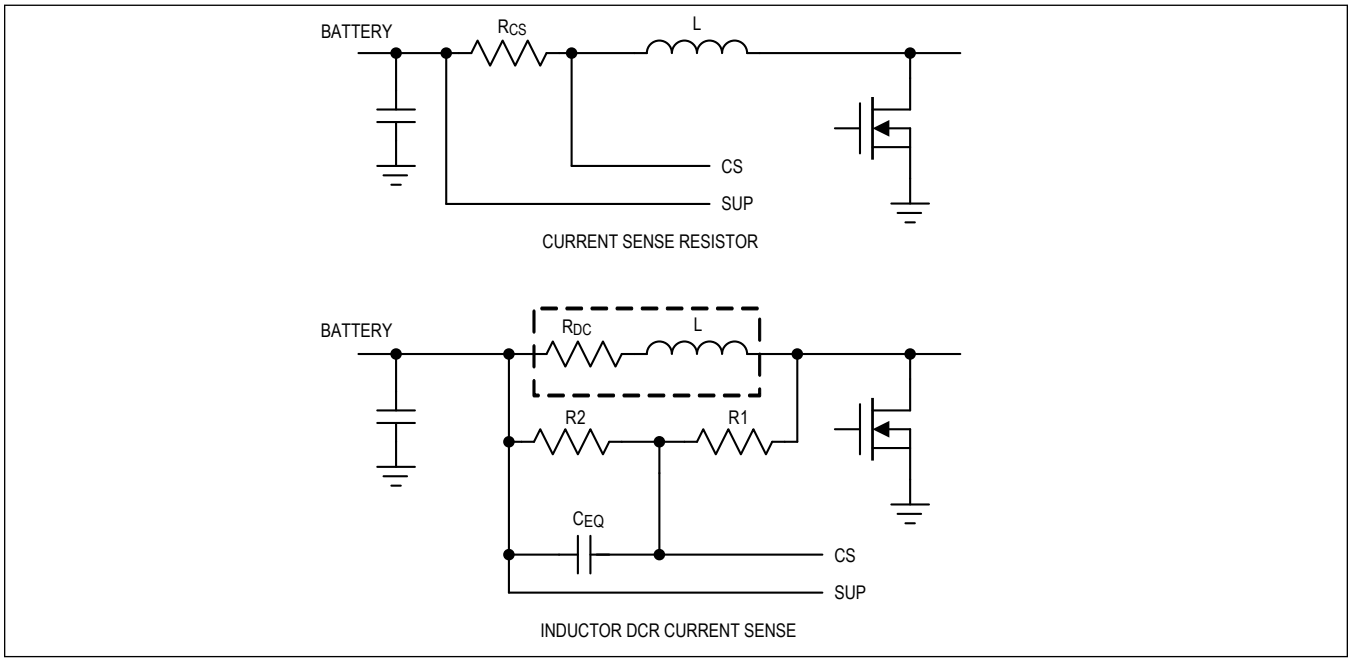

Figure 1. Current Sense Configurations

Inductor DCR Current Sense

High-power applications that do not require accurate current sense can use the inductor's DC resistance as the current sense element instead of the current-sense resistor. This is done by connecting an RC network across the inductor. The equivalent sense resistance of the network is:

$$R_{CS\_EQ} = \left(\frac{R2}{R1 + R2}\right) \times R_{DC}$$

where R_{DC} is the DC resistance of the inductor, R1 is connected from the switch side of the inductor to CS, and R2 is connected from the battery side of the inductor to CS. The capacitor C_{EQ} (connected parallel to R2) is calculated as follows:

$$C_{EQ} = \frac{L}{R_{DC}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

Boost Converter Compensation

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in Figure 2. The power modulator has a DC gain set by gmc x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equations:

$$G_{MOD} = g_{MC} \times R_{LOAD} \times \left(\frac{1 - D}{2}\right) \times \left(\frac{1 + j\frac{f}{f_{zMOD}}}{1 + j\frac{f}{f_{pMOD}}}\right) \times \left(1 - j\frac{f}{f_{Rph\_zMOD}}\right)$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_{mc} =1/(A_{V_CS} x R_{DC}) in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 12V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The right-half plane zero is at:

$$f_{Rph\_zMOD} = \frac{R_{LOAD}}{2\pi \times L} \times (1 - D) \times (1 - D)$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = ESR(EACH)/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1.0V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = gm_{,EA}$ x $R_{OUT,EA}$, where $gm_{,EA}$ is the error-amplifier transconductance, which is 345µS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 10MΩ (typ) (see the Electrical Characteristics table.)

A dominant pole (f_{dpEA}) is set by the compensation capacitor (CC) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (RC) and the compensation capacitor (CC). There is an optional pole (f_{PEA}) set by CF and RC to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Thus:

$$f_{pEA} = \frac{1}{2\pi \times \left(R_{OUTEA} + R_C\right) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{p2EA} = \frac{1}{2\pi \times R_C \times C_F}$$

The loop gain crossover frequency (f_C) should be ≤ 1/3 of right-half plane zero frequency.

$$f_C \le \frac{f_{Rph\_zMOD}}{3}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,\,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,\,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,\,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

MOSFET Selection

The key selection parameters to choose the n-channel MOSFET used in the boost converter are as follows.

Threshold Voltage

The boost n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V.

Maximum Drain-to-Source Voltage (VDS(MAX))

The MOSFET must be chosen with an appropriate VDS rating to handle all VIN voltage conditions.

Current Capability

The n-channel MOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V.

Low Voltage Operation

The devices start with a supply voltage as low as 4.5V, and can operate after initial start up with a supply voltage as low as 1.8V. At very low input voltages it is important to remember that input current will be high and the power components (inductor, MOSFET, and diode) must be specified for this higher input current.

In addition, the current-limit must be set high enough so that the limit is not reached during the MOSFET's on time, which would limit output power and eventually force the MAX25200 into hiccup mode. Estimate the maximum input current using the following equation:

$$I_{SUPMAX} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{SUPMIN}} + 0.5 \times \frac{V_{OUT} - V_{SUPMIN}}{V_{OUT}} \times \frac{V_{SUPMIN}}{f_{SW} \times L}$$

where I_{SUPMAX} is the maximum input current; V_{OUT} and I_{OUT} are the output voltage and current, respectively; η is the estimated efficiency (which is lower at low input voltages due to higher resistive losses); V_{SUPMIN} is the minimum value of the input voltage; f_{SW} is the switching frequency; and L is the minimum value of the chosen inductor.

Flyback Converter

The choice of the conversion topology is the first stage in power-supply design. The topology selection criteria include input voltage range, output voltage, peak currents in the primary and secondary circuits, efficiency, form factor, and cost.

For an output power of less than 50W and a 1:2 input voltage range with small form factor requirements, the flyback topology is the best choice. It uses a minimum of components, thereby reducing cost and form factor. The flyback converter can be designed to operate either in a continuous or a discontinuous mode of operation. In discontinuous mode, the transformer core completes its energy transfer during the off-cycle; in continuous mode, the next cycle begins before the energy transfer is complete. The discontinuous mode of operation is chosen for the present example because:

- it maximizes the energy storage in the magnetic component, thereby reducing size;
- it simplifies the dynamic stability compensation design (no right-half plane zero);
- it provides higher unity-gain bandwidth.

A major disadvantage of discontinuous mode is the higher peak-to-average current ratio in the primary and secondary circuits. Higher peak-to-average current means higher RMS current, and therefore, higher loss and lower efficiency. For low-power converters, the advantages of using discontinuous mode easily surpass the possible disadvantages. Moreover, the drive capability of the MAX25200 is good enough to drive a large switching MOSFET. With the MOSFETs

presently available, power output of up to 50W is easily achievable with a discontinuous mode flyback topology when the MAX25200 is used in automotive applications.

Transformer Design

The following section provides an example of a discontinuous flyback design. Follow the steps below when designing a discontinuous mode transformer:

1. Calculate the secondary winding inductance for guaranteed core discharge within a minimum off-time.

   As discussed earlier, the core must be discharged during the off-cycle for discontinuous mode operation.

   The secondary inductance determines the time required to discharge the core. Use the following equations to calculate the secondary inductance:

   $$L_S \le \frac{\left(V_{OUT} + V_D\right) \times \left(D_{OFFMIN}\right)^2}{2 \times I_{OUT} \times f_{OUT(MAX)}}$$

   $$D_{OFF} = \frac{t_{OFF}}{t_{ON} + t_{OFF}}$$

   where:

   D_{OFFMIN} = Minimum D_{OFF}

   V_D = Secondary diode forward voltage drop

   I_{OUT} = Maximum output rated current

2. Calculate primary winding inductance for sufficient energy to support the maximum load.

   The rising current in the primary builds the energy stored in the core during on-time, which is then released to deliver the output power during the off-time. Primary inductance is then calculated to store enough energy during the on-time to support the maximum output power.

   $$L_P = \frac{V_{SUPMIN}^2 \times D_{MAX}^2 \times \eta}{2 \times P_{OUT} x f_{OUT(MAX)}}$$

   $$D = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

   D_{MAX} = Maximum D.

3. Calculate the secondary and bias winding turns ratios.

   Calculate the secondary to primary turns ratio (N_{SP}) and the bias winding to primary turns ratio (N_{BP}) using the following equations:

   $$N_{SP} = \frac{N_S}{N_P} = \sqrt{\frac{L_S}{L_P}}$$

   and

   $$N_{BP} = \frac{N_{BIAS}}{N_P} = \frac{11.7}{V_{OUT} + 0.35}$$

   The forward bias drops of the secondary diode and the bias rectifier diode are assumed to be 0.35V and 0.7V, respectively. Refer to the diode manufacturer's data sheet to verify these numbers.

4. Calculate the RMS current in the primary and estimate the secondary RMS current.

   The transformer manufacturer needs the RMS current maximum values in the primary, secondary, and bias windings to design the wire diameter for the different windings. Use only wires with a diameter smaller than 28AWG to

keep skin effect losses under control. To achieve the required copper cross-section, multiple wires must be used in parallel. Multifilar windings are common in high-frequency converters. Maximum RMS currents in the primary and secondary occur at 50% duty cycle (minimum input voltage) and maximum output power. Use the following equations to calculate the primary and secondary RMS currents:

$$I_{PRMS} = \frac{P_{OUT}}{0.5 \times D_{MAX} \times \eta \times V_{SUPMIN}} \times \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{SRMS} = \frac{I_{OUT}}{0.5 \times D_{OFFMAX}} \times \sqrt{\frac{D_{OFFMAX}}{3}}$$

The bias current for most MAX25200 applications is about 20mA and the selection of wire depends more on convenience than on current capacity.

5. Consider proper sequencing of windings and transformer construction for low leakage.

   The winding technique and the windings sequence are important considerations when attempting to reduce the leakage inductance spike at switch turn-off. For example, interleave the secondary between two primary halves. Keep the bias winding close to the secondary, so that the bias voltage tracks the output voltage.

MOSFET Selection in Flyback Configuration

MOSFET selection criteria include the maximum drain voltage, peak/RMS current in the primary and the maximum-allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage through transformer turns ratio and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case (maximum input voltage and output load) drain voltage.

$$V_{DSMAX} = V_{SUPMAX} + \left[\frac{N_P}{N_S} \times \left[V_{OUT} + V_D\right]\right] + V_{SPIKE}$$

Lower maximum V_{DS} requirement means a shorter channel, lower $R_{DS(ON)}$, lower gate charge, and smaller package. A lower N_P/N_S ratio allows a low V_{DSMAX} specification and keeps the leakage inductance spike under control. A resistor/diode/capacitor snubber network can also be used to suppress the leakage inductance spike.

The DC losses in the MOSFET can be calculated using the value for the primary RMS maximum current. Switching losses in the MOSFET depend on the operating frequency, total gate charge, and the transition loss during turn-off. There are no transition losses during turn-on because the primary current starts from zero in the discontinuous conduction mode. MOSFET derating may be necessary to avoid damage during system turn-on and any other fault conditions. Use the following equation to estimate the power dissipation due to the power MOSFET:

$$P_{MOS} = \left(1.4 \times R_{DSON} \times I^2_{RMS}\right) + \left(Q_g \times V_{SUP} \times f_{OUTMAX}\right) +$$

$$\left(\frac{V_{INMAX} \times I_{PK} \times t_{OFF} \times f_{OUTMAX}}{4}\right)$$

$$+ \frac{C_{DS} \times V^2_{DS} \times f_{OUTMAX}}{2}$$

where:

Q_g = Total gate charge of the MOSFET (C) at 7.4V

V_{SUP} = Input voltage (V)

t_{OFF} = Turn-off time (s)

C_{DS} = Drain-to-source capacitance (F)

Output Filter Design in Flyback Configuration

The output capacitance requirements for the flyback converter depend on the peak-to-peak ripple acceptable at the load. The output capacitor supports the load current during the switch on-time. During the off-cycle, the transformer secondary discharges the core, thereby replenishing the lost charge and simultaneously supplying the load current. The output ripple is the sum of the voltage drop due to charge loss during the switch on-time and the ESR of the output capacitor. The high switching frequency of the MAX25200 reduces the capacitance requirement.

An additional small LC filter may be necessary to suppress the remaining low-energy high-frequency spikes. The LC filter also helps attenuate the switching frequency ripple. Care must be taken to avoid any compensation problems due to the insertion of the additional LC filter. Design the LC filter with a corner frequency at more than a decade higher than the estimated closed-loop, unity-gain bandwidth to minimize its effect on the phase margin. Use 1µF to 10µF low-ESR ceramic capacitors and calculate the inductance using following equation:

$$L \le \frac{1}{4 \times 10^3 \times f_C^2 \times C}$$

where f_C = estimated converter closed-loop unity-gain frequency.

SEPIC Converter

The MAX25200 can be configured for SEPIC conversion when the operating range of the input voltage includes values higher and lower than the target output voltage. The duty-cycle equation:

$$\frac{V_{OUT}}{V_{SUP}} = \frac{D}{1 - D}$$

indicates that the output voltage is lower than the input for a duty cycle lower than 0.5 while V_{OUT} is higher than the input at a duty cycle higher than 0.5. The inherent advantage of the SEPIC topology over the boost converter is that the output is completely isolated from the source when an output fault occurs. The SEPIC converter output can be fed back to IN through a Schottky diode (see Figure 3), allowing the controller to function during low voltage conditions such as cold-crank. Use a Schottky diode (ΔV_{SUP}) in the V_{SUP} path to avoid backfeeding the input source.

The SEPIC converter design includes sizing of inductors, a MOSFET, series capacitance, and the rectifier diode. The inductance is determined by the allowable ripple current through all the components mentioned above. Lower ripple current means lower peak and RMS currents and lower losses. The higher inductance value needed for a lower ripple current means a larger-sized inductor, which is a more expensive solution. The inductors (L1 and L2) can be independent. However, winding them on the same core reduces the ripple currents.

Calculate the maximum duty cycle using the following equation and choose the RT and CT values accordingly for a given switching frequency (see the Oscillator Frequency/External Synchronization section).

$$D = \left[\frac{V_{OUT} + V_D}{V_{SUPMIN} + V_{OUT} + V_D - \left[V_{DS} + V_{CS}\right]}\right]$$

where V_D is the forward voltage of the Schottky diode, V_{CS} (50mV) is the current-sense threshold of the MAX25200, and V_{DS} is the voltage drop across the switching MOSFET during the on-time.

Inductor Selection in SEPIC Converter

Use the following equations to calculate the inductance values. Assume both L1 and L2 are equal and that the inductor ripple current (ΔIL) is equal to 20% of the input current at nominal input voltage to calculate the inductance value.

$$L = L1 = L2 = \frac{V_{SUPMIN} \times D_{MAX}}{2 \times f_{OUT} \times \Delta I_L}$$

$$\Delta I_L = \frac{0.2 \times I_{OUTMAX} \times D_{MAX}}{\left(1 - D_{MAX}\right) \times \eta}$$

where f_{OUT} is the converter switching frequency and η is the targeted system efficiency. Use the coupled inductors such

as MSD-series from Coilcraft or PF0553-series from Pulse Engineering, Inc. Make sure the inductor saturating current rating (ISAT) is 30% higher than the peak inductor current, calculated using the following equation. Use the current-sense resistor, calculated based on the I_{LPK} value from the equation below (see the Current Limit section).

$$I_{LPK} = \frac{I_{OUTMAX} \times D_{MAX}}{\left(1 - D_{MAX}\right) \times \eta} + I_{OUTMAX} + \Delta I_L$$

MOSFET, Diode, and Series Capacitor Selection in a SEPIC Converter

For the SEPIC configuration, choose an n-channel MOSFET with a V_{DS} rating at least 20% higher than the sum of the output and input voltages. When operating at a high switching frequency, the gate charge and switching losses become significant. Use low gate-charge MOSFETs. The RMS current of the MOSFET is:

$$I_{MOSRMS}(A) = \sqrt{\left[I_{LPK}^2 + I_{LDC}^2 + I_{LPK} \times I_{LDC}\right] \times \frac{D_{MAX}}{3}}$$

where $I_{LDC} = I_{LPK} - \Delta I_L$

Use Schottky diodes for higher conversion efficiency. The reverse voltage rating of the Schottky diode must be higher than the sum of the maximum input voltage (V_{supmax}) and the output voltage. Since the average current flowing through the diode is equal to the output current, choose the diode with forward current rating of I_{OUTMAX}. The current sense (RCS) can be calculated using the current-limit threshold and I_{LPK}. Use a diode with a forward current rating more than the maximum output current limit if the SEPIC converter needs to be output short-circuit protected.

$$R_{CS} = \frac{V_{CS}}{I_{LPK}}$$

Select R_{CS} 20% below the value calculated above. Calculate the output current limit using the following equation:

$$I_{OUTLIM} = \frac{D}{1 - D} \times \left(I_{LPK} - \Delta I_L\right)$$

where D is the duty cycle at the highest input voltage (V_{SUPMAX}).

The series capacitor should be chosen for minimum ripple voltage (ΔV_{CP}) across the capacitor. We recommend using a maximum ripple ΔV_{CP} to be 5% of the minimum input voltage (V_{SUPMIN}) when operating at the minimum input voltage. The multilayer ceramic capacitor X7R series are recommended due to their high ripple current capability and low ESR. Use the following equation to calculate the series capacitor CP value.

$$CP = \frac{I_{OUTMAX} \times D_{MAX}}{\Delta V_{CP} \times f_{OUT}}$$

Where ΔV_{CP} is 0.05 x V_{SUPMIN}.

For more information refer to *http://pdfserv.maximintegrated.com/en/an/AN1051.pdf*

Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Layout of the switching power components requires particular attention. Follow these guidelines for good PCB layout:

- Keep high-current paths short, especially at the ground terminals.
- Minimize resistance in high-current paths by keeping the traces short and wide. Using thick (2oz vs. 1oz Copper) improves full load efficiency.
- Connect the CS and SUP connections used for current sensing directly across the sense resistor using a Kelvin sense connection.
- Route noisy switching and clock traces away from sensitive analog areas (FB, CS).

Typical Application Circuits

Boost Application Circuit

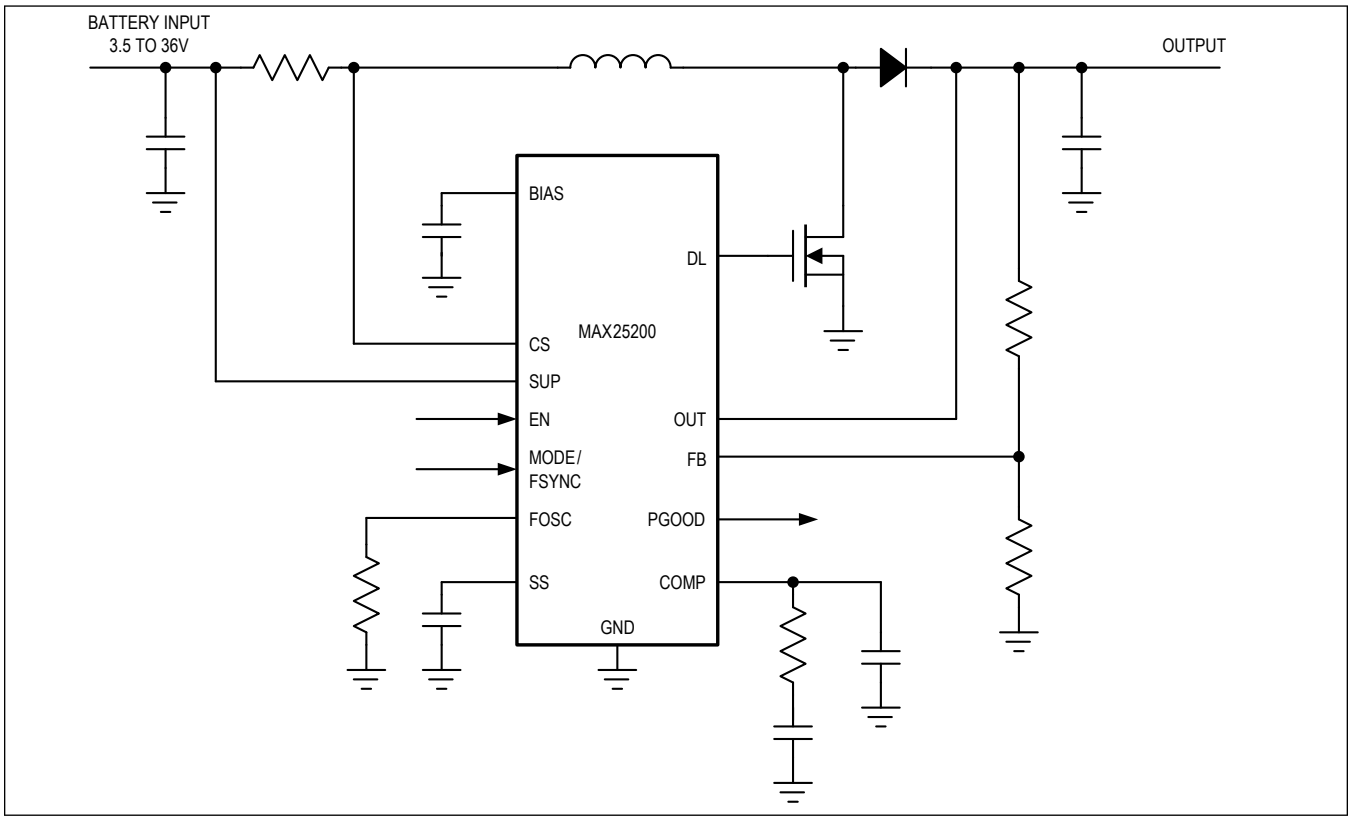

Figure 2. Booster Application Circuit

Typical Application Circuits (continued)

SEPIC Application Circuit

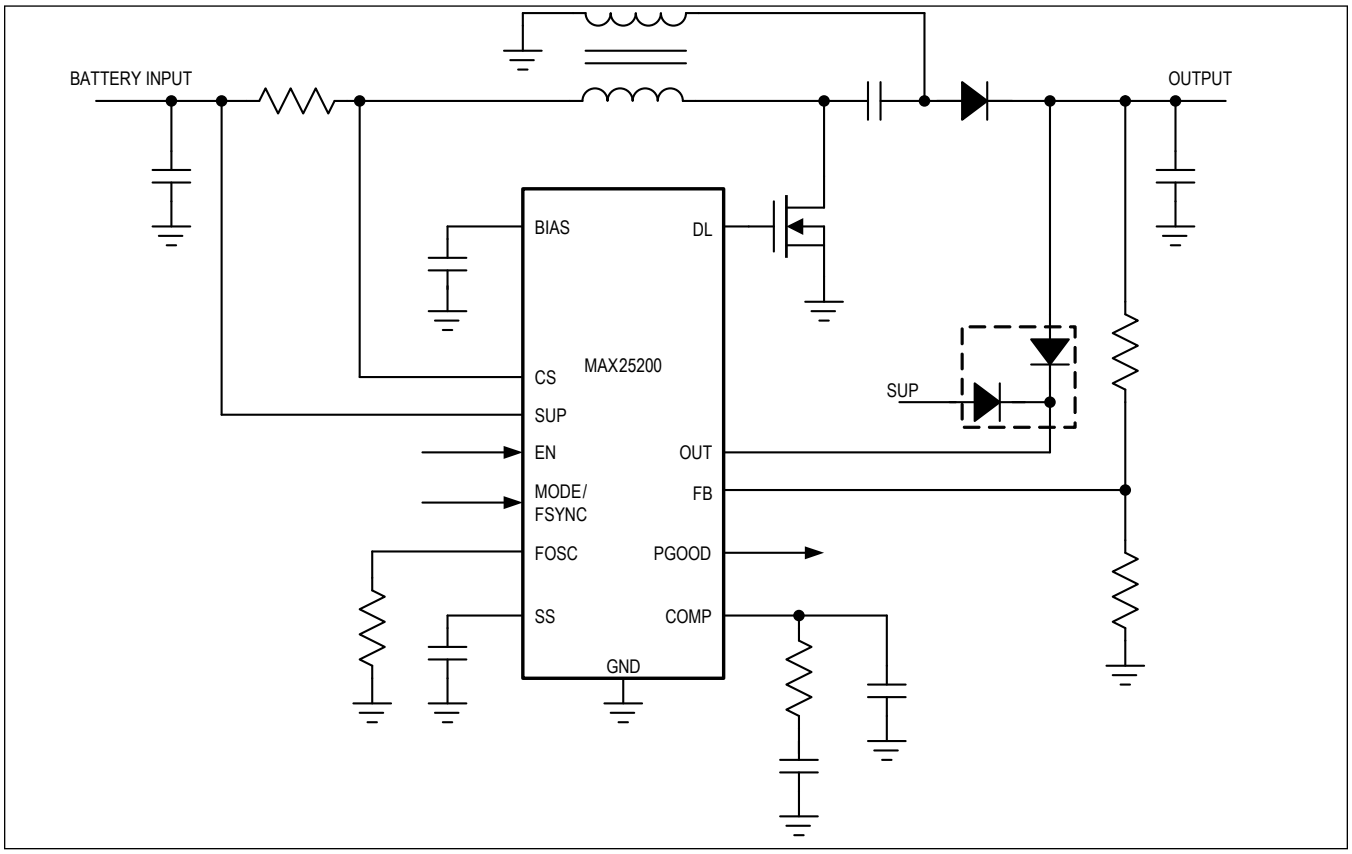

Figure 3. SEPIC Application Circuit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT} RANGE	FIXED V_{OUT}	SPREAD SPECTRUM
MAX25200ATEA/VY+	-40°C to +125°C	16 TQFN-EP*	3.5V to 36V	5.12V	OFF
MAX25200ATEB/VY+	-40°C to +125°C	16 TQFN-EP*	3.5V to 36V	5.12V	ON
MAX25200ATEC/VY+**	-40°C to +125°C	16 TQFN-EP*	20V to 60V	N/A	OFF
MAX25200ATED/VY+	-40°C to +125°C	16 TQFN-EP*	20V to 60V	N/A	ON

**EP = Exposed Pad.*

***Future product—contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/19	Initial release	—
1	1/20	Removed future-product notation from MAX25200ATEB/VY+ and MAX25200ATED/VY+ in *Ordering Information*	28