

SCOPE: VOLTAGE-OUTPUT 12-BIT MULTIPLYING DACs

<u>Device Type</u>	<u>Generic Number</u>	<u>Circuit Function</u>
01	MAX532A(x)/883B	Dual, Serial-Input, Voltage-Output, 12-Bit
02	MAX532B(x)/883B	Multiplying Digital to Analog Converter

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIN SMD			
JE E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16

Absolute Maximum Ratings:

V_{DD} to DGND, AGNDA, AGNDB	-0.3V, +17V
V_{SS} to DGND, AGNDA, AGNDB	+0.3V, -17V
VREFA, VREFB	(V_{SS} -0.3V) to (V_{DD} +0.3V)
AGNDA, AGNDB	(DGND-0.3V) to (V_{DD} +0.3V)
V_{OUTA} , V_{OUTB}	(V_{SS} -0.3V) to (V_{DD} +0.3V)
RFBA, RFBB	(V_{SS} -0.3V) to (V_{DD} +0.3V)
SCLK, DIN, DOUT, DOUT, LDAC, CS	(DGND-0.3V) to (V_{DD} +0.3V)
DOUT Sink Current	20mA

Lead Temperature (soldering, 10 seconds) +300°C

Storage Temperature -65°C to +150°C

Continuous Power Dissipation T_A =+70°C

16 pin CERDIP(derate 10.0mW/°C above +70°C) 800mW

Junction Temperature T_J +150°C

Thermal Resistance, Junction to Case, θ_{JC}

16 pin CERDIP..... 100°C/W

Thermal Resistance, Junction to Ambient, θ_{JA} :

16 pin CERDIP..... 50°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) -55°C to +125°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125 °C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE		2/					
Resolution	N		1,2,3	All	12.0		Bits
Relative Accuracy	INL		1,2,3	01 02	-0.5 -1.0	+0.5 +1.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Zero Code Offset Error	VOE	DAC latch loaded with all 0s	1 2,3 2,3	All 01 02		±2.0 ±3.0 ±4.0	mV
Gain Error	AE	DAC latch loaded with all 1s	1	01 02		±2.0 ±5.0	LSB
		DAC latch loaded with all 1s	2,3	01 02		±4.0 ±7.0	
REFERENCE INPUT		(VREFA, VREFB)					
VREFA, VREFB Input Resistance	RIN		1,2,3	All	8	13	kΩ
VREFA, VREFB Input Resistance matching	RMATCH		1,2,3	All		3.0	%
DIGITAL INPUTS		SCLK, DIN, LDAC, CS					
Input High Voltage	V _{IH}		1,2,3	All	2.4		V
Input Low Voltage	V _{IL}		1,2,3	All		0.8	V
Input Current	I _{IN}	V _{IN} =0V or V _{DD}	1,2,3	All		±1.0	μA
Input Capacitance	C _{IN}	NOTE 3	4	All		8.0	pF
DIGITAL OUTPUT	DO _{UT}	NOTE 4					
Output Voltage Low	V _{OL}	I _{SINK} =5mA	1,2,3	All		0.4	V
Output High Leakage	I _{LKG}	V _{DO_{UT}} =0V to V _{DD}	1,2,3	All		±10	μA
Output High Capacitance	CO _{UT}	NOTE 3	4	All		15	pF
ANALOG OUTPUTS		VO_{UT}A, VO_{UT}B					
Output Voltage Swing			1,2,3	All	V _{DD} -2.5 to V _{SS} +2.5		V
POWER REQUIREMENTS							
Positive Supply Voltage	V _{DD}		1,2,3	All	11.4	16.5	V
Negative Supply Voltage	V _{SS}		1,2,3	All	-11.4	-16.5	V
Power Supply Rejection	PSR	ΔFull scale/ΔV _{DD} , V _{DD} =11.4V to 16.5V, VREF=-8.9V, DAC latches loaded with all 1s.	1,2,3	All		±0.035	LSB/ %
		ΔFull scale/ΔV _{SS} , V _{SS} =-11.4V to -16.5V, VREF=8.9V, DAC latches loaded with all 1s.					

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Positive Supply Current	I _{DD}	Output unloaded	1,2,3	All		10	mA
Negative Supply Current	I _{SS}	Output unloaded	1,2,3	All		6	mA
TIMING CHARACTERISTICS		NOTES 5, 6					
SCLK Clock Frequency	f _{CLK}		9,10,11	All		6.25	MHz
SCLK Pulse Width High	t _{CH}		9,10,11	All	80		ns
SCLK Pulse Width Low	t _{CL}		9,10,11	All	80		ns
DIN to SCLK Rise Setup Time	t _{DS}		9,10,11	All	50		ns
DIN to SCLK Rise Hold Time	t _{DH}		9,10,11	All	0		ns
CS Fall to SCLK Rise Setup Time	t _{CSSO}		9,10,11	All	50		ns
CS Rise to SCLK Rise Setup Time	t _{CSS1}		9,10,11	All	50		ns
SCLK Fall to CS Fall Hold Time	t _{C SHO}		9,10,11	All	5		ns
SCLK Rise to CS Rise Hold Time	t _{C SH1}		9,10,11	All	80		ns
CS Pulse Width High	t _{CSW}		9,10,11	All	120		ns
SCLK Fall to DOUT Valid	t _{DO}	CL=20pF, Rpull-up=1kΩ to 5V NOTE 7	9,10,11	All	0	200	ns
CS Fall to DOUT Enable	t _{DV}	CL=20pF, Rpull-up=1kΩ to 5V NOTE 8	9,10,11	All		100	ns
CS Rise to DOUT Disable	t _{TR}	CL=20pF, Rpull-up=1kΩ to 5V NOTE 8	9,10,11	All		60	ns
LDAC Pulse Width Low	t _{LDAC}		9,10,11	All	60		ns
CS Rise to LDAC Fall Setup Time	t _{LDACS}		9,10,11	All	100		ns

NOTE 1: V_{DD}=11.4V to 16.5V, V_{SS}=-11.4 to -16.5V, AGNDA=AGNDB=DGND=0V, VREF_A and VREF_B=+10V, R_L=2kΩ, C_L=100pF, V_{OUT_} connected to RFB_{_}.

NOTE 2: Static performance tested at V_{DD}=+15V, V_{SS}=-15V. Performance over supplies guaranteed by PSR test.

NOTE 3: Guaranteed by design. Not subject to production testing.

NOTE 4: Open-drain output.

NOTE 5: All input signals are specified with t_R=t_F≤5ns. Logic input swing is 0V to 5V.

NOTE 6: See Figure 1 in commercial datasheet.

NOTE 7: Timing is for SCLK fall to DOUT fall to 0.8V or for SCLK fall to DOUT rise to 2.4V. Additional time must be added for any larger passive RC pull-up delay.

NOTE 8: DOUT enable: DOUT falls to 4.5V from 5.0V. DOUT disable: DOUT rises to 0.5V from 0V.

	Package	ORDERING INFORMATION:	SMD NUMBER
01	16 pin Cerdip	MAX532AMJE/883B	5962-9566701MEA
02	16 pin Cerdip	MAX532BMJE/883B	5962-9566702MEA

TERMINAL CONNECTIONS:

Pin		Pin	
1	RFBA	9	V _{SS}
2	VREFA	10	DGND
3	V _{OUTA}	11	SCLK
4	AGNDA	12	DOUT
5	AGNDB	13	DIN
6	VOUTB	14	$\overline{\text{CS}}$
7	VREFB	15	$\overline{\text{LDAC}}$
8	RFBB	16	V _{DD}

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, Capacitance tests are tested only at initial qualification and at redesign.