Apollo MxFE Octal, 16-Bit, 16 GSPS RF DAC and Octal, 12-Bit, 8 GSPS RF ADC

FEATURES

- Flexible reconfigurable common platform design
  - 8 DACs and 8 ADCs (8D8A)
  - Usable RF analog bandwidth to 16 GHz
  - Maximum DAC/ADC sample rate up to 16 GSPS/8 GSPS
- DAC to ADC sample rate ratios of 1 and 2
  - Clocking
  - On-chip PLL (7 GHz to 14 GHz VCO)
- External RFCLK input up to 8 GHz
  - Multichip synchronization
- Single-ended (SE) ADC inputs
  - 50 Ω input impedance
  - Integrated on-chip wide bandwidth balun
- ADC AC performance at 8 GSPS
  - Full-scale input voltage: 650 mV p-p/0.3 dBm
  - Noise density: −148 dBFS/Hz at −20 dBFS at 2 GHz
  - HD2/HD3: −70 dBFS/−75 dBFS at −7 dBFS at 2 GHz
  - IMD3: −75 dBFS at −13 dBFS/tone at 2 GHz
- DAC AC performance at 16 GSPS
  - Full-scale output power: −1.1 dBm at 2 GHz
  - IMD3: −7 5 dBc at −13 dBFS/tone at 2 GHz
  - NSD (shuffling disabled): −163 dBFS/Hz at −1 dBFS at 2 GHz
  - NSD (shuffling enabled): −158 dBFS/Hz at −1 dBFS at 2 GHz
- Versatile digital features
  - Supports real or complex digital data (8-, 12-, 16-bit)
  - Configurable DDC and DUC
  - 16 fine complex DUCs and 8 coarse complex DUCs
  - 16 fine complex DDCs and 8 coarse complex DDCs
  - Option to bypass fine and coarse DUC/DDC
  - DUC/DDC alias rejection
  - 85 dB for interpolation filters
  - 100 dB for decimation filters
- Programmable FIR filters for transmit/receive.
- Dynamic configuration through SPI/HSCI/GPIO
- Interface
  - SPI
  - High-Speed Control Interface
  - JESD204B/JESD204C: 20 Gbps/32.5 Gbps
- 24 lanes for Rx, 24 lanes for Tx
- Signal monitor for slow AGC control
- Auxiliary features
  - Power amplifier downstream protection circuitry
  - On-chip temperature monitoring unit
  - TDD power savings option
- Total power consumption dependent on device configuration: 14 W to 20 W typical
- 24 mm × 26 mm, 889-ball BGA with 0.8 mm pitch
- Operating junction temperature (T_J): −40°C to +110°C

APPLICATIONS

- Radar and communications
  - L/S/C band radar and electronic warfare
  - Phase array system
  - Broadband communications systems
- Electronic test and measurement systems
- Satellite communications
- Microwave point-to-point, E-band and 5G mmWave

FUNCTIONAL BLOCK DIAGRAM

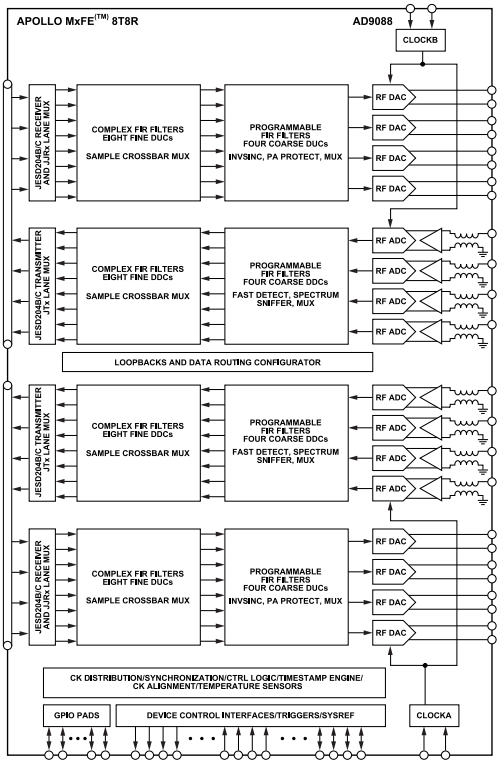

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The Apollo mixed signal front-end (MxFE®) is a highly integrated device with a 16-bit, 16 GSPS maximum sample rate, RF digital-to-analog converter (DAC) core, and 12-bit, 8 GSPS maximum sample rate, RF analog-to-digital converter (ADC) core. The AD9088 supports eight transmit channels and eight receive channels. The AD9088 is well suited for applications requiring both wideband ADCs and DACs to process signal(s) having wide instantaneous bandwidth. The device features a 48 lane, 32.5 Gbps JESD204C or 20 Gbps JESD204B data transceiver port, an on-chip clock multiplier, and a digital signal processing (DSP) capability targeted at either wideband or multi-band, direct to RF applications. The AD9088 also features a bypass mode that allows the full bandwidth capability of the ADC and/or DAC cores to bypass the DSP datapaths. The device also features low latency loopback and frequency hopping modes targeted at phased array radar systems and electronic warfare applications.

The AD9088 is available in a 24mm x 26mm, 899-ball BGA and operates within the –40°C to +110°C junction temperature range. For additional information, contact ApolloSupport@analog.com.

Table 1. Product Listing with Distinguishing Features

	Tx				Rx					Digital Features					
Part No.	DAC Ch	Max DAC Rate (GSPS)	Analog BW[1] (GHz)	Max Tx iBW (GHz)	ADC Ch	Max ADC Rate (GSPS)	Analog BW[2] (GHz)	Max Rx iBW (GHz)	Input Network	FSRC	Rx to Tx Loop back	Fast Freq Hopping	PFILT/ CFIR	Dynamic Config (PFILT CFIR, DDC/DUC)	Spectrum Sniffer
AD9084–DF	4	28	18	14	4	20	18	10	DIFF	Yes	Yes	Yes	Yes	Yes	Yes
AD9084–SE	4	28	18	14	4	14	16	7	SE	Yes	Yes	Yes	Yes	Yes	Yes
AD9088	8	16	18[3].	8	8	8	16	4	SE	No	Yes	Yes	Yes	Yes	Yes

1 Analog bandwidth is the allowed frequency range supported by the DAC output port. It may be limited by the maximum DAC sampling rate due to sinc roll-off, return loss of the PCB layout, and balun response. Check detailed specifications for operating at higher frequencies.

2 Analog BW represents the −3 dB point relative to the input power level near DC. Limited by the on-chip balun response and the return loss of the PCB layout. Check detailed specifications for operating at higher frequencies.

3 Actual output power level is limited by the maximum DAC sampling rate in the adjacent column due to sinc roll-off

OUTLINE DIMENSIONS

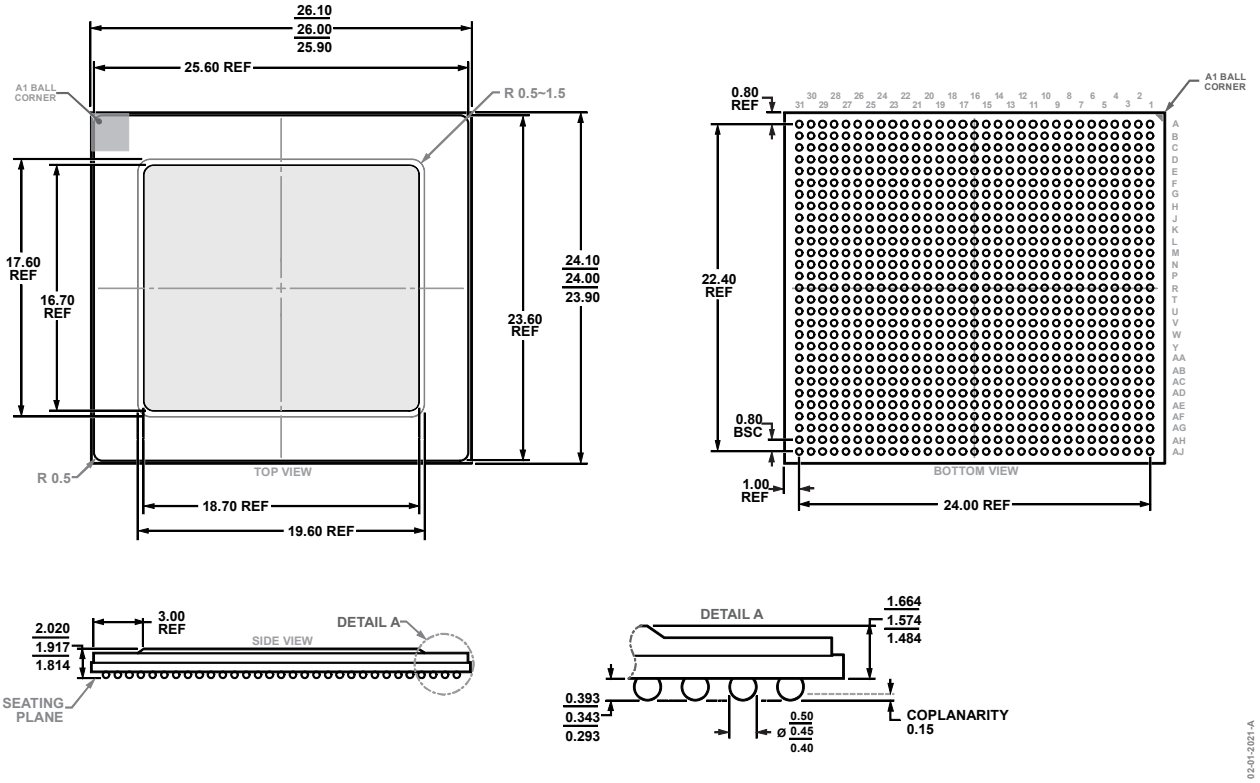

Figure 2. 899-Ball (29 x 31) Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-899-1)
Dimensions shown in millimeters