What's New with LTspice?

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LTspice Blog
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NEW RELEASE OF LTspice

The LTspice® XVII simulator represents the 2017 release of this simulator and has many new features. One of the most significant usability enhancements is an updated graphics library that supports multi-monitor support (or floating windows). This allows users to display a schematic capture window in one monitor and display the simulation results in the waveform viewer window on another monitor. There are also several new interfaces for composing and editing various types of SPICE syntax. New simulator features include improved simulation speeds, support for Unicode, improved VDMOS model, native IGBT device, diode soft recovery, and an arbitrary state machine (.mach).

LTspice MODELS OF ISO 7637-2 & ISO 16750-2 TRANSIENTS
www.linear.com/solutions/7719

Simulating ISO 7637-2 and ISO 16750-2 transients early in the design phase of an automotive product can pinpoint issues that would otherwise come to light during electromagnetic compatibility (EMC) testing. Spending a few minutes simulating the protection circuitry in LTspice helps to avoid expensive hardware respins due to EMC failures. The ISO16750-2 and ISO7637-2 symbols and models in LTspice simplify this task by providing a nearly complete set of ISO transients.

SELECTED DEMO CIRCUITS

For a complete list of example simulations, please visit www.linear.com/democircuits.

Buck Regulators

- **LT8609S:** 2MHz low EMI high voltage synchronous buck regulator (5.5V–42V to 5V at 2A) www.linear.com/LT8609S
- **LTC3895:** High efficiency high voltage buck converter (14V–130V to 12V at 5.0A) www.linear.com/solutions/7343
- **LTM4636**: High current step-down regulator (4.7V–15V to 1V at 40A) www.linear.com/solutions/7703
- **LTM4647**: Single output, high current buck regulator (6V–15V to 1.0V at 30A) www.linear.com/solutions/7671

Isolated Converters

- **LT8310/LT1431:** 92W isolated nonsynchronous forward converter with opto feedback (43V–53V to 54V at 1.7A) www.linear.com/solutions/7821
- **LT8315**: µPower no-opto isolated flyback converter (20V–450V to 12V at 220mA) www.linear.com/LT8315

Surge Stopper

- **LTC7860:** High voltage, high efficiency switching surge stopper with timer (7V–100V to $34V_{MAX}$ at 10A) www.linear.com/solutions/6089

Op Amps

- **LTC6261**: Second order Bessel filter www.linear.com/solutions/7725
- **LTC6362**: Baseband design example for a low power IQ modulator www.linear.com/solutions/7116

SELECT MODELS

To search the LTspice library for a particular device model, press F2. To update to the current version, choose Sync Release from the Tools menu.

Buck Regulators

- **LT8640S:** 42V, 6A synchronous step-down Silent Switcher®2 with 2.5µA quiescent current www.linear.com/LT8640S
- **LTC3126:** 42V, 2.5A synchronous step-down regulator with no-loss input PowerPath™ www.linear.com/LTC3126
- **LTM4643**: Ultrathin quad µModule® regulator with configurable 3A output array www.linear.com/LTM4643

Charge Pumps

- **LTC7820:** Fixed ratio high power charge pump DC/DC controller www.linear.com/LTC7820

Isolated Converters

- **LT8304-1:** 100V input µPower no-opto isolated flyback converter with 150V/2A switch www.linear.com/LT8304

Op Amps

- **LT1997-3:** Precision, wide voltage range gain selectable amplifier www.linear.com/LT1997-3
- **LTC6262**: Dual 30MHz, 240µA power efficient rail-to-rail I/O op amps www.linear.com/LTC6262

Voltage Reference

- **LT6658:** Precision dual output, high current, low noise, voltage reference www.linear.com/LT6658 ■

Power User Tip

SIMULATING SAR ADC ANALOG INPUTS

As resolution and sample rates continue to rise for ADCs, the driver circuitry for the analog inputs, not the ADC itself, has increasingly become the limiting factor in determining overall circuit accuracy. Beyond a simple 1-pole RC lowpass filter (LPF1) for noisy input signals (Figure 1), a coupling RC filter network (LPF2) is often used between the buffer and ADC input to minimize disturbances reflected into the buffer from ADC sampling transients. Long RC time constants at the analog inputs slow the settling of these disturbances. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer.

Simulating the interface between the amplifier and ADC presents some interesting trade-offs between settling time and noise performance. Experimenting with such simulations helps one develop an intuitive understanding of how the filter design affects these performance aspects.

The analog input of a fully differential SAR ADC can be modeled as a switched capacitor load on the drive circuit shown in equivalent form in Figure 2. The values shown are from the LTC2378-20 20-bit, 1Msps, low power SAR ADC but can easily be modified to represent other ADCs. During the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the ON-resistance of the sampling switch. The inputs draw a current spike while charging the C_{IN} capacitors in this phase. During the subsequent conversion phase, the analog inputs draw only a small leakage current and the capacitors are fully discharged. This modeling of the ADC analog input highlights one of the biggest challenges in coupling an amplifier to a SAR ADC such as the LTC2378-20; dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase.

A simulation schematic of this equivalent circuit is shown in Figure 3. The low power LTC6362 differential op amp is configured to convert a single-ended input signal to a fully differential output to drive the LTC2378-20. To simplify the simulation, the input ESD protection diodes are not included. The two 45pF input capacitors (C1 and C2) are charged via voltage controlled switches (S1 and S2) that are defined by a SW model statement with an ON resistance of 40Ω. These switches are driven by a pulsed voltage source with a duration of 312ns and period of 1µs to simulate the acquisition time of the LTC2378-20 SAR ADC at 1Msps. To ready the sampling capacitors for the next acquisition phase, an idealized behavior inverter (A1) is used to turn on the second set of switches (S3 and S4) that discharge the capacitors.

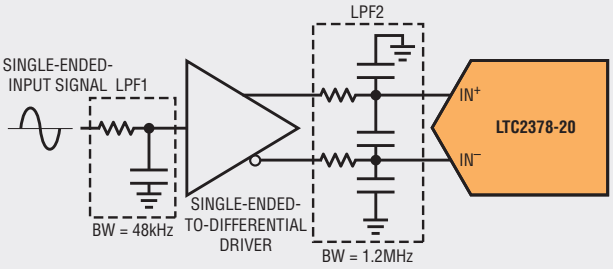

Figure 1. Simulating the interface between an amplifier and ADC can help determine trade-offs between noise and settling time.

The RC filter network between the amplifier and the ADC serves several purposes. First, the filter network reduces the amount of wideband noise entering the ADC. Second, the capacitors serve as a charge reservoir to absorb charge kickback from the ADC's internal sampling capacitors. After each conversion cycle, the discharged sample capacitors (45pF) are reconnected to the amplifier circuit. By placing a much larger reservoir capacitor at the ADC input, the voltage excursion caused by these sample capacitors is reduced. There is, however, a trade-off between wideband noise and settling time performance. While the sample capacitors are connected to the amplifier circuit (acquisition time), the RC network should fully settle to within the resolution of the ADC. Using too much reservoir capacitance in the filter network increases this settling time beyond acceptable limits. For further discussion of this trade-off, watch Kris Lokere's "SAR ADC Driver Interface" video at www.linear.com/solutions/4679.

Happy simulations!

Figure 2. Equivalent circuit for the analog input of the SAR ADC

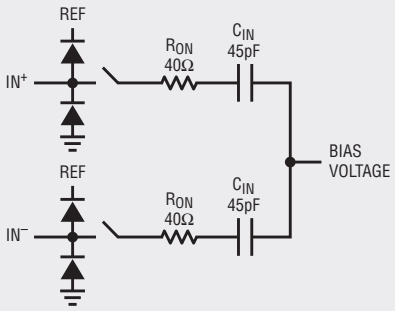

Figure 3. Simulation schematic of SAR ADC analog input equivalent circuit