SCOPE: HIGH-SPEED 12-BIT A/D CONVERTER WITH EXTERNAL REFERENCE INPUT

Device Type	Generic Number	Circuit Function
01	MX7672T(x)05/883B	5microsecond, 1 LSB Linearity
02	MX7672U(x)05/883B	5 microsecond, 1/2 LSB Linearity
03	MX7672T(x)10/883B	10 microsecond, 1 LSB Linearity
04	MX7672U(x)10/883B	10 microsecond, 1/2 LSB Linearity

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP3-T24 or CDIP4-T24	24 LEAD CERDIP	R24
E	CQCC1-N28	28 Leadless Chip Carrier	L28

Absolute Maximum Ratings

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND..... +0.3V to -17V
AGND to DGND ..... -0.3V to (V_{DD}+0.3V)
AIN to AGND ..... -15V to +15V
VREF to AGND ..... V_{SS} -0.3V to (V_{DD}+0.3V)

Digital Input Voltage to DGND (CLKIN, $\overline{CS}$, $\overline{RD}$) ..... -0.3V, (V_{DD}+0.3V)

Digital Output Voltage to DGND (CLKOUT, D11-D0, $\overline{BUSY}$ ..... -0.3V, (V_{DD}+0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
24 pin CERDIP(derate 16.7mW/°C above +70°C) 1000mW
28 pin LCC (derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
24 pin CERDIP..... 40°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
24 pin CERDIP..... 80°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V_{DD}) ..... +4.75V to +5.25V
Negative Supply Voltage (V_{SS}) ..... -10.8V to -13.2V
Clock Frequency (f_{CLK}) Slow-Memory Mode (01,02) ..... 2.5 MHz
Clock Frequency (f_{CLK}) Slow-Memory Mode (03,04) ..... 1.25 MHz
VREF ..... -5V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C 1/ V_{DD}=+5V±5%, V_{SS}=-12V±10%, Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	N		1,2,3	All	12		Bits
Integral Nonlinearity	INL	Tested Range ±5V	1,2,3	01,03	-1.0	+1.0	LSB
			1	02,04	-0.5	+0.5	
			2,3	02,04	-0.75	+0.75	
Differential Nonlinearity	DNL	12 bits, no missing codes over temperature	1,2,3	All		±0.9	LSB
Unipolar Offset Error	V_{OS}		1	01,03	-5.0	+5.0	LSB
				02,04	-3.0	+3.0	
			2,3	01,03	-6.0	+6.0	
				02,04	-4.0	+4.0	
Unipolar Gain Error	V_{OS}		1	01,03	-5.0	+5.0	LSB
				02,04	-4.0	+4.0	
			2,3	01,03	-7.0	+7.0	
				02,04	-6.0	+6.0	
Bipolar Zero Error	V_{OS}		1	01,03	-5.0	+5.0	LSB
				02,04	-3.0	+3.0	
			2,3	01,03	-6.0	+6.0	
				02,04	-4.0	+4.0	
Bipolar Gain Error	V_{OS}		1	01,03	-5.0	+5.0	LSB
				02,04	-4.0	+4.0	
			2,3	01,03	-7.0	+7.0	
				02,04	-6.0	+6.0	
Conversion Time	T_{CONV}	Synchronous CLK (12.5 Clks)	1,2,3	01,02		5.0	µs
		Asynchronous Clk (12 to 13 Clks)			4.8	5.2	
		Synchronous Clk (12.5 Clks)				10	
		Asynchronous Clk (12 to 13 Clks)	1,2,3	03,04	9.6	10.4	
Analog Input Current AIN1 or AIN2		Unipolar input ranges 0V to +5V, 0V to +10V	1,2,3	All		3.5	mA
		Bipolar Range ±5V				±1.75	
VREF Input Range	VREF		1,2,3	All	-5.05	-4.95	V
VREF Input Current			1,2,3	All		±3	µA
Digital Input Low Voltage	V_{INL}	__ ___ CS, RD, CLKIN	1,2,3	All		0.8	V
Digital Input High Voltage	V_{INH}	__ ___ CS, RD, CLKIN	1,2,3	All	2.4		V
Digital Input Capacitance	C_{IN}	NOTE 2	4	All		10	pF
Digital Input Current	I_{IN}	__ ___ CS, RD; V_{IN}=0V to V_{DD}	1,2,3	All		±10	µA
		CLKN; V_{IN}=0V to V_{DD}				±20	
Digital Output Low Voltage	V_{OL}	I_{SINK}=1.6mA, _____ CLKOUT, D11-D0, BUSY	1,2,3	All		0.4	V

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤+125°C 1/ V_{DD}=+5V±5%, V_{SS}=-12V±10%, Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Digital Output High Voltage	V_{OH}	I_{SOURCE}=200µA, $\overline{\text{CLKOUT}}$, D11-D0, BUSY	1,2,3	All	4.0		V
Floating State Leakage Current	I_{LKG}	D11-D0, V_{OUT}=0V to V_{DD}	1,2,3	All	-10	10	µA
Floating State Output Capacitance	C_{OUT}	NOTE 2	4	All		15	pF
Supply Voltage	V_{DD} V_{SS}		1,2,3	All	4.75 -13.2	5.25 -10.8	V
Supply Current	I_{DD} I_{SS}	$\overline{CS}$=$\overline{RS}$=V_{DD}, $\overline{BUSY}$=High, AIN1=AIN2=5V	1,2,3	All		7 -12	mA
Power Dissipation	PD	V_{DD}=5V, V_{SS}=-12V	1,2,3	All		179	mW
Power-Supply Rejection V_{DD} only		FS Change, V_{SS}=-12V, V_{DD}=4.75 to 5.25V	1,2,3	All		±2	LSB
Power-Supply Rejection V_{SS} only		FS Change, V_{DD}=5V, V_{SS}=-10.8V to -13.2V	1,2,3	All		±1	LSB
TIMING CHARACTERISTICS		**CONDITIONS** -55 °C ≤T_A≤+125°C V_{DD}=+5V±5%, V_{SS}=-12V±10%, Unless otherwise specified					
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1	NOTE 2	9,10,11	All	0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L=50pF	9 10,11	All		190 270	ns
Data-Access Time	t_3	C_L=100pF, NOTE 4	9 10,11	All		125 170	ns
$\overline{RD}$ Pulse Width	t_4	NOTE 2	9,10,11	All	t_3		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5	NOTE 2	9,10,11	All	0		ns
Data-Setup Time After $\overline{BUSY}$	t_6	C_L=100pF, NOTE 4	9 10,11	All		70 100	ns
Bus-Relinquish Time	t_7	NOTE 5	9 10,11	All		75 90	ns
Delay Between Read Operations	t_8		9,10,11	All	200		ns
$\overline{CLKIN}$ to $\overline{BUSY}$ Delay	t_9	NOTE 2	9 10,11	All		120 180	ns
$\overline{RD}$ to CLKIN Setup/Hold Time	t_{10}	NOTES 2, 6	9,10,11	All		100	ns

NOTE 1: V_{DD}=+5V, V_{SS}=-12V, 1LSB=FS/4096. Performance over power-supply tolerance is guaranteed by power supply rejection test. VREF=-5V, Slow memory mode, f_{CLK}=2.5MHz for 01, 02, f_{CLK}= 1.25MHz for 03,04.

NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.

NOTE 3: All inputs are 0V to +5V swing with tr=tf=5ns (10% to 90% of +5V) and timed from a 1.6V voltage level.

NOTE 4: Times t_3 and t_6 are measured with the load circuits for Figure1 in the commercial datasheet and defined as the time required for an output to cross 0.8V or 2.4V.

NOTE 5: Time t_7 is defined as the same time required for the data lines to change 0.5V when loaded with the circuits of Figure 2 of commercial datasheet, __

NOTE 6: For predictable conversion times, RD to CLKIN falling edge must be outside this window. CLKIN edge: If t_{10}<25ns, conversion will skip first falling CLKIN edge and start on second falling CLKIN edge. If t_{10}>100ns, conversion will start on first falling CLKIN edge.

	Package	**ORDERING INFORMATION:**
01	24 pin CERDIP	MX7672TQ05/883B
01	28 pin LCC	MX7672TE05/883B
02	24 pin CERDIP	MX7672UQ05/883B
02	28 pin LCC	MX7672UE05/883B
03	24 pin CERDIP	MX7672TQ10/883B
03	28 pin LCC	MX7672TE10/883B
04	24 pin CERDIP	MX7672UQ10/883B
04	28 pin LCC	MX7672UE10/883B

TERMINAL CONNECTIONS:

	J24	L28
1	AIN1	NC
2	VREF	AIN1
3	AGND	VREF
4	D11(MSB)	AGND
5	D10	D11(MSB)
6	D9	D10
7	D8	D9
8	D7	NC
9	D6	D8
10	D5	D7
11	D4	D6
12	DGND	D5
13	D3	D4
14	D2	DGND
15	D1	NC
16	D0	D3
17	CLKIN	D2
18	CLKOUT	D1
19	$\overline{RD}$	D0
20	$\overline{CS}$	CLKIN
21	$\overline{BUSY}$	CLKOUT
22	V_{SS}	NC
23	V_{DD}	$\overline{RD}$
24	AIN2	$\overline{CS}$
25		$\overline{BUSY}$
26		V_{SS}
27		V_{DD}
28		AIN2

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.