Click here to ask an associate for production status of specific part numbers.

2.5V to 22V Input, 7.8A Switching Current High-Efficiency Buck-Boost Converter for USB-PD/PPS Applications

MAX77859

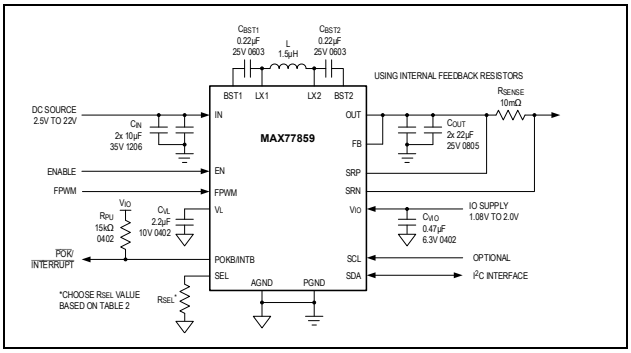
Product Highlights

- Wide Input Voltage Range: 2.5V to 22V
- Programmable Output Voltage
  - 3.2V to 16V with Internal Feedback Resistors
  - 3.0V to 20V with External Feedback Resistors, See *Table 1*
- USB Type-C® Power Delivery (PD)/Programmable Power Supply (PPS)
  - 20mV Output Voltage Step Size
  - 50mA Output Current Limit Step Size
- Maximum Output Current
  - Buck Mode: Up to 6A
  - Boost Mode: Up to 4A (V_{IN} = 3.7V, V_{OUT} = 5V)
- 7.8A Typical Switching Current
- Automatic SKIP Mode and Forced-PWM Mode
- R_{SEL} Configuration
  - I²C Interface Target Address
  - Switching Current Limit Threshold
  - Internal/External Feedback Resistors
- I²C Programming
  - Output Voltage (DVS)
  - Slew Rate of Output Voltage Change
  - Output Current Limit Threshold
  - Switching Current Limit Threshold
  - Switching Frequency
  - Forced-PWM Mode Operation (FPWM)
  - Loop Compensation
  - Power-OK (POK) and Fault Status/Interrupts
- Output Active Discharge
- Open-Drain Status/Interrupts Pin
- Available in a 3.01mm x 2.78mm 42 Wafer-Level Packaging (WLP) or 4.0mm x 4.0mm 19 FC2QFN

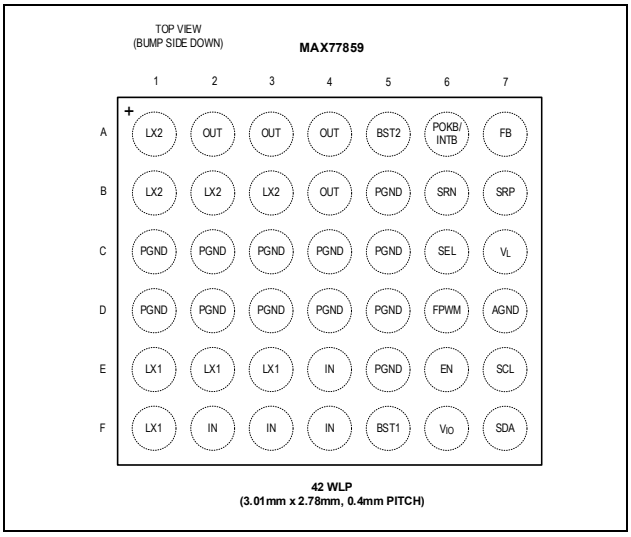
Key Applications

- USB PD 3.0 (PPS) Dynamically-Reconfigurable Processor (DRP) Applications
  The highest output power from any existing ultrabook Universal Serial Bus (USB) Type-C® port is 15W, 5V, and 3A. The MAX77859 can enable USB PD output up to 30W, and it is PPS compliant, which can double the charging speed of any USB Type-C PD-compliant smartphone and peripherals. When implemented, a 15-minute quick recharge on the peripheral from the ultrabook can enable hours of operation to get through the day.

Simplified Application Diagram



Pin Description



- Space-Constrained Applications
  USB-C® PD DRP design is complex and extremely limited in real estate, especially close to the port area. A buck-boost topology design is required to enable USB PD, but the solution size is the critical bottleneck. The MAX77859 is a fully integrated buck-boost converter to help shrink the solution size by 80% plus compared to a discrete buck-boost solution with similar output power capability.

USB Type-C and USB-C are registered trademarks of USB Implementers Forum.

***Ordering Information* appears at end of data sheet**

19-101672; Rev 1; 05/23

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

IN, LX1, LX2 to PGND ..... -0.3V to +24.0V

OUT, FB, SRP, SRN to PGND ..... -0.3V to +22.0V

BST1, BST2 to AGND..... -0.3V to +26.0V

BST1 to LX1, BST2 to LX2 ..... -0.3V to +2.2V

POKB/INTB, FPWM to AGND, PGND..... -0.3V to V_{IO}+0.3V

SCL, SDA to AGND, PGND..... -0.3V to V_{IO}+0.3V

V_L, V_{IO}, SEL, EN to AGND, PGND ..... -0.3V to +2.0V

PGND to AGND .....-0.3V to +0.3V

Continuous Power Dissipation.....

WLP Package (T_A = +70°C, derate 23.2mW/°C above +70°C (Note 1)) 1856mW

Maximum Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (Reflow) .....+260°C

Note 1: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

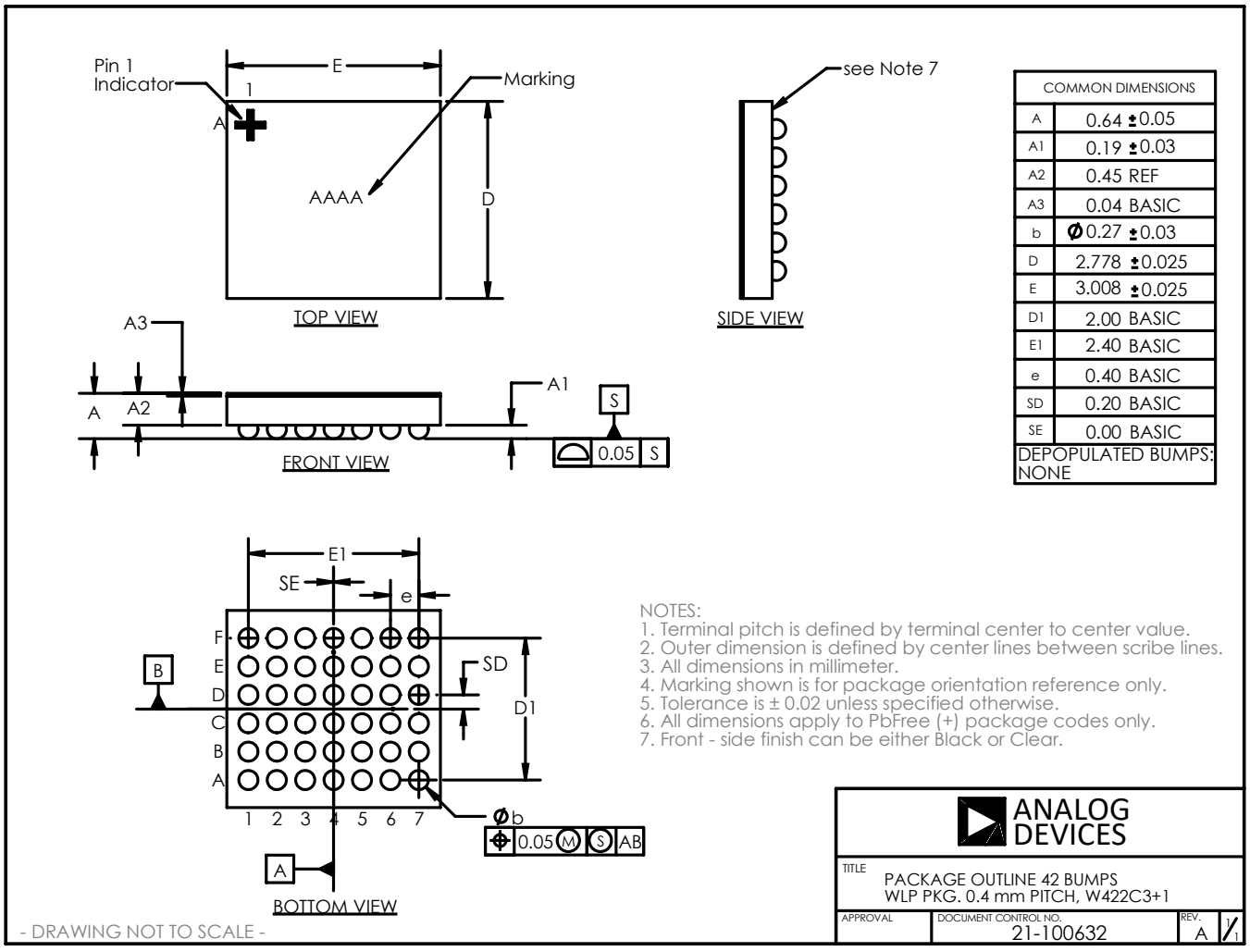
Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE
Input Voltage Range	V_{IN}		2.5V to 22V
Output Voltage Range	V_{OUT}	Internal Feedback	3.2V to 16V
		External Feedback	3V to 20V
Output Current Range	I_{OUT}	For continuous operation at 6A, the junction temperature (T_J) is limited to +105ºC. If the junction temperature is higher than 105ºC, the expected lifetime at 6A continuous operation is derated.	0A to 6A
Junction Temperature Range	T_J		-40°C to +125°C
Ambient Temperature Range	T_A		-40°C to +85°C

Package Information

42 WLP

Package Code	W422C3+1
Outline Number	21-100632
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	43.1°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	2.778 ±0.025
E	3.008 ±0.025
D1	2.00 BASIC
E1	2.40 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 42 BUMPS
WLP PKG. 0.4 mm PITCH, W422C3+1

APPROVAL | DOCUMENT CONTROL NO. 21-100632 | REV. A | 1/1

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Voltage Range	V_{IN}			2.5		22	V
Input Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		2.3	2.4	2.5	V
Input UVLO Hysteresis	V_{UVLO_HYS}	$V_{UVLO\_R} - V_{UVLO\_F}$			300		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = -40°C to +85°C			2	5.5	µA
Quiescent Supply Current	I_Q	EN = HIGH, R_{SEL} = short to GND, no switching	MAX77859B, FPWM = 0 (SKIP mode), T_J = -40°C to +85°C		60	100	µA
			MAX77859A, FPWM = 0 (SKIP mode)		300	500	
			FPWM = 1 (FPWM mode)		5		mA
OUTPUT VOLTAGE							
Output Voltage Regulation Range	V_{OUT}	Using internal feedback resistors		3.2		16	V
		Using external feedback resistors		3.0		20	
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 2.5V to 22V, V_{OUT} = 3.2V to 16V, I_{OUT} = 0mA, using internal feedback resistors	FPWM = 0 (SKIP mode)	-1		+4.5	%
			FPWM = 1 (FPWM mode)	-2		+1.5	
FB Accuracy	V_{FB_ACC}	V_{IN} = 2.5V to 22V, VREF[9:0] = 0x0A0 to 0x320		-2		+1.5	%
V_L INTERNAL SUPPLY							
V_L Regulator Voltage	V_{VL}			1.65	1.8	1.89	V
V_{IO} SUPPLY							
V_{IO} Voltage Range	V_{VIO}			1.08		2.0	V
V_{IO} Valid Threshold	$V_{VIO\_VALID\_R}$	V_{IO} Rising		0.965	1.02	1.08	V
	$V_{VIO\_VALID\_F}$	V_{IO} Falling		0.85	0.9	0.955	
V_{IO} Bias Current	I_{VIO}	No I^2C interface (SDA and SCL unconnected)				2.0	µA
		$f_{SCL} = f_{SDA}$ = 1MHz			50		
ENABLE							
EN Input LOW Voltage	V_{EN_IL}					0.4	V
EN Input HIGH Voltage	V_{EN_IH}			0.9			V
EN Internal Pulldown Current	I_{EN_PD}	EN = HIGH			0.1		µA

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-OK							
POK Output LOW Voltage	V_{POK_OL}	I_{POK} = 1mA				0.3	V
POK Rising Threshold	V_{POK_R}	V_{OUT} rising, expressed as percentage of target V_{OUT} voltage		90	93		%
POK Falling Threshold	V_{POK_F}	V_{OUT} falling, expressed as percentage of target V_{OUT} voltage			85		%
THERMAL PROTECTION							
Thermal Shutdown Threshold	T_{SHDN_R}	T_J rising (*Note 2*)			150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}	$T_{SHDN\_R} - T_{SHDN\_F}$ (*Note 2*)			15		°C
BUCK-BOOST REGULATOR							
Switching Frequency	f_{SW}	I_{OUT} = 0mA, FPWM = 1 (FPWM mode)	FREQ[1:0] = 00	1.10	1.20	1.30	MHz
			FREQ[1:0] = 01 (default)	1.38	1.50	1.62	
			FREQ[1:0] = 10	1.66	1.80	1.94	
			FREQ[1:0] = 11	1.93	2.10	2.27	
Startup Delay Time	t_{SUDLY}	(*Note 2*)			100		µs
Soft-Start Time	t_{SS}	Measured from OUT start ramping to stop ramping during startup, C_{OUT} = 44µF, I_{OUT} = 0mA (*Note 2*)			1.7		ms
Soft-start Switching Current Limit	I_{LIM_SS}	ILIM[2:0] = 100, 101, 110, or 111 ($I_{LIM} \leq$ 3.8A)			I_{LIM}		A
Soft-start Switching Current Limit	I_{LIM_SS}	ILIM[2:0] = 000, 001, 010, or 011 (I_{LIM} > 3.8A)			3.8		A
High Side Switching Current Limit	I_{LIM}	ILIM[2:0] = 000 (*Note 2*)		6.63	7.80	8.97	A
		ILIM[2:0] = 001 (I^2C only, not available with R_{SEL}) (*Note 2*)			6.80		
		ILIM[2:0] = 010 (*Note 2*)		4.93	5.80	6.67	
		ILIM[2:0] = 011 (I^2C only, not available with R_{SEL}) (*Note 2*)			4.80		
		ILIM[2:0] = 100 (*Note 2*)		3.23	3.80	4.37	
		ILIM[2:0] = 101 (I^2C only, not available with R_{SEL}) (*Note 2*)			2.80		
		ILIM[2:0] = 110 (*Note 2*)		1.70	2.00	2.30	
		ILIM[2:0] = 111 (I^2C only, not available with R_{SEL}) (*Note 2*)			1.20		
Valley Current Limit	I_{LIM_VALLEY}	ILIM[2:0] = 000 or 001 (*Note 2*)			3.8		A
		ILIM[2:0] = 010 or 011 (*Note 2*)			2.73		

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		ILIM[2:0] = 100 or 101 (*Note 2*)			1.5		
		ILIM[2:0] = 110 or 111 (*Note 2*)			0.35		
Skip Mode Switching Current Limit	I_{LIM_SKIP}	FPWM = 0 (SKIP mode) (*Note 2*)			1.2		A
Output Current Limit	I_{OUT_LIM}	R_{SENSE} = 10mΩ	IOUTLIM[6:0] = 0x13, code clamped below this level		1		A
			IOUTLIM[6:0] = 0x3B, default value		3		
			IOUTLIM[6:0] = 0x63, code clamped above this level		5		
Output Current Limit Range	I_{OUT_LIM}	R_{SENSE} = 10mΩ	IOUTLIM[6:0] = 0x13 to 0x63	1		5	A
Current Loop Regulation Voltage	V_{SR}	Measured across SRP and SRN, R_{SENSE} = 10mΩ, IOUTLIM[6:0] = 0x3B (3A)		28		32	mV
Line Regulation	$\Delta V/V_{IN}$	V_{IN} = 2.5V to 22V, V_{OUT} = 5V, I_{OUT} = 0mA and 1A (Note 2)			±0.2		%/V
Load Regulation	$\Delta V/V_{OUT}$	V_{IN} ≥ 4V, V_{OUT} = 5V, I_{OUT} = 0mA to 3A (Note 2)			±0.6		%/A
Internal Reference Voltage	V_{REF}	VREF[9:0] = 0x0A0, code clamped below this level			0.19531		V
		VREF[9:0] = 0x0FA, default value			0.30518		
		VREF[9:0] = 0x320, code clamped above this level			0.97656		
Internal Reference Voltage Programmable Range	V_{REF}	VREF[9:0] = 0x0A0 to 0x320		0.19531		0.97656	V
Internal Reference DVS Ramp Rate	$\Delta V_{REF}/\Delta t$	SLEW_RATE[1:0] = 00 (default)	FREQ[1:0] = 00		3/2		mV/µs
			FREQ[1:0] = 01 or 10		1		
			FREQ[1:0] = 11		4/5		
		SLEW_RATE[1:0] = 01			1/2		
		SLEW_RATE[1:0] = 10			1/4		
		SLEW_RATE[1:0] = 11			1/8		
FB Input Leakage Current	I_{FB_LK}			-1		+1	µA
High Side MOSFET On Resistance	R_{DSON_HS}	IN to LX1, LX2 to OUT, T_J = -40°C to +85°C			20	35	mΩ

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Side MOSFET On Resistance	R_{DSON_LS}	LX1 to PGND, LX2 to PGND, T_J = -40°C to +85°C		20	37	mΩ
Output Active Discharge Current	I_{DISCHG}	EN = LOW or $V_{IN} < V_{UVLO\_F}$, V_{OUT} = 15V		5		mA

Note 2: Guaranteed by design. Not production tested.

Note 3: Characterized by ATE or Bench test, not production tested.

Electrical Characteristics – I²C Serial Interface

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}		0.7 x V_{VIO}			V
SCL, SDA Input LOW Voltage	V_{IL}				0.3 x V_{VIO}	V
SCL, SDA Input Hysteresis	V_{HYS}	Fast mode/Fast-mode plus	0.05 x V_{VIO}			V
		High-speed mode	0.1 x V_{VIO}			
SDA Output LOW Voltage	V_{OL}	I_{SINK} = 2mA (Fast mode/Fast-mode plus) or 3mA (High-speed mode)			0.2 x V_{VIO}	V
SCL, SDA Input Capacitance	C_I	(*Note 2*)			10	pF
SCL, SDA Input Leakage Current	I_{LK}		-10	0.001	+10	µA
TIMING (FAST MODE)						
Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		1.3			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.6			µs
SCL LOW Period	t_{LOW}		1.3			µs
SCL HIGH Period	t_{HIGH}		0.6			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.6			µs
DATA Setup Time	T_{SU_DATA}		100			ns
SCL, SDA Receiving Rise Time	t_{R_REV}		20		300	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO}/ 5.5V)		300	ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				900	ns
Data Valid Acknowledge Time	t_{VD_ACK}				900	ns
Bus Capacitance	C_B	(*Note 2*)			400	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING (FAST-MODE PLUS)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.26			µs
DATA Setup Time	T_{SU_DATA}		50			ns
SCL, SDA Receiving Rise Time	t_{R_REV}				120	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO}/ 5.5V)		120	ns
Setup Time for STOP condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				450	ns
Data Valid Acknowledge Time	t_{VD_ACK}				450	ns
Bus Capacitance	C_B	(*Note 2*)			550	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns
TIMING (HIGH-SPEED MODE, BUS CAPACITANCE = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_START}		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Setup Time REPEATED START Condition	t_{SU_START}		160			ns
DATA Hold Time	t_{HD_DATA}				95	ns
DATA Setup Time	T_{SU_DATA}		10			ns
SCL, SDA Receiving Rise Time	t_{R_REV}		10		50	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		10		50	ns

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B	(*Note 2*)			100	pF
Pulse Width of Suppressed Spikes	t_{SP}				30	ns

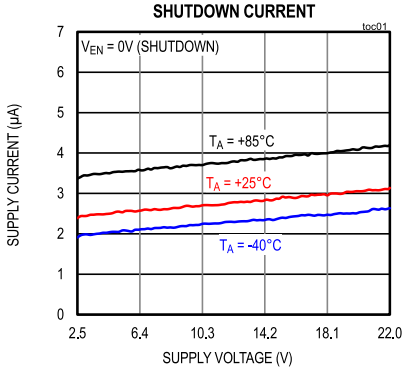
Note 2: Guaranteed by design. Not production tested.

Note 3: Characterized by ATE or Bench test, not production tested.

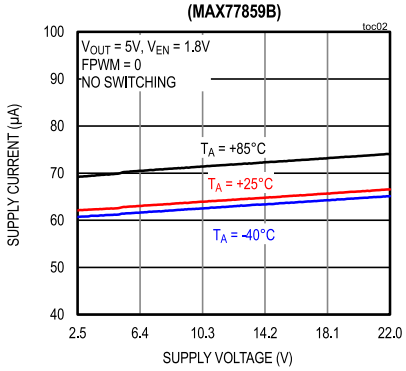
Typical Operating Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

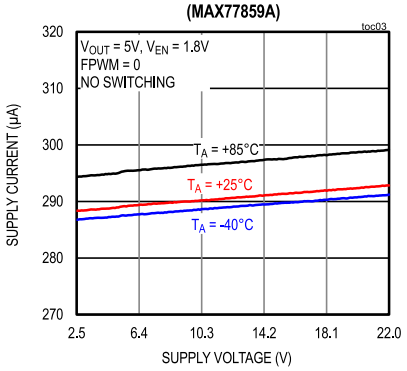
SHUTDOWN CURRENT



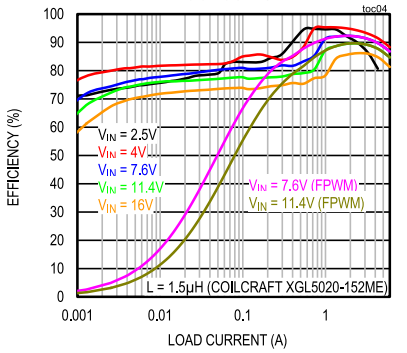
QUIESCENT CURRENT (MAX77859B)



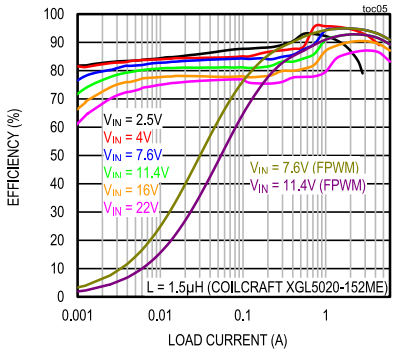
QUIESCENT CURRENT (MAX77859A)



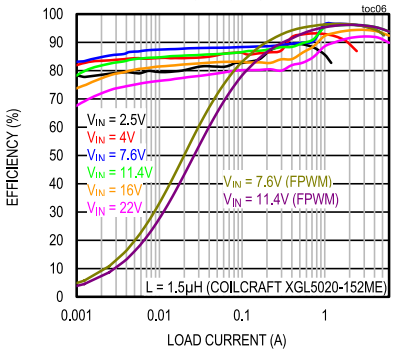
EFFICIENCY 3.3V OUTPUT



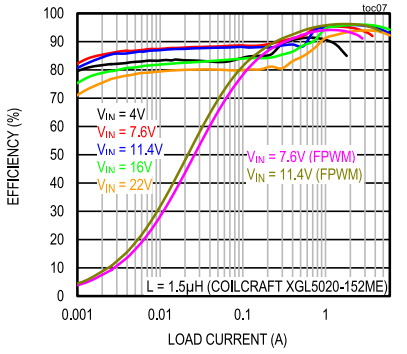
EFFICIENCY 5V OUTPUT



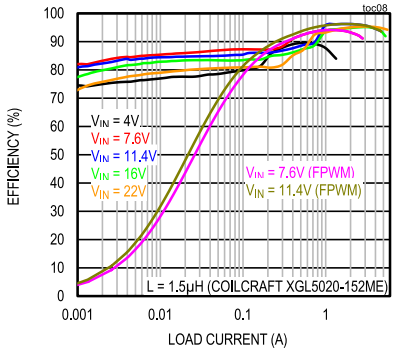
EFFICIENCY 9V OUTPUT



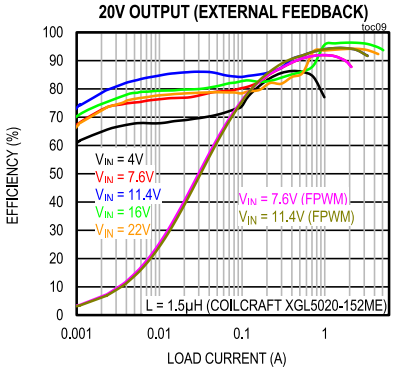
EFFICIENCY 12V OUTPUT



EFFICIENCY 15V OUTPUT



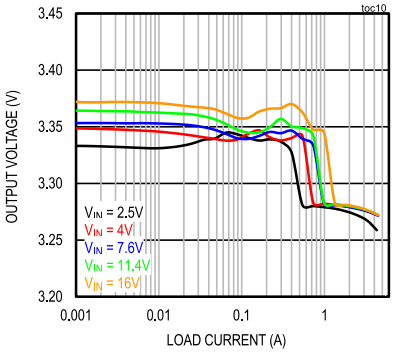
EFFICIENCY 20V OUTPUT (EXTERNAL FEEDBACK)



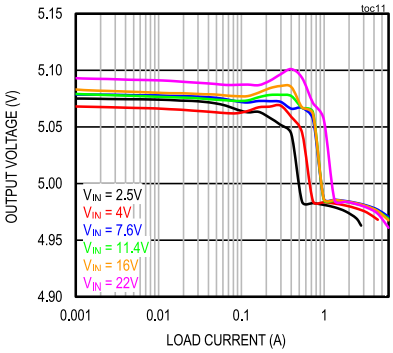
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

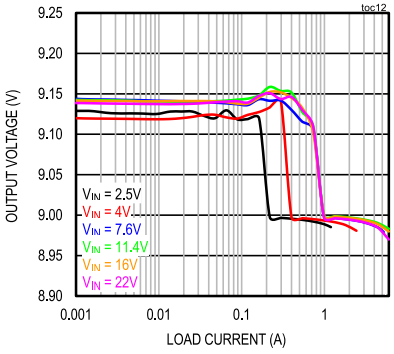
LOAD REGULATION
3.3V OUTPUT



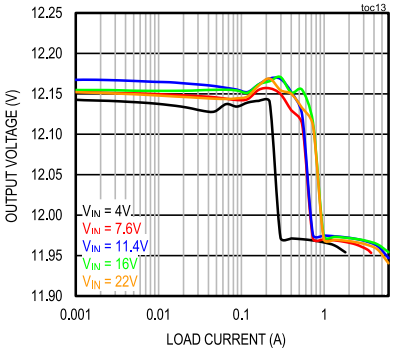
LOAD REGULATION
5V OUTPUT



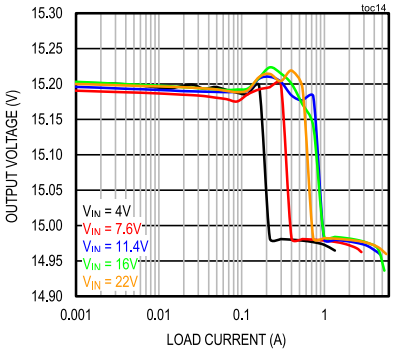
LOAD REGULATION
9V OUTPUT



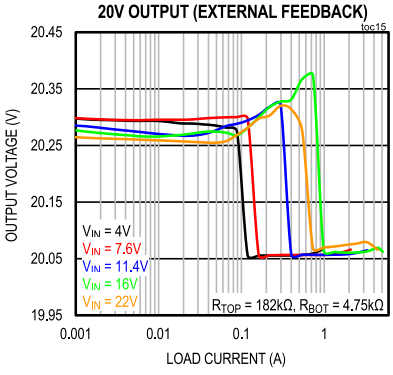
LOAD REGULATION
12V OUTPUT



LOAD REGULATION
15V OUTPUT



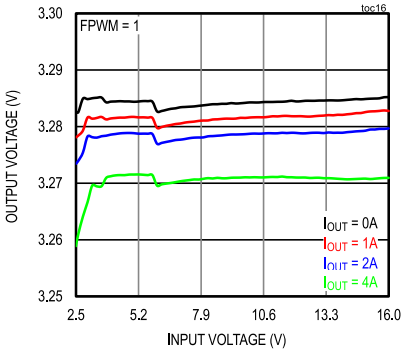
LOAD REGULATION
20V OUTPUT (EXTERNAL FEEDBACK)



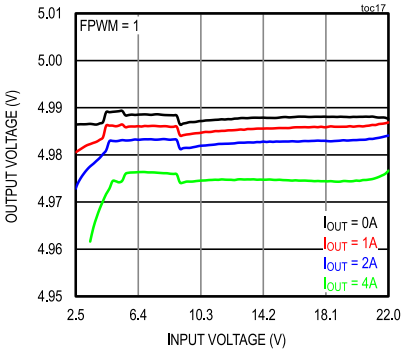
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

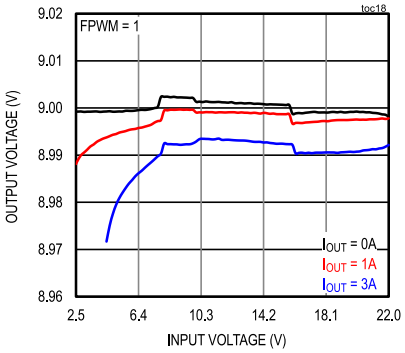
LINE REGULATION
3.3V OUTPUT



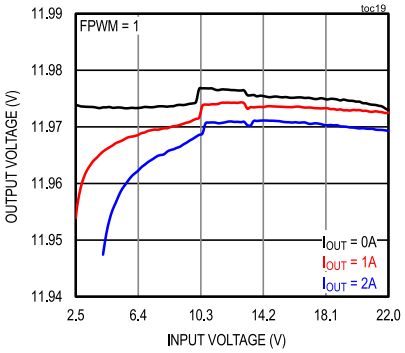
LINE REGULATION
5V OUTPUT



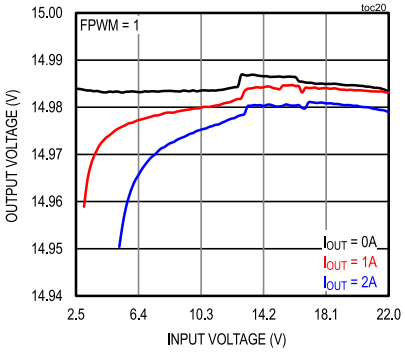
LINE REGULATION
9V OUTPUT



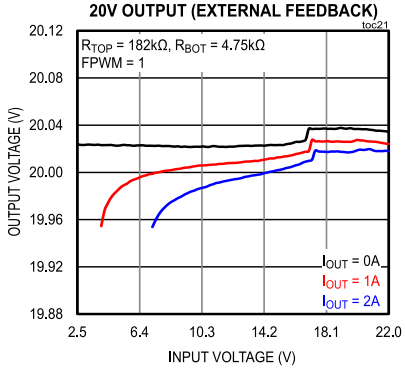
LINE REGULATION
12V OUTPUT



LINE REGULATION
15V OUTPUT



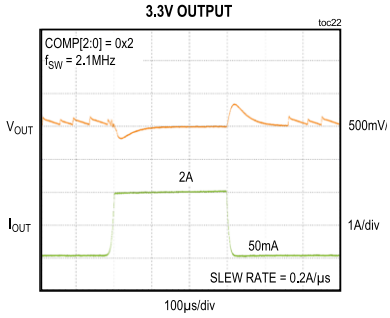
LINE REGULATION
20V OUTPUT (EXTERNAL FEEDBACK)



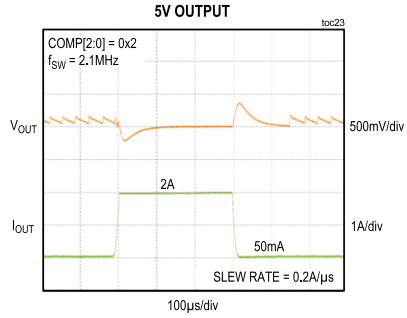
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

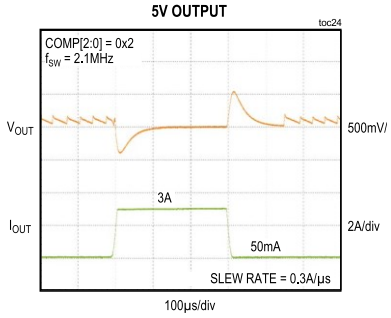
LOAD TRANSIENT RESPONSE
3.3V OUTPUT



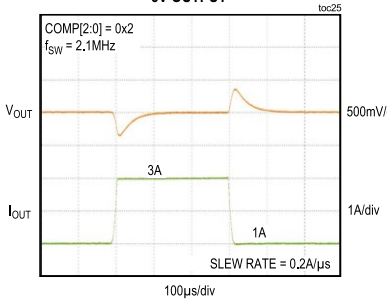
LOAD TRANSIENT RESPONSE
5V OUTPUT



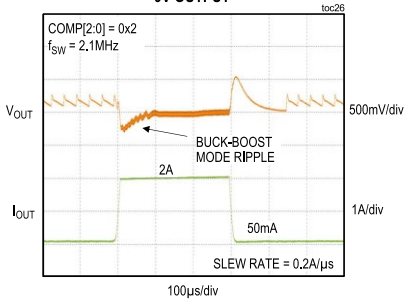
LOAD TRANSIENT RESPONSE
5V OUTPUT



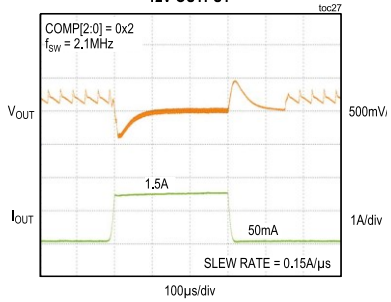
LOAD TRANSIENT RESPONSE
5V OUTPUT



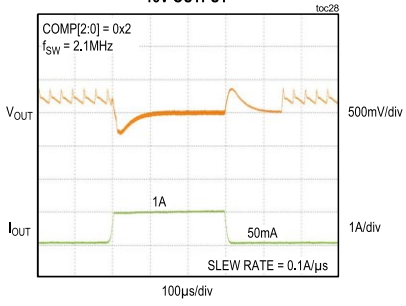
LOAD TRANSIENT RESPONSE
9V OUTPUT



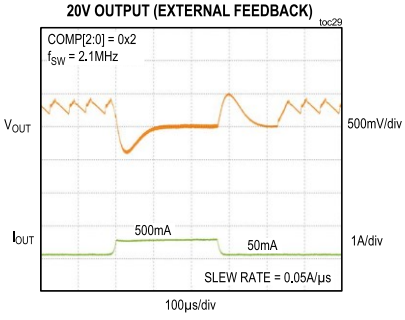
LOAD TRANSIENT RESPONSE
12V OUTPUT



LOAD TRANSIENT RESPONSE
15V OUTPUT



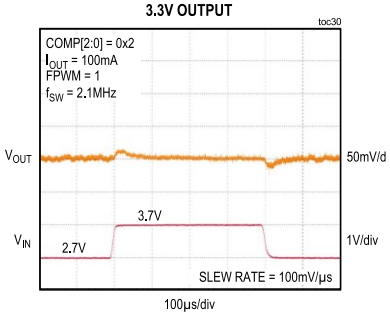
LOAD TRANSIENT RESPONSE
20V OUTPUT (EXTERNAL FEEDBACK)



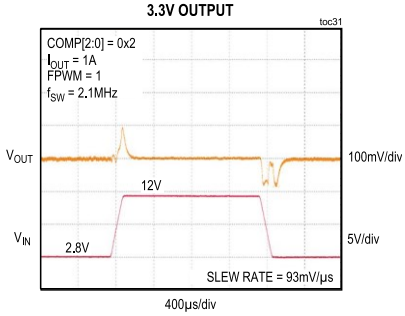
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

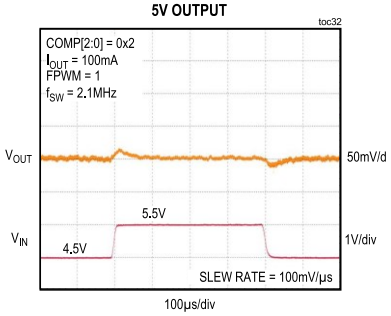
LINE TRANSIENT RESPONSE
3.3V OUTPUT



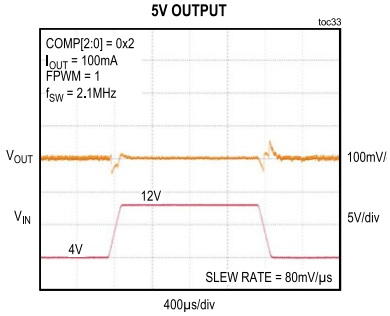
LINE TRANSIENT RESPONSE
3.3V OUTPUT



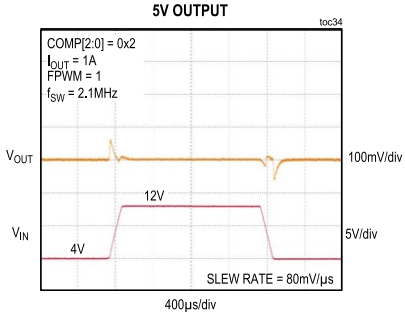
LINE TRANSIENT RESPONSE
5V OUTPUT



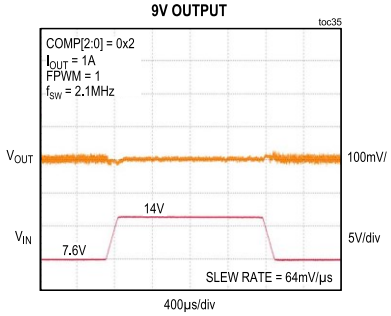
LINE TRANSIENT RESPONSE
5V OUTPUT



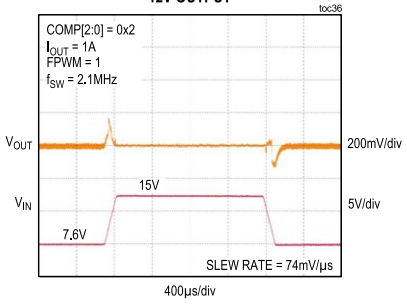
LINE TRANSIENT RESPONSE
5V OUTPUT



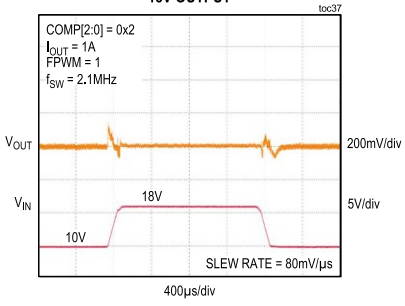
LINE TRANSIENT RESPONSE
9V OUTPUT



LINE TRANSIENT RESPONSE
12V OUTPUT



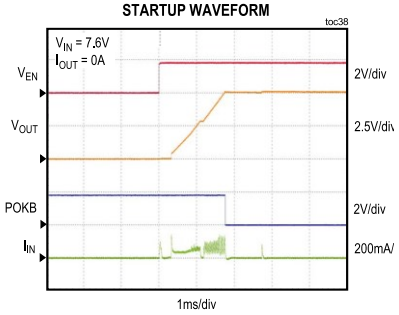
LINE TRANSIENT RESPONSE
15V OUTPUT



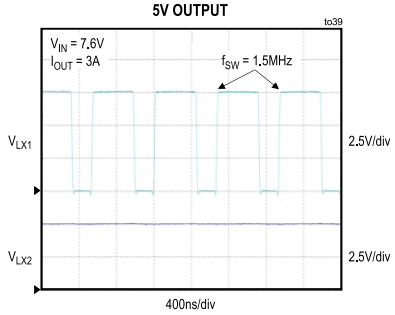
Typical Operating Characteristics (continued)

(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

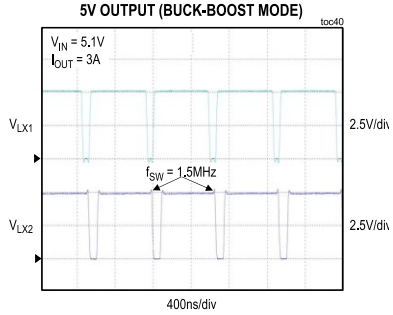
STARTUP WAVEFORM



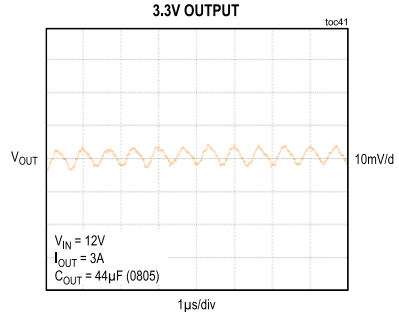
SWITCHING WAVEFORM
5V OUTPUT



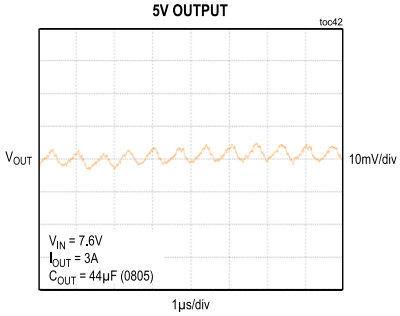
SWITCHING WAVEFORM
5V OUTPUT (BUCK-BOOST MODE)



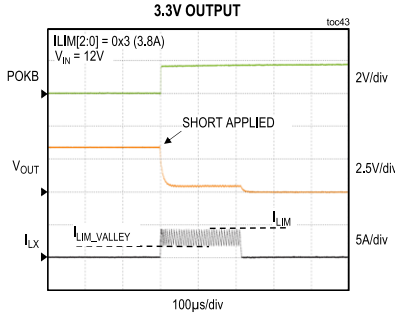
OUTPUT VOLTAGE RIPPLE
3.3V OUTPUT



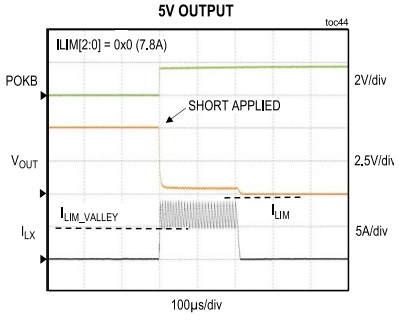
OUTPUT VOLTAGE RIPPLE
5V OUTPUT



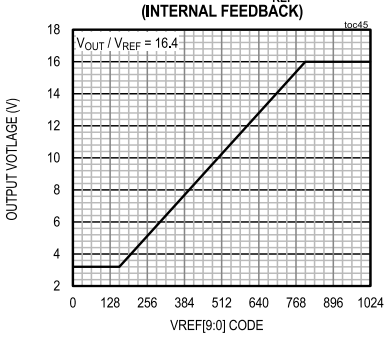
SHORT-CIRCUIT RESPONSE
3.3V OUTPUT



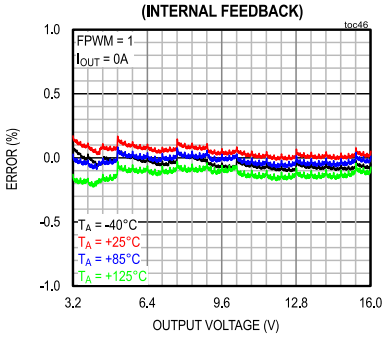
SHORT-CIRCUIT RESPONSE
5V OUTPUT



OUTPUT VOLTAGE vs. V_{REF} CODE
(INTERNAL FEEDBACK)

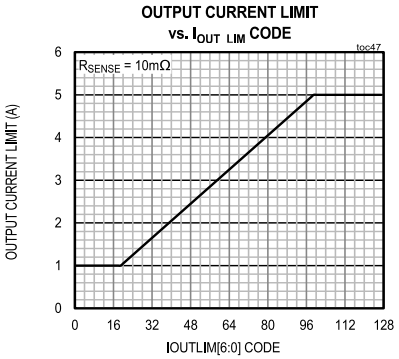


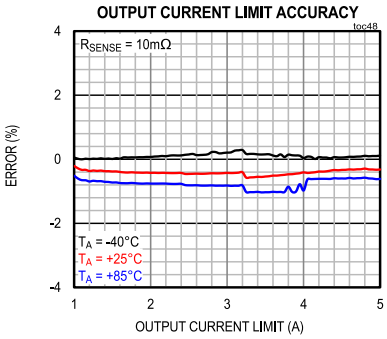
OUTPUT VOLTAGE ACCURACY
(INTERNAL FEEDBACK)

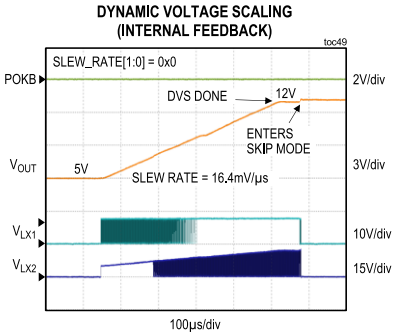


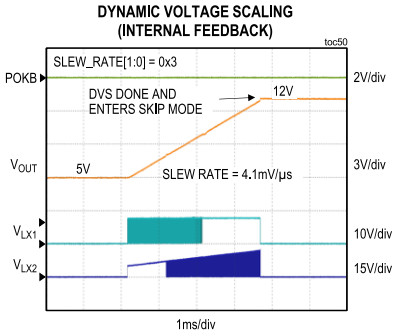
Typical Operating Characteristics (continued)

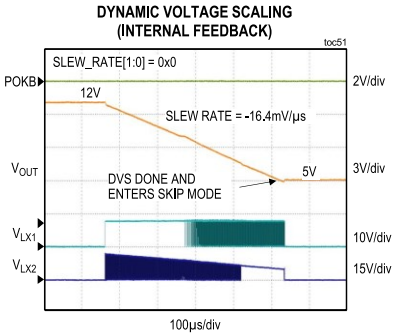
(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

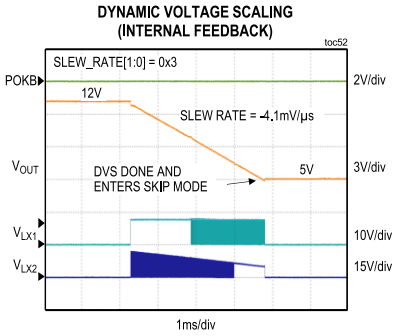






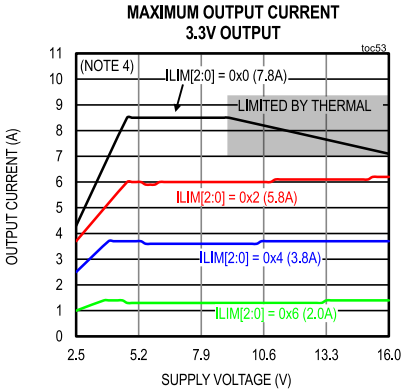


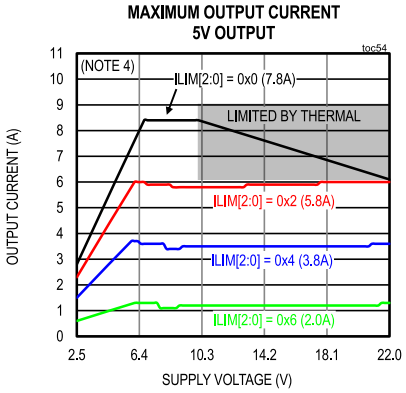


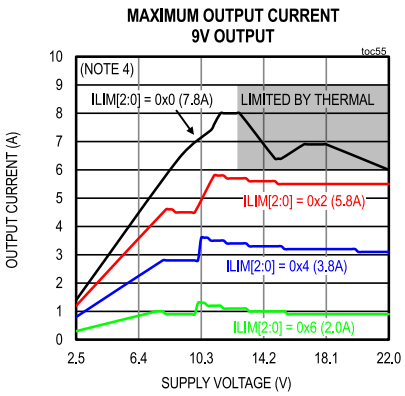


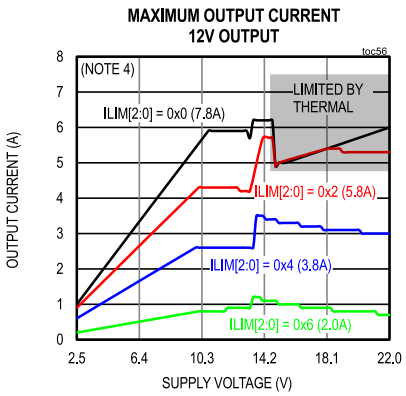
Typical Operating Characteristics (continued)

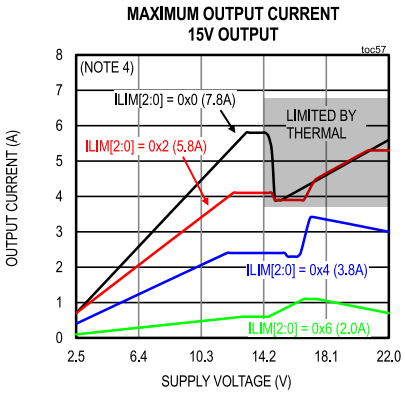
(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XGL5020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7.8A), f_{SW} = 1.5MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4:** Measurement limited by switching current limit unless otherwise noted. Actual maximum output current depends on system thermal performance.)

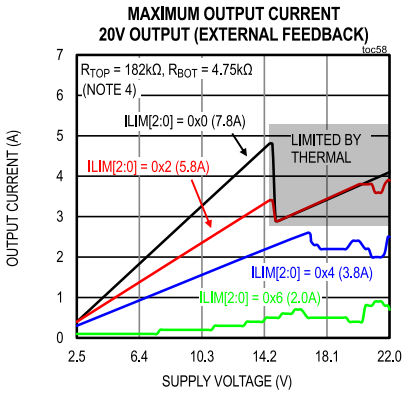










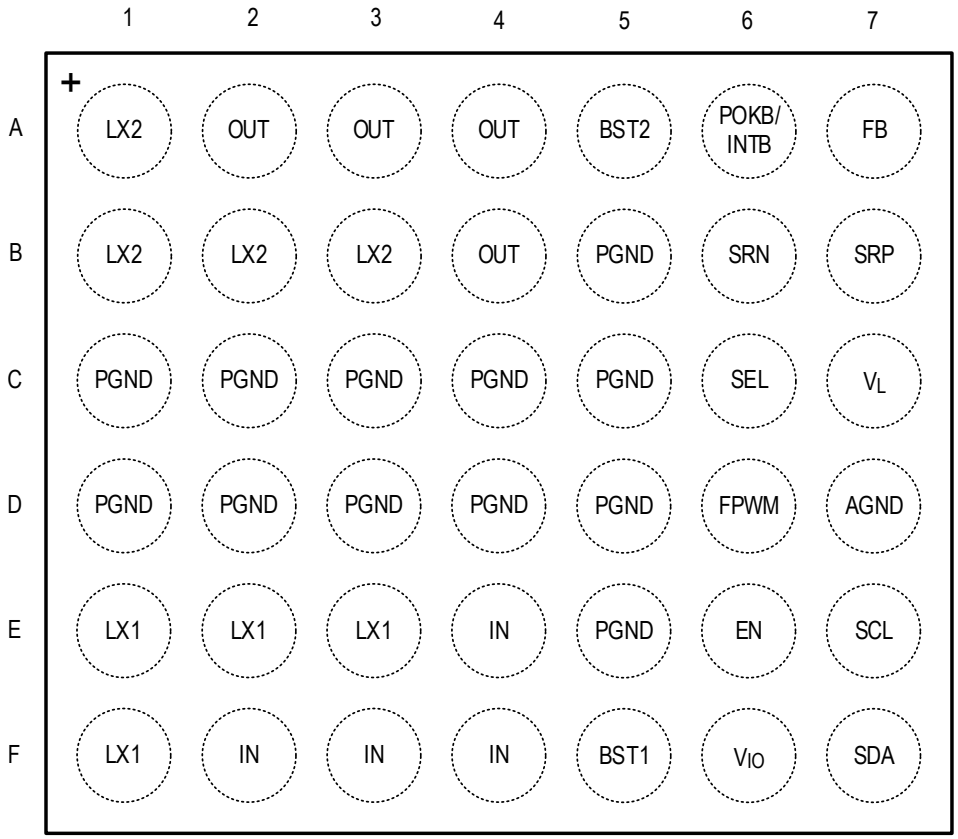


Pin Configurations

42 WLP

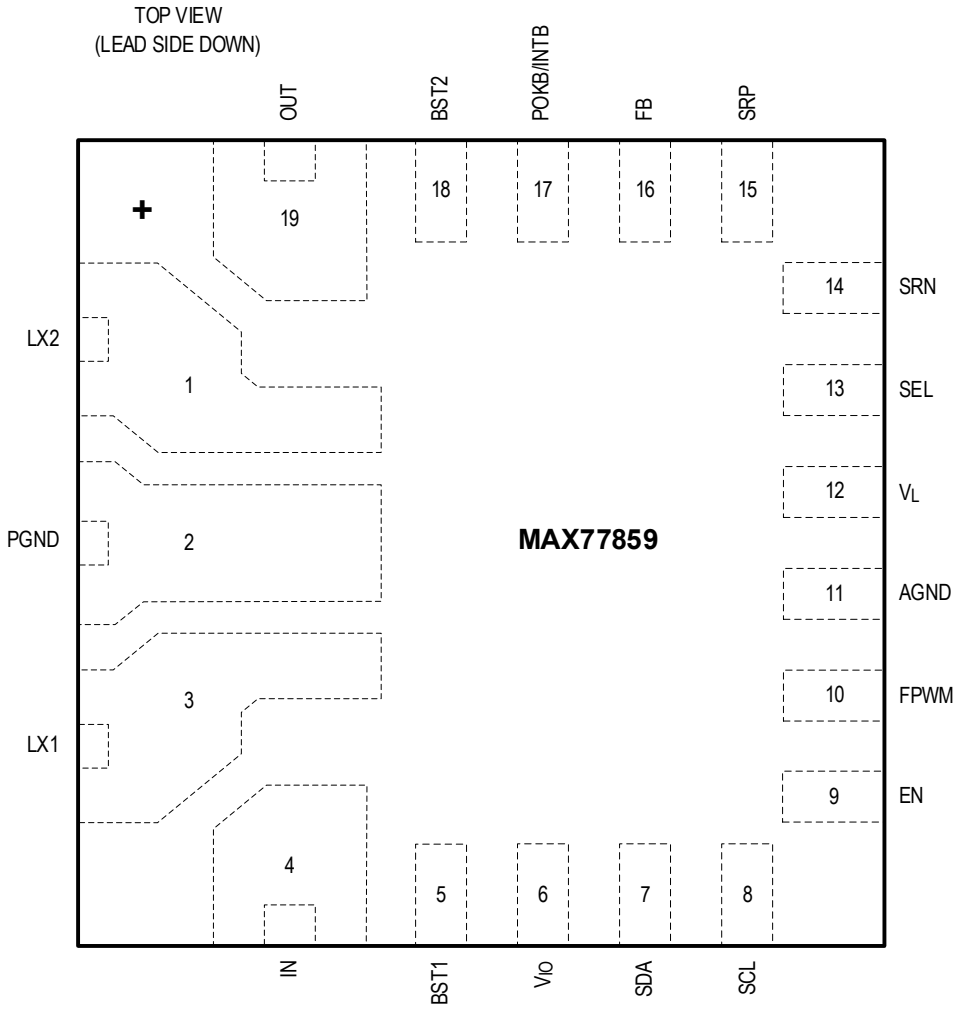
TOP VIEW
(BUMP SIDE DOWN)

MAX77859



42 WLP
(3.01mm x 2.78mm, 0.4mm PITCH)

19 FC2QFN



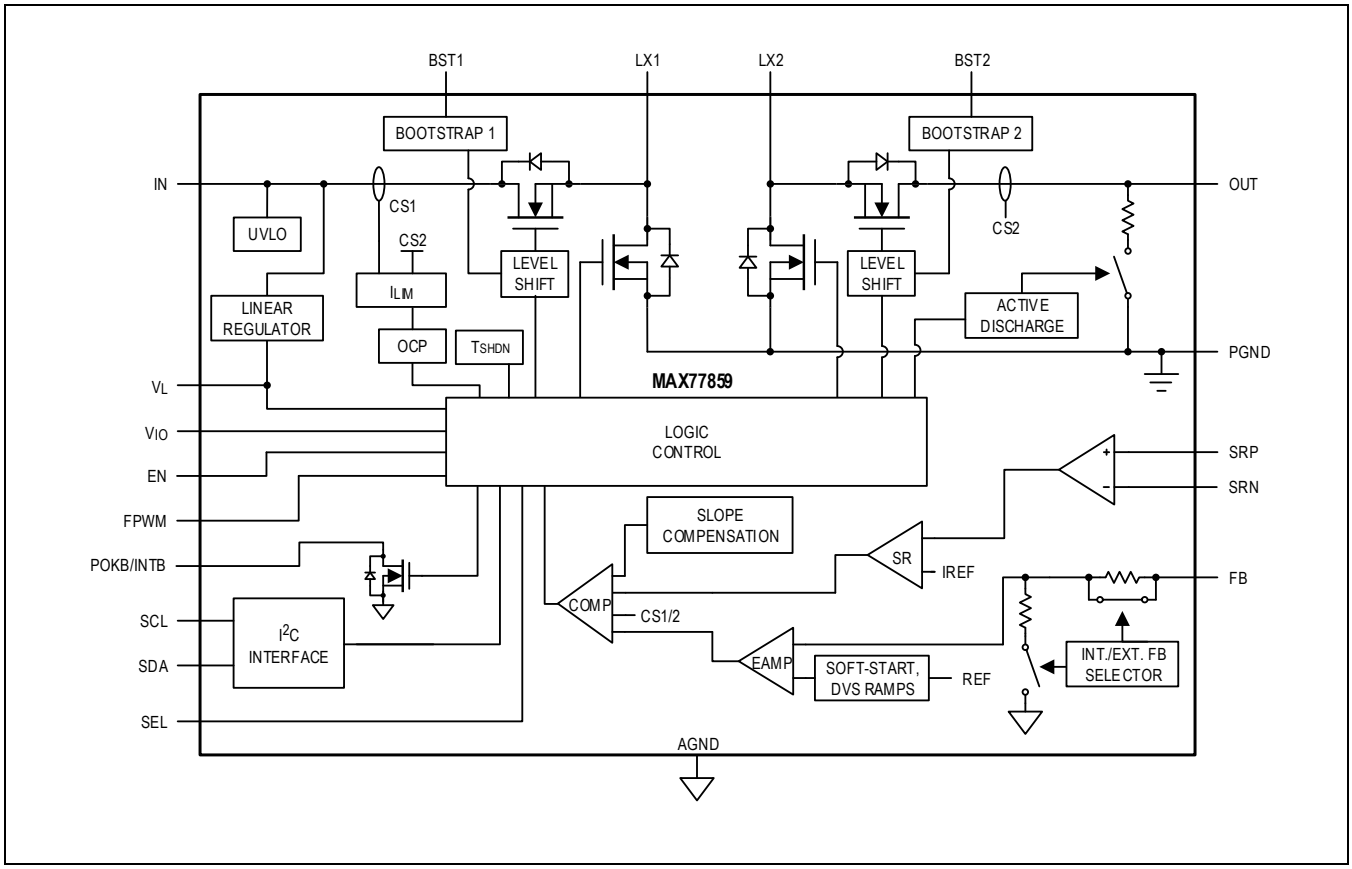
19 FC2QFN
(4.0mm x 4.0mm, 0.5mm PITCH)

Pin Descriptions

PIN		NAME	FUNCTION	Type
42 WLP	19 FC2QFN			
A1, B1, B2, B3	1	LX2	Buck-Boost Switching Node 2.	Power
B5, C1, C2, C3, C4, C5, D1, D2, D3, D4, D5, E5	2	PGND	Power Ground. Connect to AGND on the PCB. See the *PCB Layout Guidelines* section for more details.	Ground
E1, E2, E3, F1	3	LX1	Buck-Boost Switching Node 1.	Power
F5	4	BST1	LX1 High-Side FET Driver Supply. Connect a 25V 0.22µF ceramic capacitor between BST1 and LX1.	Power Input
E4, F2, F3, F4	5	IN	Buck-Boost Input. Bypass to PGND with two 35V 22µF ceramic capacitors as close as possible.	Power Input
C7	6	V_L	Low-Voltage Internal Supply. Powered from IN. Bypass to AGND with a 10V 2.2µF ceramic capacitor. Do not load this pin externally except for usage stated in *Non-I²C and Standalone Operation* section.	Analog
D7	7	AGND	Analog Ground. Connect to PGND on the PCB. See the *PCB Layout Guidelines* section for more details.	Ground
F6	8	V_{IO}	IO Voltage Supply. Bypass to AGND with a 6.3V 0.47µF ceramic capacitor. Registers are held in reset when this pin's voltage is invalid.	Power Input
E7	9	SCL	I²C Serial Interface Clock (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor.	Digital Input
F7	10	SDA	I²C Serial Interface Data (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor.	Digital I/O
E6	11	EN	Active-High Buck-Boost Enable Input. Compatible with the V_{IO} voltage domain. Pull down internally with 0.1µA current source. See *Non-I²C and Standalone Operation* section for more information if the application desires to control EN with IN (i.e., start up MAX77859 whenever IN's voltage is valid.)	Digital Input
A6	12	POKB/INTB	Active-Low Open Drain Status/Interrupts Output. Connect to V_{IO} with a 15kΩ pullup resistor. See *Power-OK (POK) and Fault Status/Interrupts* section for more details. Do not connect to this pin if not in use.	Digital Output
D6	13	FPWM	Active-High Forced-PWM Mode Control Input.	Digital Input
C6	14	SEL	Configuration Selection. Connect a resistor between SEL and AGND. See *Table 2* for resistor values and configurations.	Analog
B6	15	SRN	Sense Resistor Negative Input. Connect to the negative terminal of the 10mΩ sense resistor placed between output capacitors and load. Route SRN trace in parallel with SRP trace as short as possible and avoid noise source. When a sense resistor is not used, short to SRP pin.	Analog
B7	16	SRP	Sense Resistor Positive Input. Connect to the positive terminal of the 10mΩ sense resistor placed between output capacitors and load. Route SRP trace in parallel with SRN trace as short as possible and avoid noise source. When a sense resistor is not used, short to SRN pin.	Analog

A7	17	FB	**Using Internal Feedback Resistor:** Output Voltage Sense Input. Connect to the output at the point-of-load (close to the output capacitor). **Using External Feedback Resistors:** Output Voltage Feedback Input. Connect to the center tap of an external resistor divider from OUT to AGND to set the output voltage. See the *Output Voltage Configuration* section for more details.	Analog
A2, A3, A4, B4	18	OUT	Buck-Boost Output. Bypass to PGND with two 25V 22µF ceramic capacitors as close as possible.	Power Output
A5	19	BST2	LX2 High-Side FET Driver Supply. Connect a 25V 0.22µF ceramic capacitor between BST2 and LX2.	Power Input

Functional Diagrams



Detailed Description

General Description

The MAX77859 is a high-efficiency, high-performance buck-boost converter targeted for systems requiring a wide input voltage range (2.5V to 22V). The IC can supply up to 6A of output current in buck mode and up to 4A in boost mode (V_{IN} = 3.7V, V_{OUT} = 5V). The IC allows systems to change the output voltage dynamically through I2C serial interface. MAX77859A features I2C-adjustable output current limit with resolutions of 50mA/step (with 10mΩ sense resistance) to support USB-C PPS requirements. MAX77859B is a non-PPS version and is optimized for low quiescent current. Systems equipped with MAX77859 can provide fast-charging peripheral devices with higher output voltage, minimizing power loss across cable/connector and reducing charging time.

The IC operates either in SKIP mode or in forced-PWM (FPWM) mode, depending on the operating conditions, to optimize efficiency. The default output voltage is 5V when using internal feedback resistors. The IC can also be configured to any default output voltages between 3V and 20V when using external feedback resistors. The output voltage is adjustable dynamically (DVS) between 3.2V and 16V in 20mV steps when using internal feedback resistors or between 3V to 20V when using external feedback resistors (with step-size dependent on the external feedback resistor ratio) by programming the internal reference voltage through I2C serial interface. See the *Output Voltage Configuration* section for more information.

MAX77859A features output current limit. Using a 10mΩ sense resistor, the output current limit threshold is adjustable dynamically between 1A and 5A in 50mA steps through I2C serial interface, with a 3A default value.

The SEL pin allows a single external resistor, R_{SEL}, to connect to AGND to program the following:

- I2C Interface Target Address (4 options)
- Switching Current Limit Threshold (4 options)
- Feedback Resistor Selection (Internal or external)

The different I2C interface target addresses accommodate multiple devices in a system with a limited I2C bus. The different switching current limit thresholds allow the use of lower profiles and smaller external components optimized for a particular application. Using external feedback resistors allows for a wider output voltage range and customizable output voltages at startup. See the *SEL Pin Configuration* section for more information.

An optional I2C serial interface allows dynamic control of the following:

- Output Voltage (using Internal Reference Voltage)
- Slew Rate of Output Voltage Change (4 options)
- Output Current Limit Threshold (MAX77859A only)
- Switching Current Limit Threshold (8 options)
- Switching Frequency (4 options)
- Forced-PWM Mode Operation
- Power-OK (POK) and Fault Status/Interrupts
- Internal Compensation

The different switching frequencies provide options to improve the EMI performance by avoiding EMI-sensitive frequency bands. The I2C-programmed settings have priority over the R_{SEL}-decoded settings.

Start-Up

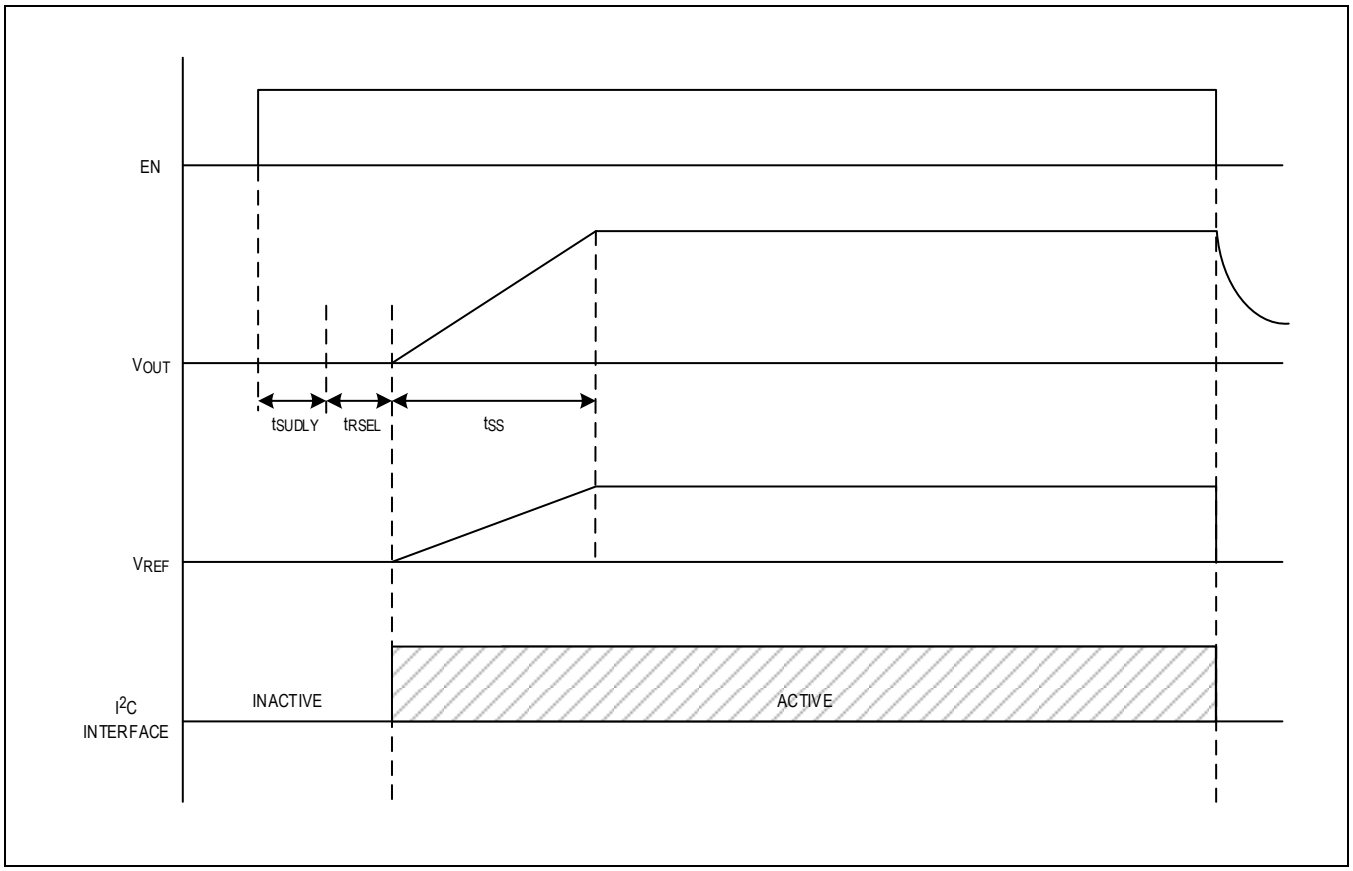


Figure 1. Start-Up Waveform

See *Figure 1* for the start-up behavior. When input voltage V_{IN} is above UVLO threshold V_{UVLO_R} and EN pin is at logic HIGH, the IC starts by first turning on the internal bias circuitry (V_L), which typically takes 100µs (t_{SUDLY}) to settle. The IC then senses the SEL pin resistance to set the I²C interface target address, switching the current limit threshold and using internal or external feedback resistors. The R_{SEL} reading takes typically 200µs (t_{RSEL}) to complete. See the *SEL Pin Configuration* section for more information. Next, the IC checks if the V_{IO} voltage is valid. If so, it activates the I²C interface and begins the buck-boost soft-start process (see ***Soft-Start*** section).

When EN toggles to logic HIGH, if the output active discharge is still active from a previous shutdown event, the IC waits for active discharge to finish before it initiates the startup sequence.

It is possible to use the internal regulator V_L to provide power to the V_{IO} pin or V_{IN} to control the EN pin. See *Non-I²C and Standalone Operation* section for more details.

Soft-Start

The MAX77859 features a soft-start to avoid a large amount of input current drawn from the system supply during startup. The default soft-start time (t_{SS}) is 1.7ms typical. During soft-start, the internal reference voltage (V_{REF}) slowly ramps up to the target value. The switching current limit threshold during soft-start is reduced to 3.8A if the I_{LIM} setting is set to be higher than such value (through R_{SEL}). If the I_{LIM} setting is set to be 3.8A or lower, then the same switching current limit threshold applies during soft-start. After the soft-start finishes, the normal switching current limit threshold applies.

Shutdown

Pull the EN pin to logic LOW to shut down the IC. In a shutdown event, the IC stops switching, resets all registers, and activates the output active discharge until the output voltage (V_{OUT}) drops below about 2.5V (typical) or after 600ms, whichever occurs sooner.

Immediate Latch-Off Conditions

The IC has a latch-off feature to protect itself under certain fault conditions by shutting down the buck-boost regulator.

Immediate Shutdown Conditions:

- IN UVLO: V_{IN} < Input UVLO Falling Threshold (V_{UVLO_F})
- V_{IO} UVLO: V_{VIO} < V_{IO} Valid Falling Threshold ($V_{VIO\_VALID\_F}$)

Latch-Off Conditions:

- Thermal Shutdown: T_J > Thermal Shutdown Rising Threshold (T_{SHDN_R}) (See *Thermal Shutdown (THS)* section)
- HARDSHORT: I_{LIM} Timer > 427µs (See *Switching Current Overcurrent Protection (SW OCP)* section)

The events in this category are associated with potentially hazardous system states. Under immediate shutdown conditions, the IC shuts down the buck-boost regulator output and the I^2C serial communication bus and resets all registers, until the system recovers from these fault conditions. Under latch-off conditions, the IC shuts down the buck-boost regulator output only, while keeping the I^2C serial communication bus active and preserving the state of the registers. To recover from latch-off, the fault condition must to be removed from the system, and a power-cycling EN pin or IN pin is required. Active discharge is engaged when the buck-boost regulator is shut down from all fault conditions except for thermal shutdown. See the *Output Active Discharge* section for more information.

Output Active Discharge

The IC includes an internal switch that provides a path to discharge the energy stored in the output capacitor to PGND. Output active discharge is activated whenever the buck-boost regulator is disabled (by a shutdown event or any conditions described in the *Immediate Latch-Off Conditions* section, except for thermal shutdown). The amount of discharge current is 5mA typical when V_{OUT} is at 15V, and it decreases as V_{OUT} decreases during the discharge. When the active discharge is enabled, the EN pin control signal is ignored. After V_{OUT} has dropped below 2.5V (typical) or the 600ms timer has expired, whichever occurs sooner, active discharge is disabled. When the buck-boost regulator operates, the internal discharging switch is disconnected from the output.

Buck-Boost Regulator

The MAX77859 buck-boost regulator utilizes a four-switch H-bridge configuration and contains buck, boost, or 3-phase operating modes. This topology maintains output voltage regulation over the input voltage range. The buck-boost regulator is ideal in up to 4-cell Li-ion battery-powered applications, providing 3V to 20V of the output voltage range. High switching frequency and a unique control algorithm allow for the smallest solution size, low output noise, and the highest efficiency across a wide input voltage and output current range.

Buck-Boost Control Scheme

The buck-boost regulator operates using a fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor. The default switching frequency is 1.5MHz. The bitfield FREQ[1:0] sets the switching frequency. The different switching frequencies provide options to avoid EMI-sensitive frequency bands and improve EMI performance.

The H-bridge topology has three switching phases, as shown in *Figure 2*:

- Φ1 switch phase (HS1 = ON, LS2 = ON) stores energy in the inductor and ramps up inductor current at a rate proportional to input voltage divided by inductance: V_{IN}/L.
- Φ2 switch phase (HS1 = ON, HS2 = ON) ramps inductor current up (in buck mode) or down (in boost mode) at a rate proportional to the differential voltage across the inductor: $(V_{IN} – V_{OUT})/L$
- Φ3 switch phase (LS1 = ON, HS2 = ON) releases energy from the inductor and ramps down inductor current at a rate proportional to output voltage divided by inductance: $-V_{OUT}/L$.

Boost mode operation (V_{IN} < V_{OUT}) utilizes Φ1 and Φ2 within a single clock period. See the representation of the inductor current waveform for boost mode operation in *Figure 2*. Buck mode operation (V_{IN} > V_{OUT}) utilizes Φ2 and Φ3 within a single clock period. See the representation of the inductor current waveform for buck mode operation in *Figure 2*. 3-Phase mode operation (V_{IN} ≈ V_{OUT}) utilizes Φ1, Φ2, and Φ3 within single clock period. See the representation of the inductor current waveform for 3-phase mode operation in *Figure 2*.

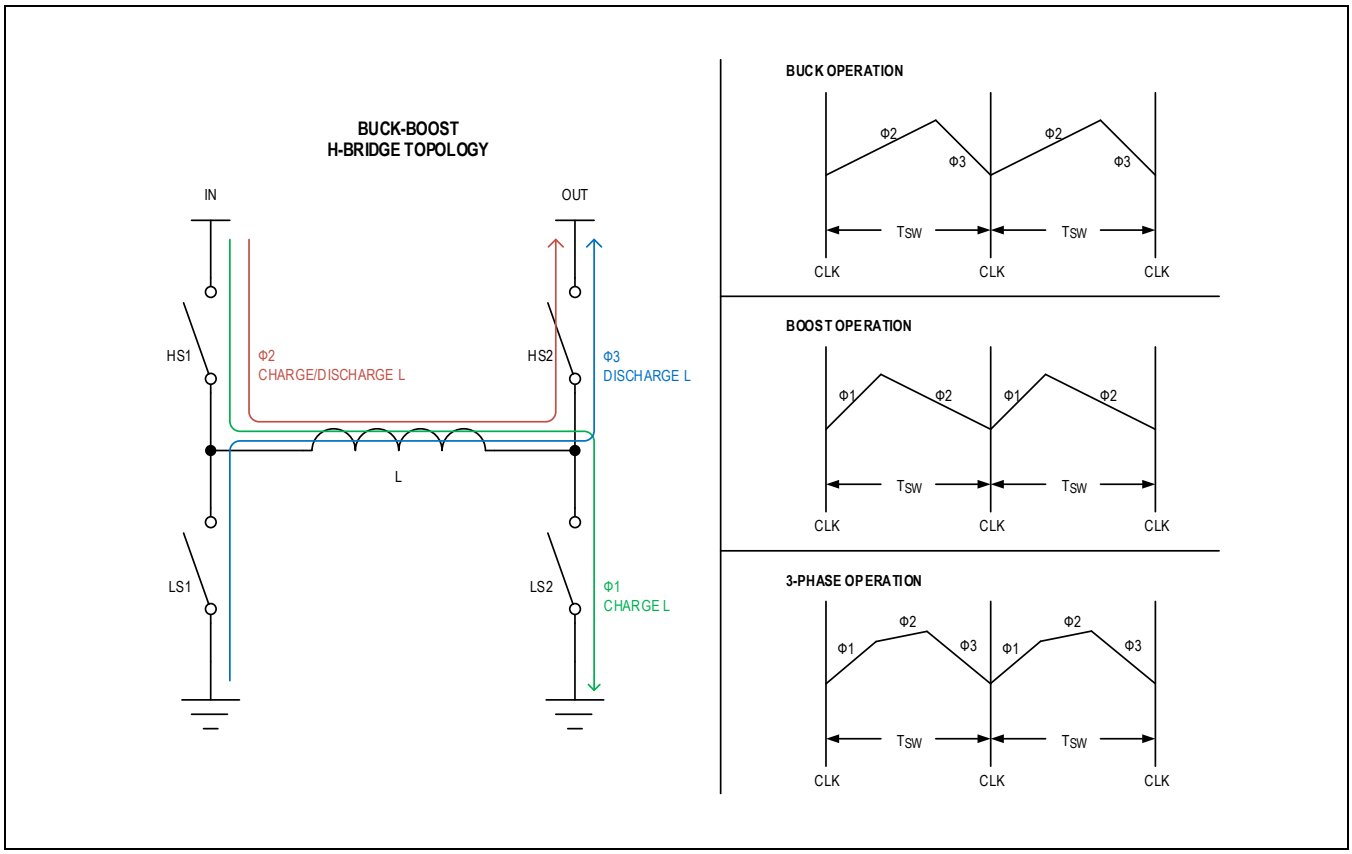


Figure 2. Buck-Boost H-Bridge Topology

SKIP Mode and Forced-PWM (FPWM) Mode

The IC automatically enters SKIP mode operation at no load or light load conditions to improve efficiency. In SKIP mode, output voltage V_{OUT} is regulated between the SKIP mode upper threshold (V_{SKIP_UPPER}) and lower threshold (V_{SKIP_LOWER}), which are typically 3% and 1% above the output voltage target (V_{TARGET}), respectively. The IC automatically transitions from SKIP mode to PWM mode depending on the output load condition and input/output voltage ratio.

Another way to enable PWM mode operation is by asserting logic HIGH on the FPWM pin or by writing 1 to FPWM[0] bitfield through I^2C serial interface. This forces PWM mode operation regardless of output load current. Forced-PWM (FPWM) mode benefits applications where the lowest output ripple is required, whereas SKIP mode helps maximize the buck-boost regulator's efficiency at light loads.

Regardless of the FPWM pin or FPWM[0] bitfield setting, the IC enters FPWM mode when V_{OUT} is changed to a different V_{TARGET} (DVS) to speed up the transition time. During DVS events transitioning from a higher V_{OUT} to a lower one, the IC enters FPWM mode when V_{OUT} falls below V_{SKIP_LOWER} of the old V_{TARGET} and stays in FPWM mode until V_{OUT} falls below V_{SKIP_UPPER} of the new V_{TARGET}. Then V_{OUT} naturally drops based on the output load condition until it falls to V_{SKIP_LOWER}, where the SKIP mode switching cycle resumes. *Figure 3* shows such an operation during DVS.

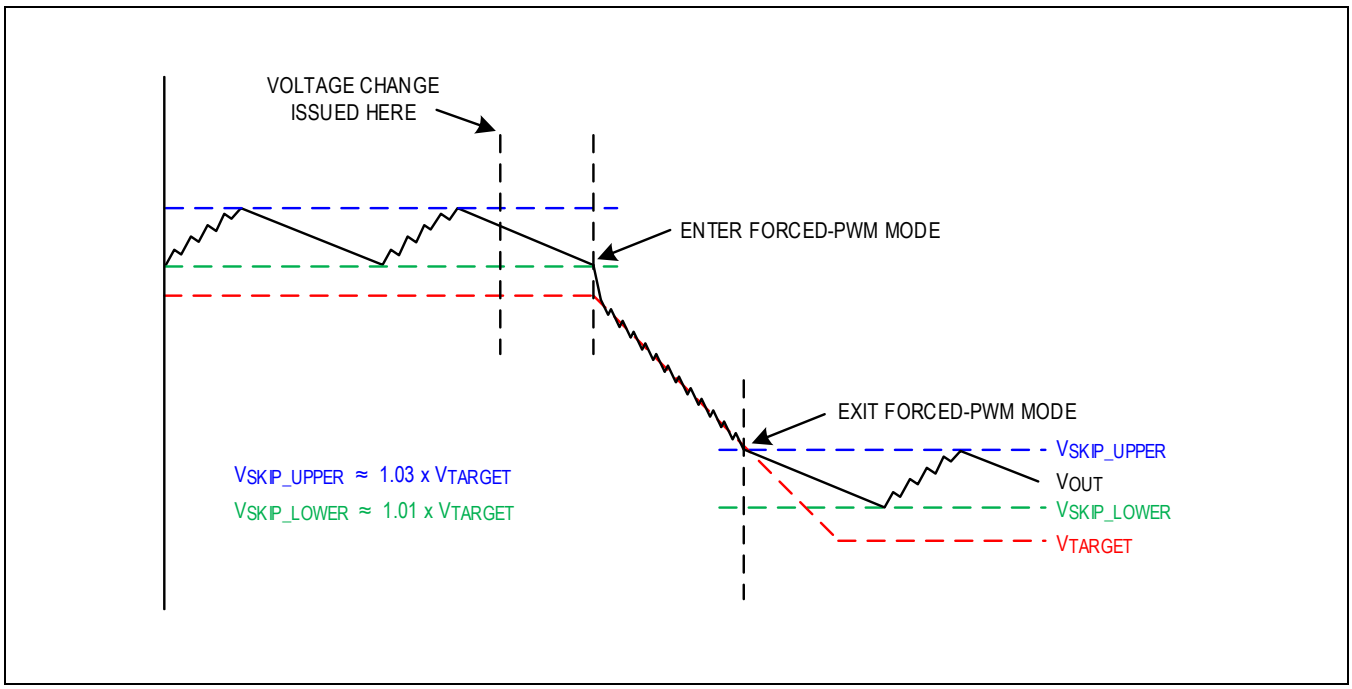


Figure 3. SKIP Mode Threshold and FPWM Mode Operation during DVS

Output Voltage Configuration

The IC supports a wide output voltage range between 3.2V and 16V when using internal feedback resistors and between 3.0V and 20V when using external feedback resistors. The use of internal feedback resistors provides the benefits of fewer external components and less overall solution size, while the use of external feedback resistors allows for a wider output voltage range and customizable output voltage V_{OUT} at startup without using I^2C serial interface. The selection between using internal or external feedback resistors is configurable by R_{SEL}. See the *SEL Pin Configuration* section for more information.

Internal Feedback Resistor Configuration

When using internal feedback resistors, the V_{OUT} range is between 3.2V and 16V in 20mV steps. Default V_{OUT} is 5V (V_{REF} = 0.30518V). Use appropriate R_{SEL} value to configure the IC for using internal feedback resistors, and connect the FB pin directly to the OUT pin at the local output capacitor.

External Feedback Resistor Configuration

When using external feedback resistors, the V_{OUT} range is between 3.0V and 20V. The actual output voltage range and step size depending on the external feedback resistor ratio. Use appropriate R_{SEL} value to configure the IC for using external feedback resistors and connect a resistor divider between OUT, FB, and AGND, as shown in *Figure 4*. If V_{OUT} is 6V or below, it is also recommended to add a 10pF feedforward capacitor (C_{FF}) in parallel with the top feedback resistor (R_{TOP}). Choose R_{TOP} (from OUT to FB) between 150kΩ and 330kΩ. Resistors with 1% tolerance (or better) are highly recommended to keep the accuracy of V_{OUT}. Calculate the value of R_{BOT} (from FB to AGND) for a desired V_{OUT} within the operating range at startup with the following equation:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{V_{OUT} - V_{REF}}$$

where V_{REF} is the default internal reference voltage.

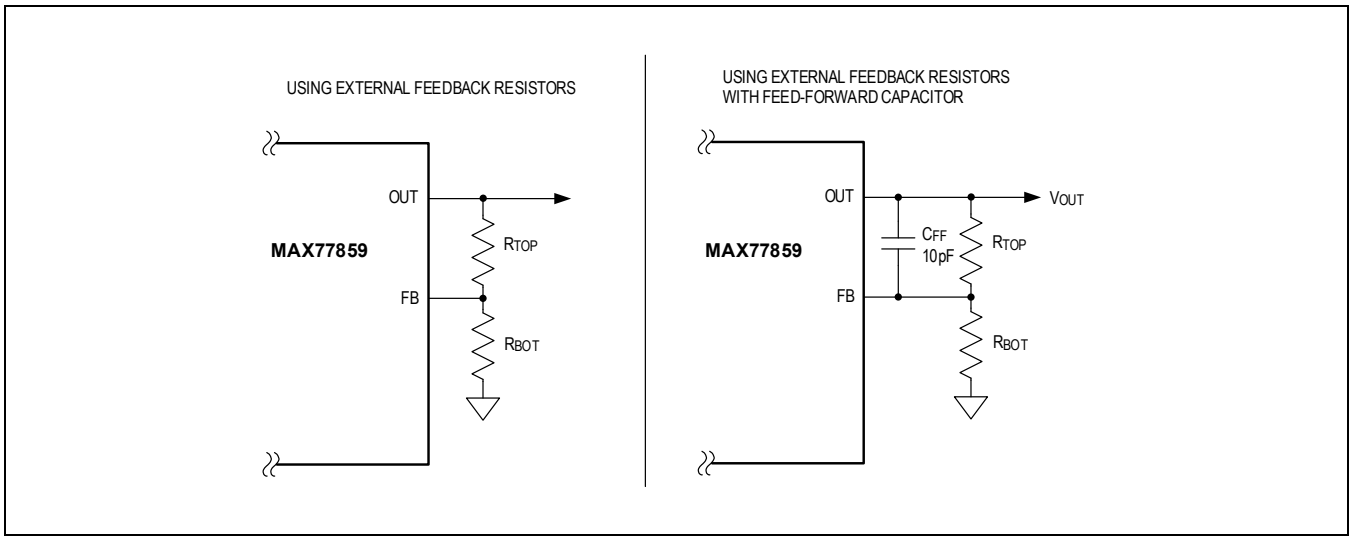


Figure 4. Connecting External Feedback Resistors to MAX77859

With a default V_{REF} of 0.30518V, *Table 1* lists the recommended external feedback resistor values (in the E192 series) for standard startup output voltages.

Table 1. Feedback Resistor Value Recommendations

DEFAULT V_{REF} (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	STARTUP V_{OUT} (V)	PROGRAMMABLE V_{OUT} RANGE (V)	V_{OUT} STEP SIZE (mV)
0.30518	205	23.2	3	3.0 to 9.61	12
	162	16.5	3.3	3.0 to 10.56	13.2
	Internal Feedback Resistors		5	3.2 to 16	20
	160	5.62	9	5.76 to 20	36
	182	4.75	12	7.68 to 20	48
	180	3.74	15	9.6 to 20	60
	330	5.11	20	12.81 to 20	80

Dynamic Voltage Scaling (DVS)

V_{OUT} is dynamically adjustable by programming V_{REF} through I^2C serial interface. The bitfield VREF[9:0] sets the V_{REF}. V_{REF} ranges between 0.19531V and 0.97656V in 1.22mV steps. When using internal feedback resistors, V_{OUT} ranges between 3.2V and 16V in 20mV steps, and it can be calculated with the following equation:

$$V_{OUT} = V_{REF} \times 16.4$$

When using external feedback resistors, the V_{OUT} range, and step size vary based on the external feedback resistor values. The V_{OUT} step size can be calculated with the following equation:

$$V_{OUT\_STEP} = \left(\frac{1.22mV}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP})$$

To calculate the V_{OUT} range, use the following equation and plug in the minimum V_{REF} of 0.19531V and maximum V_{REF} of 0.97656V:

$$V_{OUT} = \left(\frac{V_{REF}}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP})$$

Do NOT set V_{OUT} higher than the maximum output voltage of 20V or risk damaging the IC.

The bitfield VREF[9:0] is split into VREF_U[1:0] and VREF_L[7:0] in the register, in which VREF_U[1:0] represents the upper 2 bits and VREF_L[7:0] represents the lower 8 bits. After updating VREF[9:0], write 1 to DVS_STR[0] bitfield to initiate DVS and apply the new V_{REF} setting. This bit self-clears after DVS is done or if there is no change to VREF[9:0].

The bitfield SLEW_RATE[1:0] sets the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$) with a default value of 1mV/µs. The actual V_{OUT} DVS ramp rate ($\Delta V_{OUT}/\Delta t$) can be calculated from the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$) using the above equations for external feedback resistors. For example, if using internal feedback resistors, the default $\Delta V_{REF}/\Delta t$ of 1mV/µs corresponds to the $\Delta V_{OUT}/\Delta t$ of 16.4mV/µs.

SEL Pin Configuration

The SEL pin allows a single resistor (R_{SEL}) connecting the SEL pin to AGND to configure the high-side switching current limit threshold (I_{LIM}), I^2C serial interface target address, and the use of internal or external feedback resistors. Resistors with 1% tolerance (or better) should be used for R_{SEL}. *Table 2* shows nominal R_{SEL} values with corresponding settings.

Table 2. MAX77859 R_{SEL} Selection Table

R_{SEL} (Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C TARGET ADDRESS (7-BIT)	R_{SEL} (Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C TARGET ADDRESS (7-BIT)
SHORT TO GND	Internal Feedback Resistors	7.8	110 0110 (0x66)	3740	External Feedback Resistors	7.8	110 0110 (0x66)
200			110 0111 (0x67)	8060			110 0111 (0x67)
309			110 1110 (0x6E)	12400			110 1110 (0x6E)
422			110 1111 (0x6F)	16900			110 1111 (0x6F)
536		5.8	110 0110 (0x66)	21500		5.8	110 0110 (0x66)
649			110 0111 (0x67)	26100			110 0111 (0x67)
768			110 1110 (0x6E)	30900			110 1110 (0x6E)
909			110 1111 (0x6F)	36500			110 1111 (0x6F)
1050		3.8	110 0110 (0x66)	42200		3.8	110 0110 (0x66)
1210			110 0111 (0x67)	48700			110 0111 (0x67)
1400			110 1110 (0x6E)	56200			110 1110 (0x6E)
1620			110 1111 (0x6F)	64900			110 1111 (0x6F)
1870		2.0	110 0110 (0x66)	75000		2.0	110 0110 (0x66)
2150			110 0111 (0x67)	86600			110 0111 (0x67)
2490			110 1110 (0x6E)	100000			110 1110 (0x6E)
2870			110 1111 (0x6F)	OPEN			110 1111 (0x6F)

Internal Compensation Options

For designs looking to optimize its performance, COMP[2:0] bitfield for internal compensation adjustment is available through I^2C serial interface. For those systems that do not utilize I^2C serial interface, stability can still be optimized by adjusting output capacitance. In general, performance can be further optimized by lowering COMP[2:0] bitfield value or by adding additional output capacitance.

Power-OK (POK) and Fault Status/Interrupts

The IC features Power-OK (POK) comparator to monitor the regulation status of Buck-Boost output and fault status/interrupts to signal any hazardous states. The POK and fault status bits in register 0x10 (STATS) reflect the status of the IC in real-time, while the individual interrupt bit in register 0x11 (INT) is triggered and latched once the corresponding fault state occurs, and they are cleared on read.

The POK monitor continuously updates based on the actual V_{OUT} level while the buck-boost regulator is enabled. The POK bit is 0 when V_{OUT} falls below 85% (typical) of the target voltage, and it is 1 when V_{OUT} rises above 93% (typical) of the target voltage. During a soft-start or DVS event, the POK monitor update is temporarily disabled, and the POK bit holds the value before the soft-start or DVS event. POK monitor update resumes after soft-start or DVS finishes.

The IC includes several fault event monitors. Any of the following fault events asserts the corresponding bits in STATS and INT registers.

- HARDSHORT: See *Switching Current Overcurrent Protection (SW OCP)* section
- THS: See *Thermal Shutdown (THS)* section
- OCP: See *Switching Current Overcurrent Protection (SW OCP)* section

The fault interrupt bits can be masked off by writing 1 to the corresponding mask bitfield in register 0x12 (MASK). For example, when the THM_M bitfield in the MASK register is 1, the THM_I bitfield in the INT register will not be set when thermal shutdown even occurs.

The IC also features an active-low, open-drain POKB/INTB digital output pin. Connect POKB/INTB pin with a 15kΩ pullup resistor to V_{IO}. This pin can be configured as either a POK pin or a fault interrupt pin, selectable by POKBINTB[0] bit in register 0x14 (REG_CONT2).

- POKBINTB[0] = 0: POK pin (POKB).
- POKBINTB[0] = 1: Fault interrupt pin (INTB).

When the pin is configured as a POK pin, the digital output signal on POKB/INTB pin is logical NOT of the POK bit in register 0x10 (STATS), i.e., the pin is logic LOW when V_{OUT} is above the POK threshold. *Table 3* shows the truth table of the POKB/INTB pin when the pin is configured as a POK pin.

Table 3. POKB/INTB Pin Truth Table (POKBINTB = 0b0)

V_{OUT} CONDITION	POK BIT	POKB/INTB PIN
V_{OUT} < POK threshold	0	HIGH
V_{OUT} > POK threshold	1	LOW

When the pin is configured as fault interrupt pin, the signal on POKB/INTB pin is logical NOR of all unmasked bits in the register 0x11 (INT), i.e., the pin is logic LOW when there is an unmasked fault interrupt event. *Table 4* shows the truth table of POKB/INTB pin when the pin is configured as fault interrupt pin, with all interrupt bits unmasked (MASK = 0x00).

Table 4. POKB/INTB Pin Truth Table (POKBINTB = 0b1)

HARDSHORT	THS	OCP	POKB/INTB PIN
0	0	0	HIGH
1	X	X	LOW
X	1	X	LOW
X	X	1	LOW

**With all fault interrupt bits unmasked (MASK = 0x00)*

Protection Features

Undervoltage Lockout (UVLO)

The IC's undervoltage lockout feature prevents operation in abnormal input conditions when input voltage V_{IN} falls below IN UVLO falling threshold (V_{UVLO_F}) or when V_{IO} voltage (V_{VIO}) falls below V_{IO} valid falling threshold ($V_{VIO\_VALID\_F}$). Regardless of EN pin status, the IC becomes disabled, and all registers reset until V_{IN} rises above IN UVLO rising threshold (V_{UVLO_R}) and V_{IO} rises above V_{IO} valid rising threshold ($V_{VIO\_VALID\_R}$).

Switching Current Overcurrent Protection (SW OCP)

The IC features a robust switching current limit scheme that protects the IC and inductor during overload and fast transient conditions. The switching current sensing circuit takes current information from the high-side MOSFETs to determine the peak switching current ($R_{DS(ON)}$ x I_L).

The IC provides eight different cycle-by-cycle switching current limit thresholds (I_{LIM}) for the high-side MOSFET to support different output current levels. The bitfield ILIM[2:0] or R_{SEL} resistor value sets the I_{LIM}. Note that while all eight options are programmable through I^2C serial interface, only four options are selectable through R_{SEL}. When the I_{LIM} setting from I^2C serial interface and the one from R_{SEL} differ, the I^2C setting has priority over R_{SEL}.

When the inductor current (I_L) reaches the programmed peak current limit level (I_{LIM}), the IC enters the OCP state and sets OCP[0] status bit. The inductor charging phase terminates, and the discharging phase (Φ3) begins for the rest of the switching period. The charging phase begins again at the next clock cycle. OCP[0] status bit self-clears when the inductor current is no longer reaching I_{LIM}.

If V_{OUT} drops below 70% of the target, then the IC enters a HARD-SHORT state and sets HARDSHORT[0] status bit. Similar to the OCP state, the inductor charging phase terminates, and the discharging phase (Φ3) begins. But unlike the OCP state, the discharging phase does not terminate until the inductor current has dropped below the valley current limit threshold (I_{LIM_VALLEY}), and then the inductor charging phase follows. As a result, the effective switching frequency in the HARD-SHORT state differs from the normal switching frequency set in FREQ[1:0] register bitfield. See *Table 5* for available I_{LIM} options and their corresponding I_{LIM_VALLEY} values. HARDSHORT[0] status bit self-clears when V_{OUT} is no longer below 70% of the target.

Table 5. MAX77859 Switching Current Limit Options

ILIM[2:0] BITFIELD VALUE	PEAK CURRENT LIMIT (I_{LIM})	VALLEY CURRENT LIMIT (I_{LIM_VALLEY})	SOFT-START CURRENT LIMIT (I_{LIM_SS})	SKIP MODE CURRENT LIMIT (I_{LIM_SKIP})
000 (0x0)	7.8A	3.8A	3.8A	1.2A
001 (0x1)	6.8A			
010 (0x2)	5.8A	2.73A		
011 (0x3)	4.8A			
100 (0x4)	3.8A	1.5A		
101 (0x5)	2.8A		2.8A	
110 (0x6)	2.0A	0.35A	2.0A	
111 (0x7)	1.2A		1.2A	

The IC also includes a 210µs hard-short timer to latch off the buck-boost regulator in the HARD-SHORT state. When this timer expires after 210µs (e.g., when V_{OUT} has dropped below the 70% of target continuously for 210µs), the IC latches off the buck-boost regulator and sets OCP_I[0], and HARDSHORT_I[0] interrupt bits. *Figure 5* depicts the behavior during OCP and HARD-SHORT states. See the *Immediate Latch-Off Conditions* section for information about latch-off. The timer resets if the hard-short event recovers before the latch-off.

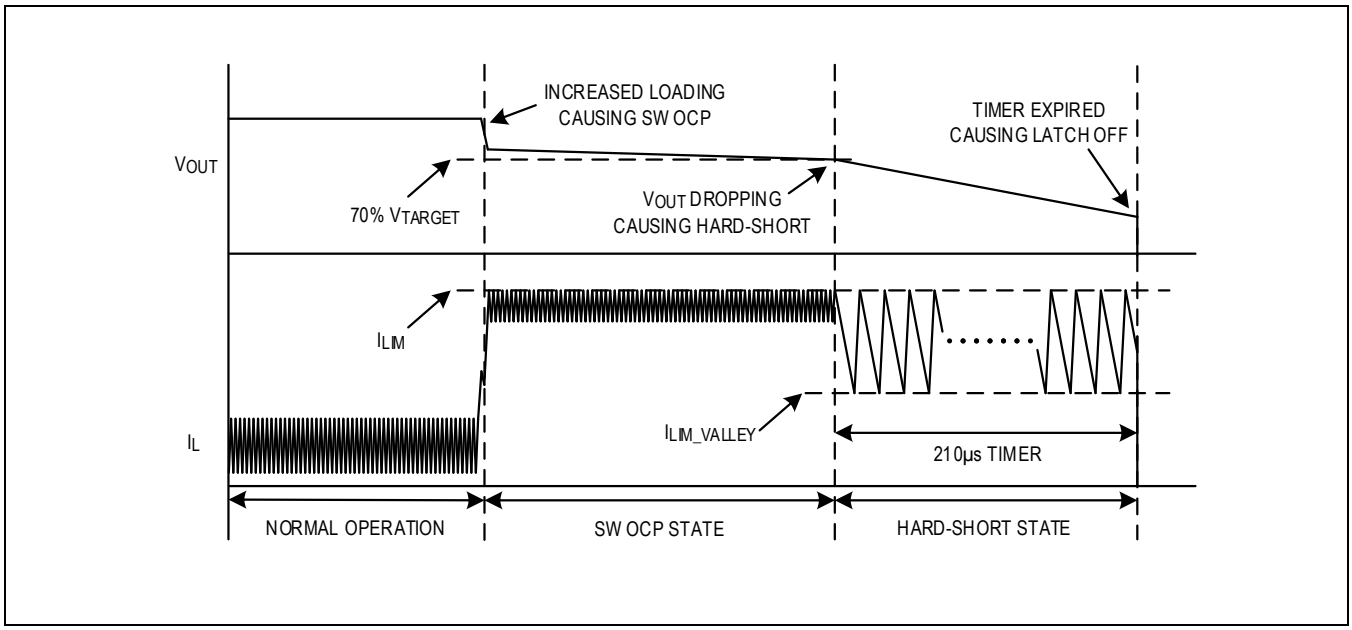


Figure 5. Switching Current Overcurrent and Output Hard-Short Behavior

Output Current Overcurrent Protection (OUT OCP, MAX77859A Only)

MAX77859A features adjustable output current limit through I²C serial interface. The IC senses the output current through an external sense resistor (10mΩ recommended). Connect the IC side of the current sense resistor directly to the SRP pin and the load side of the current sense resistor to the SRN pin. A low-pass filter can be added to the sense network to improve accuracy in boost mode and buck-boost mode operation. *Figure 6* shows the sense resistor's connection to the IC.

When the output current reaches the programmed threshold level, the regulator disables high-side MOSFETs and discharges the inductor through low-side MOSFETs. As a result, the output current is clamped at the I_{OUT_LIM} level. I_{OUT_LIM} level can be adjusted by programming IOUTLIM[6:0] bitfield. Available output current limit (I_{OUT_LIM}) options range from 1A to 5A with 50mA resolution, with a default value at 3A for a 10mΩ current sense resistor. See *Register Map* for more information.

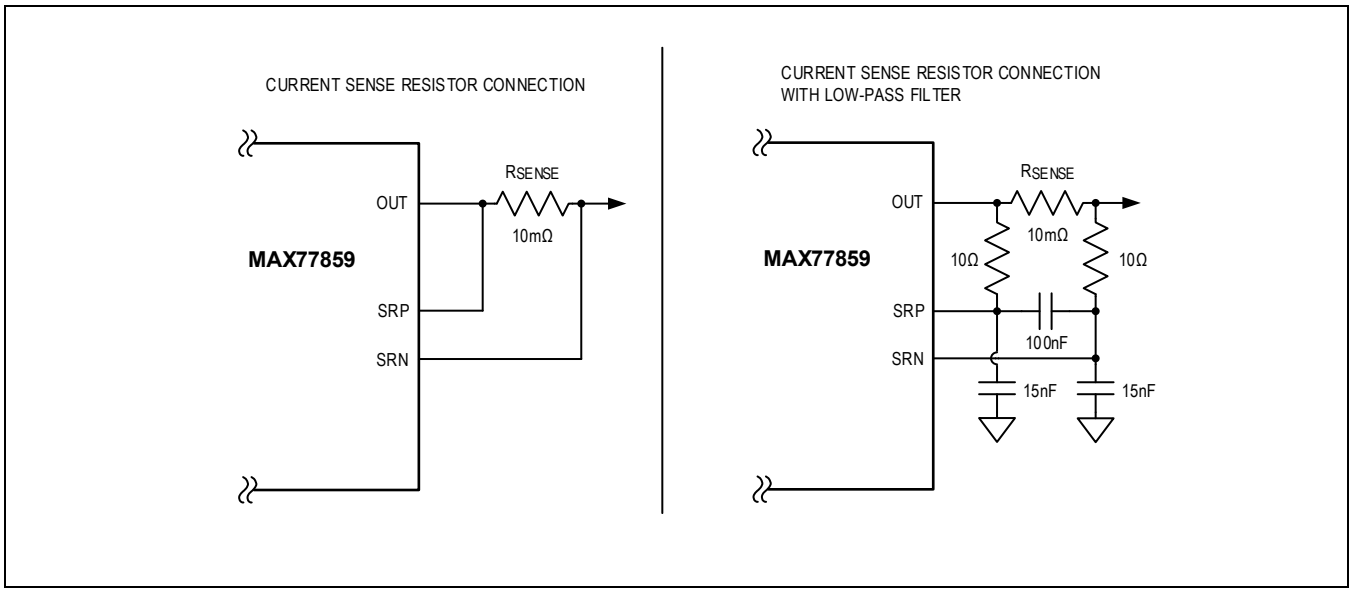


Figure 6. Connecting Output Current Sense Resistor (and with Low-Pass Filter) to MAX77859A

Thermal Shutdown (THS)

The IC contains an internal thermal protection circuit that monitors die temperature. The IC enters thermal shutdown (THS) when junction temperature (T_J) exceeds the thermal shutdown rising threshold (T_{SHDN_R}, 150°C typical). In THS, the IC is latched off and THS[0] status, and THS_I[0] interrupt bits are set. Unlike other latch-off events, output active discharge is not activated. THS[0] status bit self-clears when the temperature falls below thermal shutdown hysteresis (T_{SHDN_HYS}, 15ºC typical). Power cycling EN pin or IN pin is required for Buck-Boost output to recover from thermal shutdown. See the *Immediate Latch-Off Conditions* section for more information.

Detailed Description – I²C Serial Interface

General Description

The I²C-compatible 2-wire serial interface is used for setting output voltage and other functions. See *Register Map* for available settings.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-controller bus. The maximum number of devices that can be attached to the bus is only limited by bus capacitance.

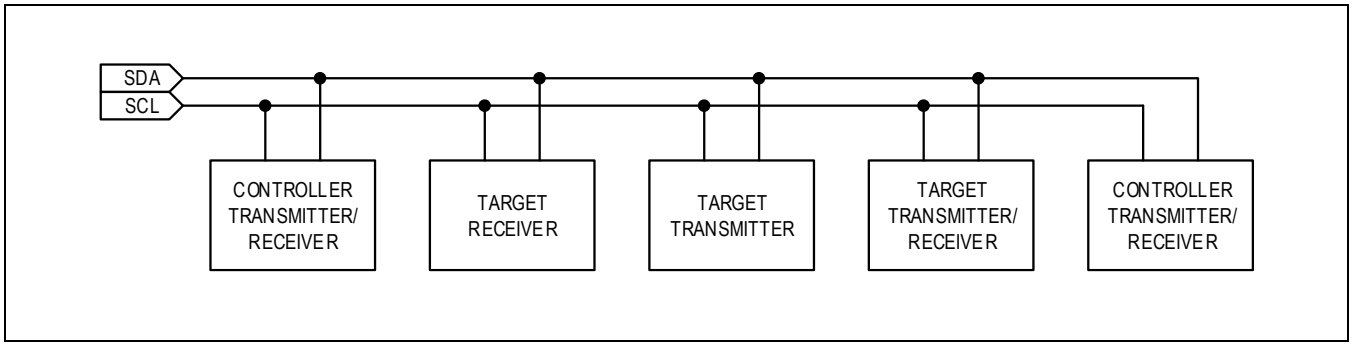


Figure 7. Functional Logic Diagram for the Communications Controller

Figure 7 shows an example of a typical I²C bus system. A device on the I²C bus that sends data to the bus is called a “transmitter.” A device that receives data from the bus is called a "receiver.” A device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a “controller.” Any device being addressed by the controller is called a “target”. The MAX77859 is a target on the I²C bus and can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on the SDA must remain stable during the HIGH portion of the SCL clock pulse. Changes in the SDA, while the SCL is HIGH, are control signals (START and STOP conditions).

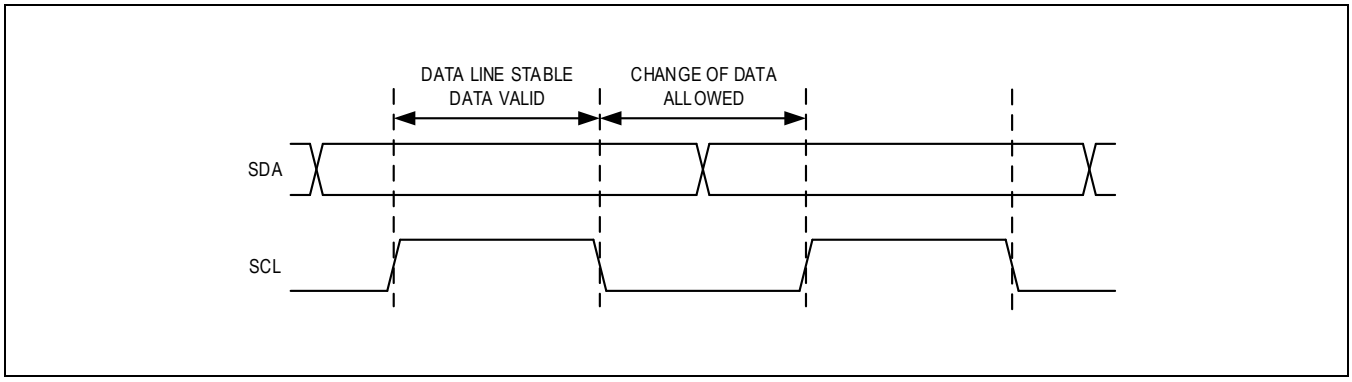


Figure 8. I²C Bit Transfer

START and STOP Conditions

When the I²C serial interface is inactive, the SDA and SCL idle HIGH. A controller device initiates communication by issuing a START condition (S). A START condition (S) is a HIGH-to-LOW transition on the SDA while, the SCL is HIGH. A STOP condition (P) is a LOW-to-HIGH transition on the SDA while, the SCL is HIGH.

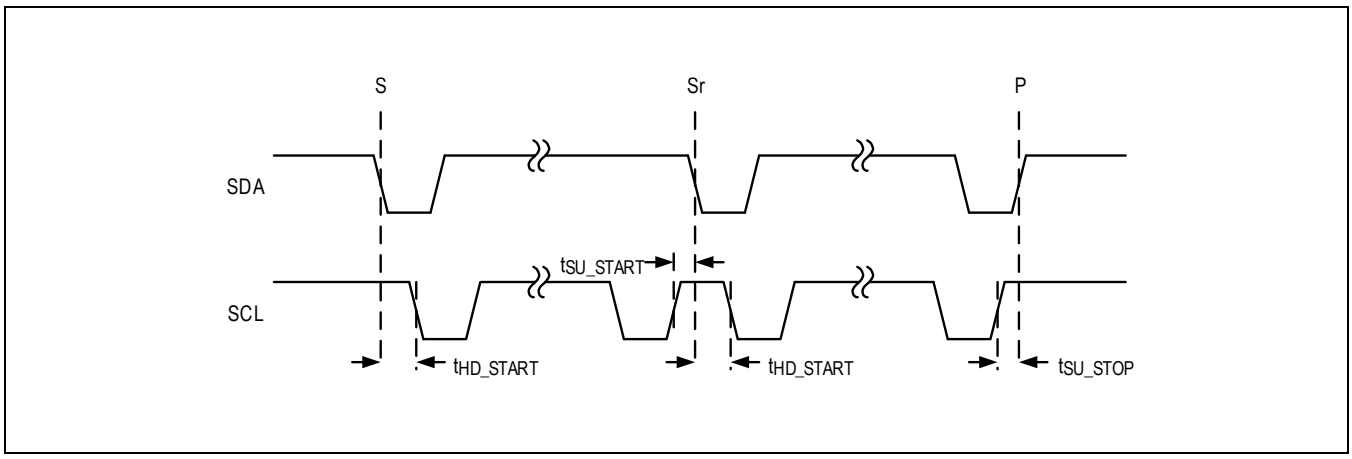


Figure 9. START and STOP Conditions

A START condition (S) from the controller device signals the beginning of a transmission. The controller terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

A STOP condition (P) frees the bus. To issue a series of commands to the target, the controller can issue REPEATED START (Sr) commands instead of a STOP condition (P) to maintain control of the bus. Generally, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or incorrect address is detected, the MAX77859 internally disconnects the SCL from the I2C serial interface until the next START condition (S), minimizing digital noise and feed-through.

Acknowledge Bit

Both the I2C bus controller device and target devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH portion of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows the SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and leaves it HIGH during the HIGH portion of the clock pulse.

Monitoring the acknowledged bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or has a system fault. In case of an unsuccessful data transfer, the bus controller should reattempt communication later.

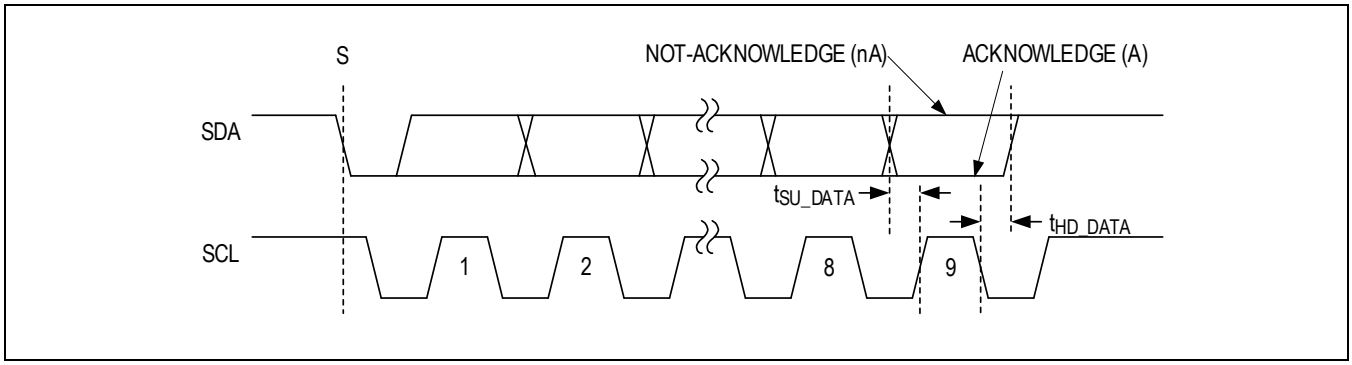


Figure 10. Acknowledge Bit

Target Address

Table 6 shows the available I²C target addresses of the MAX77859. The MAX77859 supports up to four different target addresses through R_{SEL} programming for when multiple devices in the same I²C bus line need to be used or when there is a conflict between the target addresses in the system. See Table 2 for available R_{SEL} values and the corresponding I²C target addresses.

Table 6. MAX77859 I²C Target Addresses

7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
110 0110 (0x66)	1100 1100 (0xCC)	1100 1101 (0xCD)
110 0111 (0x67)	1100 1110 (0xCE)	1100 1111 (0xCF)
110 1110 (0x6E)	1101 1100 (0xDC)	1101 1101 (0xDD)
110 1111 (0x6F)	1101 1110 (0xDE)	1101 1111 (0xDF)

Figure 11 shows the 7-bit target address at 0x66.

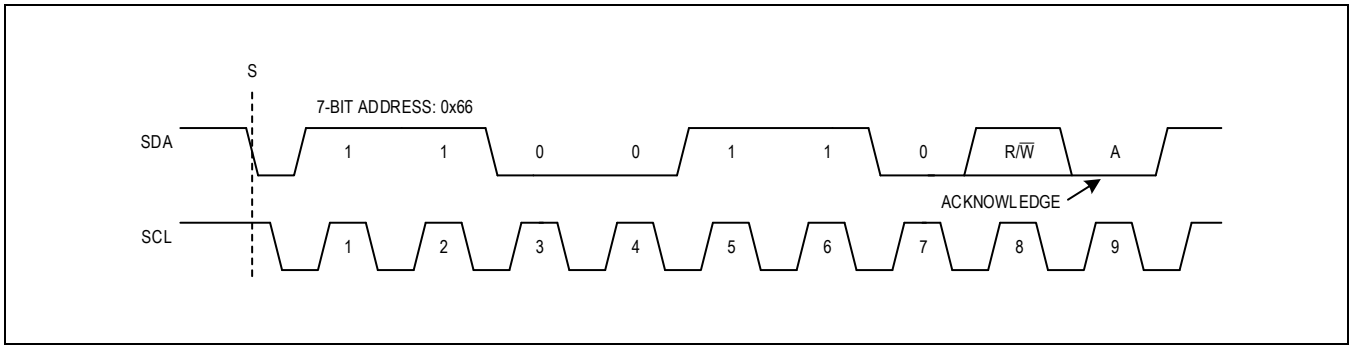


Figure 11. Target Address Byte Example

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The MAX77859 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77859 does not implement the I²C specification "General Call Address." The MAX77859 does not issue an ACKNOWLEDGE (A) if it detects the "General Call Address" (0000 0000).

Communication Speed

The MAX77859 supports the following communication speeds outlined in the I²C revision 3.0 specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pull-up resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing the bus speed, the pull-up resistance must be decreased to maintain a reasonable time constant. Refer to the *Pull-up Resistor Sizing* section of the I²C revision 3.0 specification for detailed guidance on the pull-up resistor selection. In general, for a bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a

400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pull-up resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the complete list of considerations, refer to the I^2C revision 3.0 specification. The major considerations for the MAX77859 are as follows:

- Controller device shall use current source pullups to shorten the signal rise times.
- Target device must use different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed controller code.

At power-up and after each STOP condition (P), the MAX77859 inputs filters that are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the protocol described in Engage in High-Speed Mode section.

Communication Protocals

The MAX77859 supports both writing to and reading from its registers.

Writing to a Single Register

Figure 12 shows the protocol for writing to a single register. This protocol is the same as the “Write Byte” protocol in the SMBus specification.

The “Write Byte” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The addressed target acknowledges the register pointer.
6. The controller sends a data byte.
7. The addressed target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register, and the data becomes active.
8. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

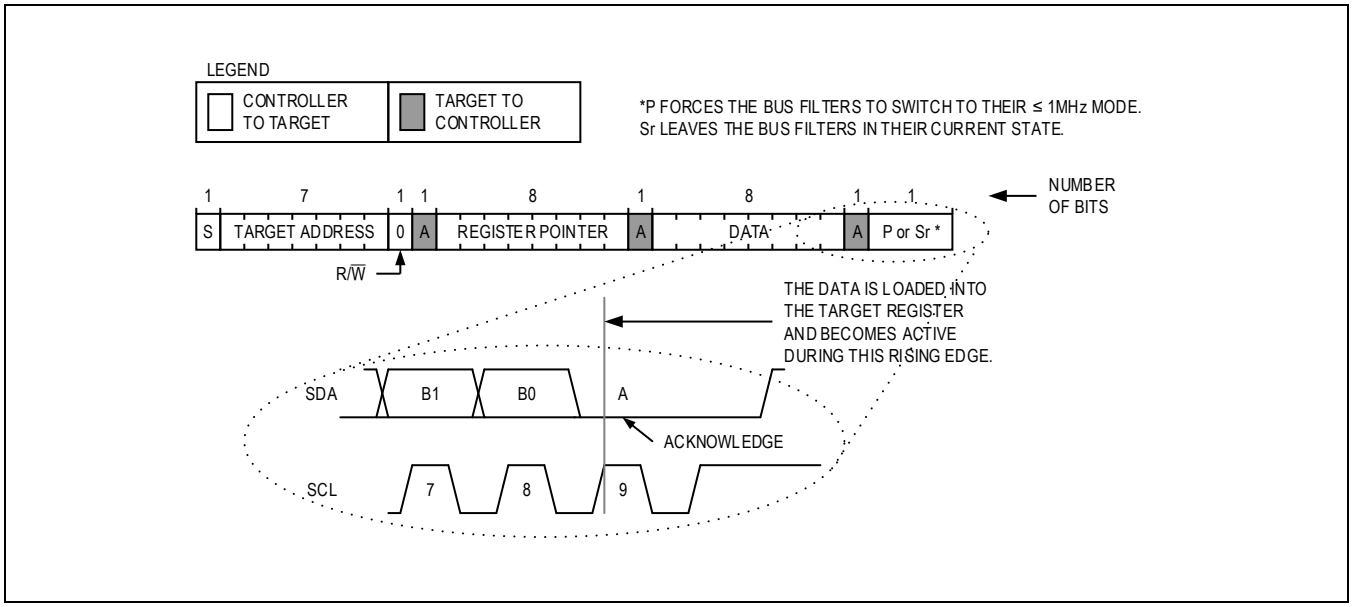


Figure 12. Writing to a Single Register

Writing to Sequential Registers

Figure 13 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the controller device continues to write after the target device receives the first byte of data. When the controller is done writing data, it issues a STOP condition (P) or REPEATED START condition (Sr).

The “Writing to Sequential Registers” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The addressed target acknowledges the register pointer.
6. The controller sends a data byte.
7. The addressed target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register, and the data becomes active.
8. Steps 6 to 7 are repeated as often as the controller requires.
9. During the last acknowledge-related clock pulse, the target issues an ACKNOWLEDGE (A).
10. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

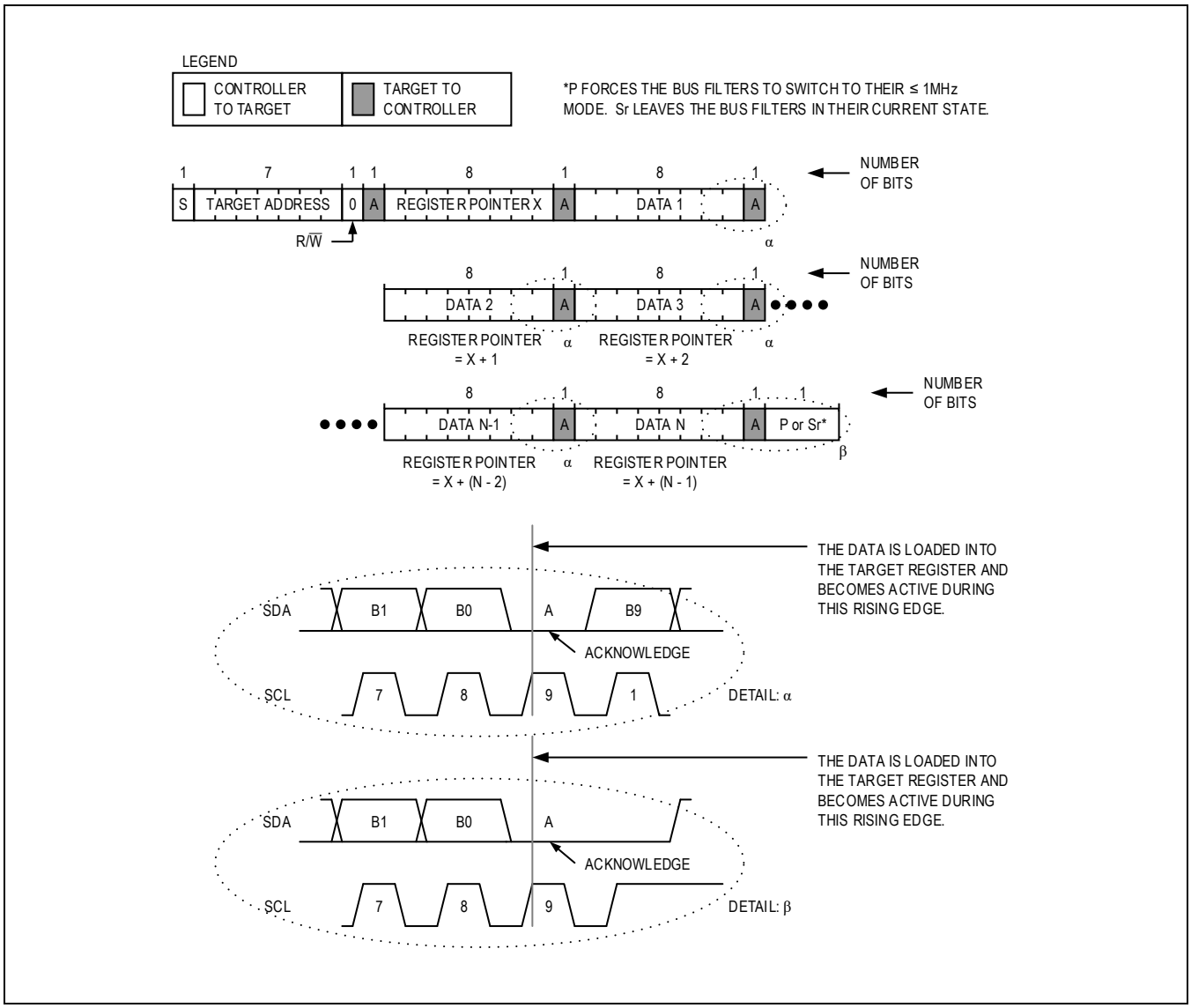


Figure 13. Writing to Sequential Registers

Reading from a Single Register

Figure 14 shows the protocol for reading from a single register. This protocol is identical to the “Read Byte” protocol in the SMBus specification.

The “Read Byte” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The addressed target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (A) by pulling SDA LOW
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.
10. The controller issues a NOT-ACKNOWLEDGE (nA).

11. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

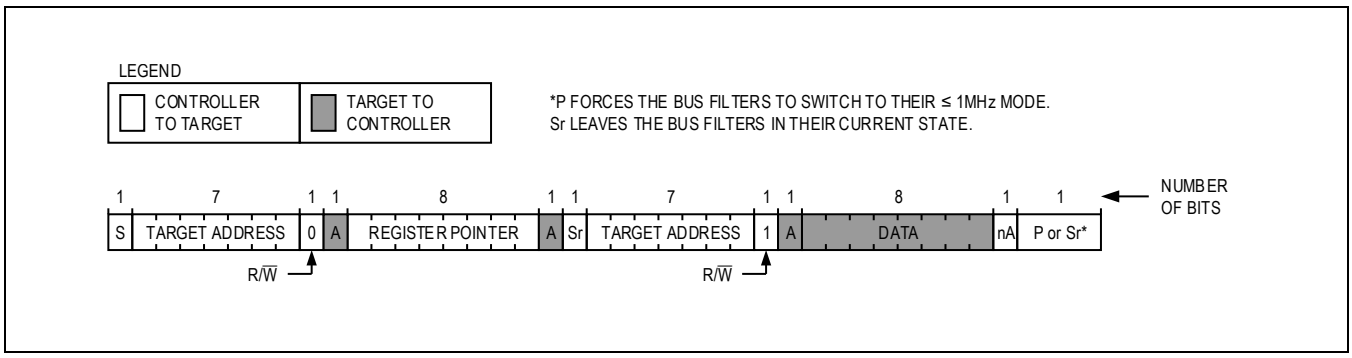


Figure 14. Reading from a Single Register

Reading from Sequential Registers

Figure 15 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol, except the controller device issues an ACKNOWLEDGE (A) to signal that the target device wants more data. When the controller device has all the required data, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit ($R/\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The addressed target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit ($R/\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.
10. The controller issues an ACKNOWLEDGE (A), signaling the target that it wishes to receive more data.
11. Step 9 to step 10 are repeated as often as the controller requires. Following the last byte of data, the controller must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

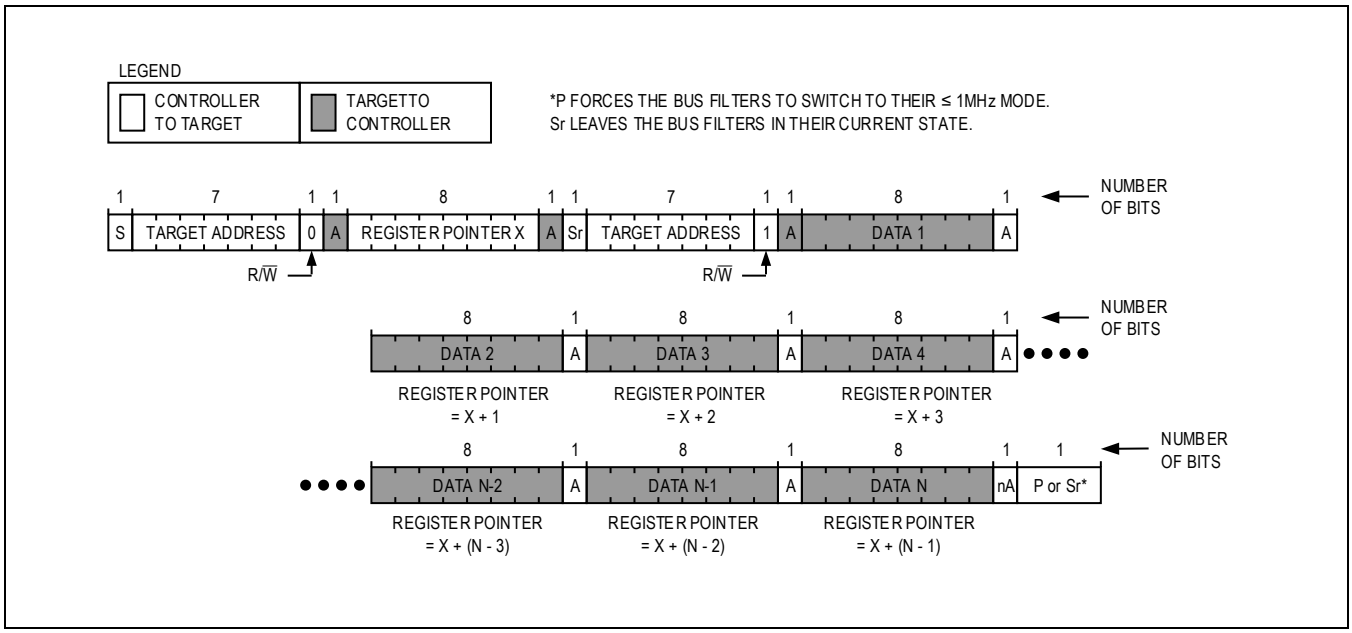


Figure 15. Reading from Sequential Registers

Engage in High-Speed

Figure 16 shows the protocol for engaging in high-speed mode operation, which allows the bus to operate at speeds up to 3.4MHz.

The protocol to engage in high-speed mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The controller sends a START condition (S).
3. The controller sends the 8-bit controller code 0000 1xx0, where ‘xx’ are don’t care bits.
4. The addressed target issues a NOT-ACKNOWLEDGE (nA).
5. The controller can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The controller can continue to issue high-speed read/write operations until a STOP condition (P) is issued. Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation.

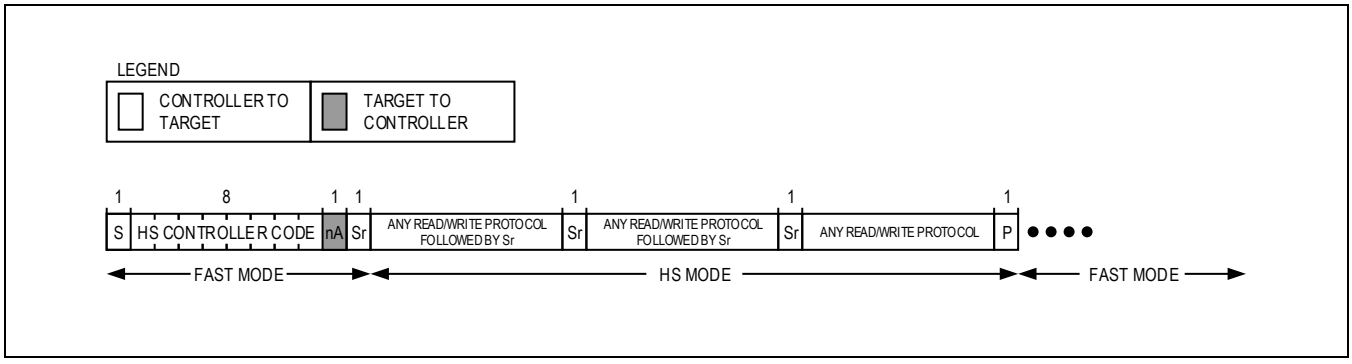


Figure 16. Engage in High-Speed Mode

High-Speed Mode Extension

The MAX77859 supports the high-speed mode extension feature. This feature keeps the IC in high-speed mode operation even after receiving a STOP condition (P). This eliminates the need for the controller device to re-issue the command for engaging in high-speed mode when the controller device wants to stay in the high-speed mode for multiple read/write cycles.

Figure 17 shows the I2C mode transition state diagram. Write 1 to the HS_EXT[0] bitfield to enable the high-speed mode extension when the MAX77859 is in low-speed mode. Enabling the high-speed mode extension when the MAX77859 is in high-speed mode is not supported.

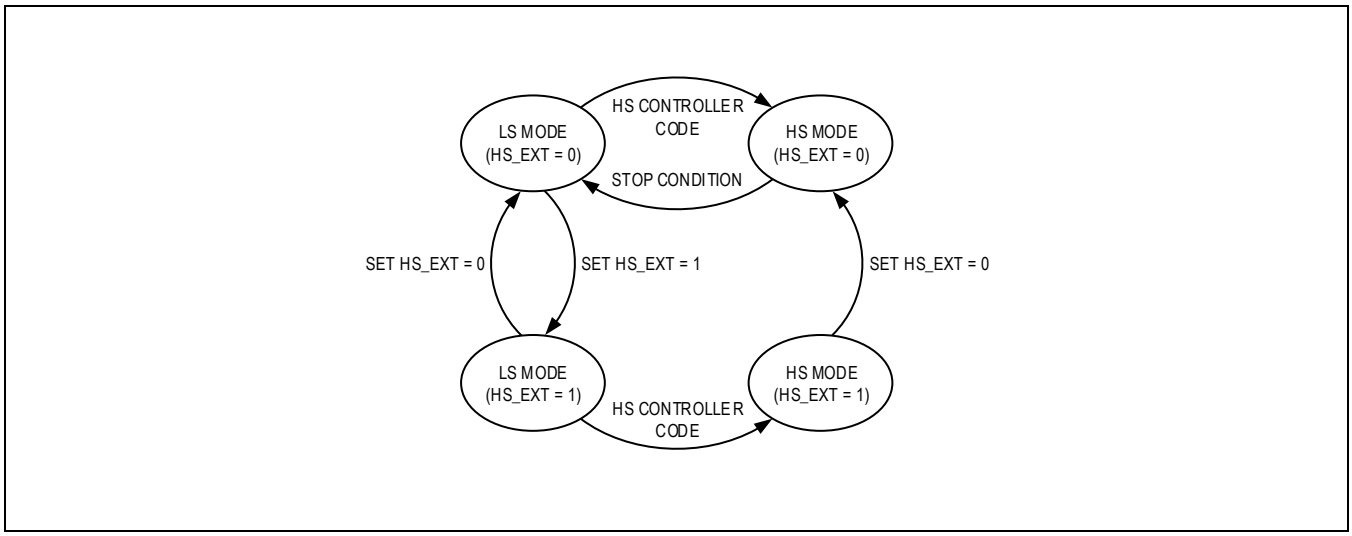


Figure 17. I2C Operating Mode State Diagram

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x10	STATS[7:0]	RSVD[2:0]			POK	RSVD	HARDSHORT	THS	OCP
0x11	INT[7:0]	RSVD[3:0]				RSVD	HARDSHORT_I	THS_I	OCP_I
0x12	MASK[7:0]	RSVD[3:0]				RSVD	HARDSHORT_M	THS_M	OCP_M
0x13	REG_CONT1[7:0]	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
0x14	REG_CONT2[7:0]	RSVD[3:0]				POKBINTB	FPWM	SLEW_RATE[1:0]	
0x15	REG_CONT3[7:0]	RSVD[4:0]					DVS_STR	VREF_U[1:0]	
0x16	REG_CONT4[7:0]	VREF_L[7:0]							
0x17	REG_CONT5[7:0]	RSVD	IOUTLIM[6:0]						
0x18	I²C_CNFG[7:0]	RSVD[6:0]							HS_EXT

Register Details

STATS (0x10)

POK and Fault Status Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			POK	RSVD	HARDSHORT	THS	OCP
Reset	0b000			0b0	0b0	0b0	0b0	0b0
Access Type	Read Only			Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:5	Reserved. Reads back 0.	N/A
POK	4	Power-OK Status	0: Output voltage is below POK threshold 1: Output voltage is above POK threshold This status bit indicate instantaneous value.
RSVD	3	Reserved	N/A

BITFIELD	BITS	DESCRIPTION	DECODE
HARDSHORT	2	Ouput Hard Short Status	0: Output voltage is above hard short threshold 1: Output voltage is below hard short threshold This status bit indicates instantaneous value.
THS	1	Thermal Shutdown Status	0: Die temperature is below thermal shutdown threshold 1: Die temperature is above thermal shutdown threshold This status bit indicates instantaneous value.
OCP	0	Overcurrent Protection Status	0: Switching current is below switching current limit 1: Switching current is triggering switching current limit This status bit indicates instantaneous value.

INT (0x11)

Fault Interrupt Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD	HARDSHORT_I	THS_I	OCP_I
Reset	0b0000				0b0	0b0	0b0	0b0
Access Type	Read Only				Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	Reserved. Reads back 0.	N/A
RSVD	3	Reserved	N/A
HARDSHORT_I	2	Ouput Hard Short Interrupt	0: Device has NOT latched off due to output hard short 1: Device has latched off due to output hard short This bit latches once triggered. Interrupt clears after read.
THS_I	1	Thermal Shutdown Interrupt	0: Device has NOT latched off due to thermal shutdown 1: Device has latched off due to thermal shutdown This bit latches once triggered. Interrupt clears after read.
OCP_I	0	Overcurrent Protection Interrupt	0: Device has NOT latched off due to overcurrent 1: Device has latched off due to overcurrent This bit latches once triggered. Interrupt clears after read.

MASK (0x12)

Fault Interrupt Mask Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD	HARDSHORT_M	THS_M	OCP_M
Reset	0b0000				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	Reserved	N/A
RSVD	3	Reserved	N/A
HARDSHORT_M	2	Ouput Hard Short Interrupt Mask	0: Ouput hard short interrupt is NOT masked (default) 1: Ouput hard short interrupt is masked
THS_M	1	Thermal Shutdown Interrupt Mask	0: Thermal shutdown interrupt is NOT masked (default) 1: Thermal shutdown interrupt is masked
OCP_M	0	Overcurrent Protection Interrupt Mask	0: Overcurrent protection interrupt is NOT masked (default) 1: Overcurrent protection interrupt is masked

REG_CONT1 (0x13)

Control Register 1

BIT	7	6	5	4	3	2	1	0
Field	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
Reset	0b010			0b10		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
COMP	7:5	Internal Compensation R_C Option (Bandwidth)	000: R_C = 30kΩ, Buck mode R_C = 20kΩ, Boost mode 001: R_C = 45kΩ, Buck mode R_C = 30kΩ, Boost mode 010: R_C = 60kΩ, Buck mode R_C = 45kΩ, Boost mode (Default) 011: R_C = 70kΩ, Buck mode R_C = 50kΩ, Boost mode 100: R_C = 80kΩ, Buck mode R_C = 55kΩ, Boost mode 101: R_C = 90kΩ, Buck mode R_C = 60kΩ, Boost mode 110: R_C = 110kΩ, Buck mode R_C = 75kΩ, Boost mode 111: R_C = 150kΩ, Buck mode R_C = 100kΩ, Boost mode
FREQ	4:3	Switching Frequency	00: 1.2MHz 01: 1.5MHz (Default) 10: 1.8MHz 11: 2.1MHz

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM	2:0	High-Side Switching Current Limit	000: 7.8A 001: 6.8A 010: 5.8A 011: 4.8A 100: 3.8A 101: 2.8A 110: 2.0A 111: 1.2A

REG_CONT2 (0x14)

Control Register 2

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				POKBINTB	FPWM	SLEW_RATE[1:0]	
Reset	0b0000				0b0	0b0	0x00	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	Reserved	N/A
POKBINTB	3	POKB/INTB Pin Configuration	0: The POKB/INTB pin is configured as a POKB pin (reflection of POK bit in STATS register) (Default) 1: The POKB/INTB pin is configured as an INTB pin (reflection of INT register)
FPWM	2	Forced-PWM Mode Control	0: Forced-PWM mode is disabled (Default) 1: Forced-PWM mode is enabled
SLEW_RATE	1:0	Internal Reference DVS Ramp Rate. See the *Output Voltage Configuration* section for equations to convert the V_{REF} DVS ramp rate to the V_{OUT} ramp rate.	00: 1.5mV/µs (FREQ = 00) 1mV/µs (FREQ = 01 or 10) 0.8mV/µs (FREQ = 11) (Default) 01: 0.5mV/µs 10: 0.25mV/µs 11: 0.125mV/µs

REG_CONT3 (0x15)

Control Register 3

BIT	7	6	5	4	3	2	1	0
Field	RSVD[4:0]					DVS_STR	VREF_U[1:0]	
Reset	0b00000					0b0	0x0	
Access Type	Write, Read					Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:3	Reserved	N/A

BITFIELD	BITS	DESCRIPTION	DECODE
DVS_STR	2	DVS Start	Initiates DVS to apply new VREF. This bit self-clears after DVS is done, or if there is no change to VREF[9:0].
VREF_U	1:0	Internal Reference Voltage Upper Bits	See VREF_L[7:0] for decode values

REG_CONT4 (0x16)

Control Register 4

BIT	7	6	5	4	3	2	1	0
Field	VREF_L[7:0]							
Reset	0xFA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VREF_L	7:0	Internal Reference Voltage Lower Bits	VREF[9:0] bitfield is a combination of VREF_U[1:0] and VREF_L[7:0], in which VREF_U[1:0] represents the upper 2 bits and VREF_L[7:0] represents the lower 8 bits. After updating VREF[9:0], write 0b1 to DVS_STR (or within the same I^2C transaction writing VREF_U[1:0]) to apply the new value. The decode of VREF[9:0] bitfield is as follows: 0x000–0x09F: 0.19531V 0x0A0–0x320: 1.22mV/LSB in a linear transfer function between 0.19531V (0x0A0) to 0.97656V (0x320) 0x321–0x3FF: 0.97656V Default: 0x0FA: 0.30518V

REG_CONT5 (0x17)

Control Register 5

BIT	7	6	5	4	3	2	1	0
Field	RSVD	IOUTLIM[6:0]						
Reset	0b0	0x3B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	N/A
IOUTLIM	6:0	Output Current Limit Threshold (MAX77859A Only)	The following decode values are based on a 10mΩ sense resistance. 0x00–0x12: 1A 0x13–0x63: 50mA/LSB in a linear transfer function between 1A (0x13) to 5A (0x63) 0x64–0x7F: 5A Default: 0x3B: 3A

I²C_CNFG (0x18)

I²C Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							HS_EXT
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:1	Reserved	N/A
HS_EXT	0	I²C High-Speed Mode Extension Control	0: I²C high-speed mode extension is disabled (Default) 1: I²C high-speed mode extension is enabled

Applications Information

Considerations for Low Output Voltage

The minimum on-time for the MAX77859 is 110ns (typical), which limits the input voltage range for low output voltage conditions. Use the equation below to calculate the maximum input voltage for a given minimum output voltage. With a bounded input voltage range, output voltages lower than 3V can be achieved. However, do not operate the device with output voltages below 2.5V.

$$V_{IN\_MAX} = V_{OUT} / (110ns \times f_{SW})$$

For example, with 2.5V output and 1.8MHz switching frequency, the maximum input voltage is 12.62V.

Considerations for Selecting Switching Frequency

The MAX77859 supports four different switching frequencies to provide options avoiding specific EMI-sensitive frequency bands and improving EMI performance. In addition, switching frequency can also impact efficiency and output voltage ripple performance. In general, the lower switching frequency option yields slightly better efficiency in PWM mode, and the higher switching frequency option results in a slightly smaller output voltage ripple in PWM mode.

For applications utilizing 3.8A or lower I_{LIM} settings, higher switching frequencies might not be suitable if the input voltage is much higher than the output voltage. Use the equation below to calculate the maximum allowable switching frequency in such an application.

$$f_{SW\_MAX} = V_{OUT} / (130ns \times V_{IN})$$

For example, with 5V output and 22V input, the calculated maximum switching frequency is 1.748MHz. Therefore, 1.8MHz and 2.1MHz settings are not suitable when utilizing 3.8A or lower I_{LIM} settings.

Software (I^2C) Control

Control the IC using software commands sent over I^2C serial interface.

Assert V_{IO} valid and connect SDA and SCL to a serial host to enable the serial bus and full software control of the IC. When using software, the serial host can accomplish the following:

- Access POK and individual fault status with POK[0], HARDSHORT[0], THS[0], and OCP[0] bitfields.
- Access individual fault interrupt with HARDSHORT_I[0], THS_I[0], and OCP_I[0] bitfields.
- Configure individual fault interrupt mask with HARDSHORT_M[0], THS_M[0], and OCP_M[0] bitfields.
- Configure POKB/INTB pin as a POK pin (POKB) or a fault interrupt pin (INTB) with POKBINTB[0] bitfield.
- Configure internal compensation option with COMP[2:0] bitfield.
- Configure switching frequency with FREQ[1:0] bitfield.
- Configure switching current limit threshold (I_{LIM}) with ILIM[2:0] bitfield.
- Configuration regulation mode (SKIP, FPWM) with the FPWM[0] bitfield.
- Configure output voltage (V_{OUT}) by setting internal reference voltage (V_{REF}) with VREF_U[1:0] and VREF_L[7:0] bitfields.
- Start V_{OUT} DVS with DVS_STR[0] bitfield.
- Configure V_{OUT} DVS slew rate with SLEW_RATE[1:0] bitfield.
- MAX77859A only: Configure output current limit threshold (I_{OUT_LIM}) with IOUTLIM[6:0] bitfield.

The configuration registers reset when V_{IO} becomes invalid, when IN falls below UVLO falling threshold (V_{UVLO_F}), or when EN is logic LOW. See *Detailed Description – I^2C Serial Interface* and *Register Map* section for more information.

Non-I^2C and Standalone Operation

The MAX77859 can operate without I^2C software control. The switching current limit can be configured by a resistor (R_{SEL}) connecting the SEL pin to AGND. The output voltage can be configured by external feedback resistors. See the *SEL Pin Configuration* section and *Output Voltage Configuration* section for more information. If the I^2C serial interface is not in use, connect both SCL and SDA pins to V_{IO} to avoid unwanted behavior. When the output current sense resistor is not in use, connect SRP and SRN pins together to avoid unwanted behavior.

Moreover, the MAX77859 is capable of standalone operation, in which the IC starts up whenever V_{IN} is valid, and it does not require a separate supply for the V_{IO} pin. This is useful for systems without a host controller, or MAX77859 is the only power supply in the system. To configure the MAX77859 for standalone operation, connect a 510kΩ from IN pin to the

EN pin. The IC clamps the voltage at the EN pin internally to ensure it does not exceed the absolute maximum rating. If the system does not have a separate supply to power V_{IO} pin, connect V_{IO} pin to V_L so V_{IO} can be supplied by the internal regulator. Connections for standalone operation are shown in *Figure 18*.

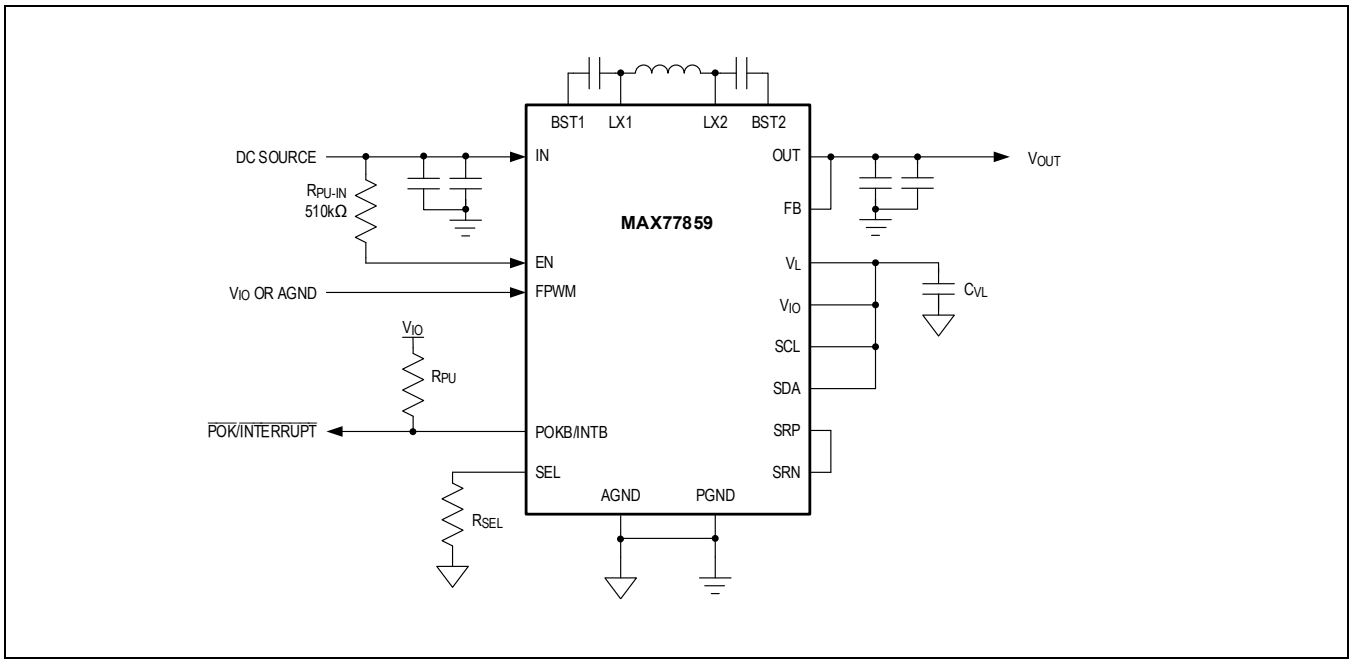


Figure 18. Connections for Standalone Operation

Inductor Selection

An inductor with a saturation current rating (I_{SAT}) greater than or equal to the typical high-side switching current limit threshold (I_{LIM}) setting is recommended. In general, inductors with lower saturation current and higher DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the RMS current rating (I_{RMS}) of the inductor (the current at which the temperature rises appreciably) based on the expected load current.

The chosen inductor value should ensure that the peak-inductor ripple current (I_{PEAK}) is below the I_{LIM} setting so that the converter can maintain regulation. A 1.5µH inductor is recommended throughout the operating range of the converter.

Table 7 lists recommended inductors.

Table 7. Inductor Recommendations

VENDOR	PART NUMBER	NOMINAL INDUCTANCE (µH)	TYPICAL DCR (mΩ)	I_{SAT} (A)	I_{RMS} (A)	DIMENSIONS L x W x H (mm)	I_{LIM} SETUP
Coilcraft	XGL5020-152MEC	1.5	11.4	8.9	12.8	5.48 x 5.28 x 2.1	ILIM[2:0] = 000 (7.80A)
Sumida	0518CDMCCDS-1R5MC	1.5	21	10.6	6.6	5.4 x 5.2 x 1.8	ILIM[2:0] = 000 (7.80A)
Bourns	SRN5020TA-1R5Y	1.5	25	4.5	3.5	5.0 x 5.0 x 2.0	ILIM[2:0] = 100 (3.80A)
Taiyo Yuden	MDMK4040T1R5MM	1.5	56	5.6	3.6	4.0 x 4.0 x 1.2	ILIM[2:0] = 100 (3.80A)

Samsung	CIGW252010GL1R5MNE	1.5	45	3.1	3.4	2.5 x 2.0 x 1.0	ILIM[2:0] = 110 (2.00A)
Murata	DFE201610E-1R5M=P2	1.5	91 (max)	2.9	2.1	2.0 x 1.6 x 1.0	ILIM[2:0] = 110 (2.00A)

Input Capacitor Selection

For most applications, bypass IN pin with two 35V 10µF nominal ceramic input capacitors (C_{IN}) that maintain 1µF or higher effective capacitance at its working voltage. Effective C_{IN} is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter but increase inrush current from voltage supply when connected. C_{IN} reduces the current peaks drawn from input power source and reduces switching noise in the system. The ESR/ESL of C_{IN} and its series PCB trace should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to the converter's switching frequency.

Pay special attention to capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{IN}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for the stable operation of the converter. Choose effective C_{OUT} to be 8.2µF minimum. Effective C_{OUT} is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. For most applications, two 25V 22µF capacitors are recommended for C_{OUT}.

Pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{OUT}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's datasheet. Refer to *Tutorial 5527* for more information.

Other Required Component Selection

Table 8 shows the requirements for other required components.

Table 8. Other Component Selection Requirements

SYMBOL	COMPONENT DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
C_{BST}	High-Side FET Driver Bootstrap Capacitor	Suggested Capacitance		0.22		µF
C_{VL}	V_L Regulator Bypass Capacitor	Effective Capacitance	0.5		3	µF
		Equivalent Series Resistance (ESR)			100	mΩ
C_{VIO}	V_{IO} Regulator Bypass Capacitor	Effective Capacitance	0.3		1.5	µF
		Equivalent Series Resistance (ESR)			100	mΩ
R_{SEL}	SEL Pin Resistor	Acceptable Tolerance	-1		+1	%
R_{PU}	POKB/INTB Pullup Resistor	Suggested Resistance		15		kΩ

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. For the WLP package, a high-density interconnect (HDI) PCB is required to route to the EN, FPWM, SEL, and SRP pins. *Figure 19* shows an example layout for the MAX77859 WLP package.

When designing the PCB, follow these guidelines:

- Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN pin and OUT pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
- Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly, and additional area creates more radiated emissions.
- Route LX nodes to their corresponding bootstrap capacitor (C_{BST}) as short as possible. Prioritize C_{BST} placement to reduce trace length to the IC.
- Connect the inner PGND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create PGND islands, as PGND islands risk interrupting the hot loops. Connect AGND and AGND island to the low-impedance ground plane on the PCB (the same net as PGND).
- Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
- When utilizing the output current sense feature (MAX77859A only), route SRP and SRN to the sense resistor in parallel, and make sure the traces are as short as possible to limit the amount of noise couple in the signal.
- Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

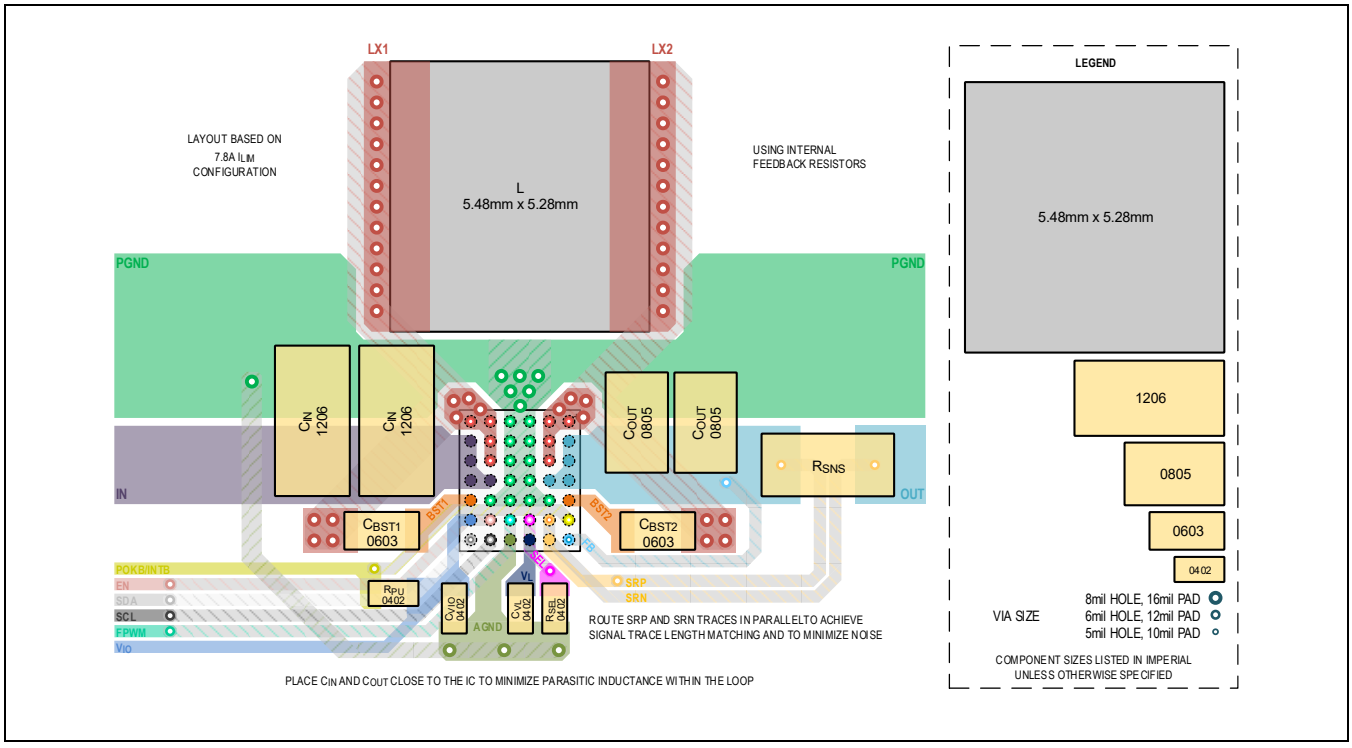
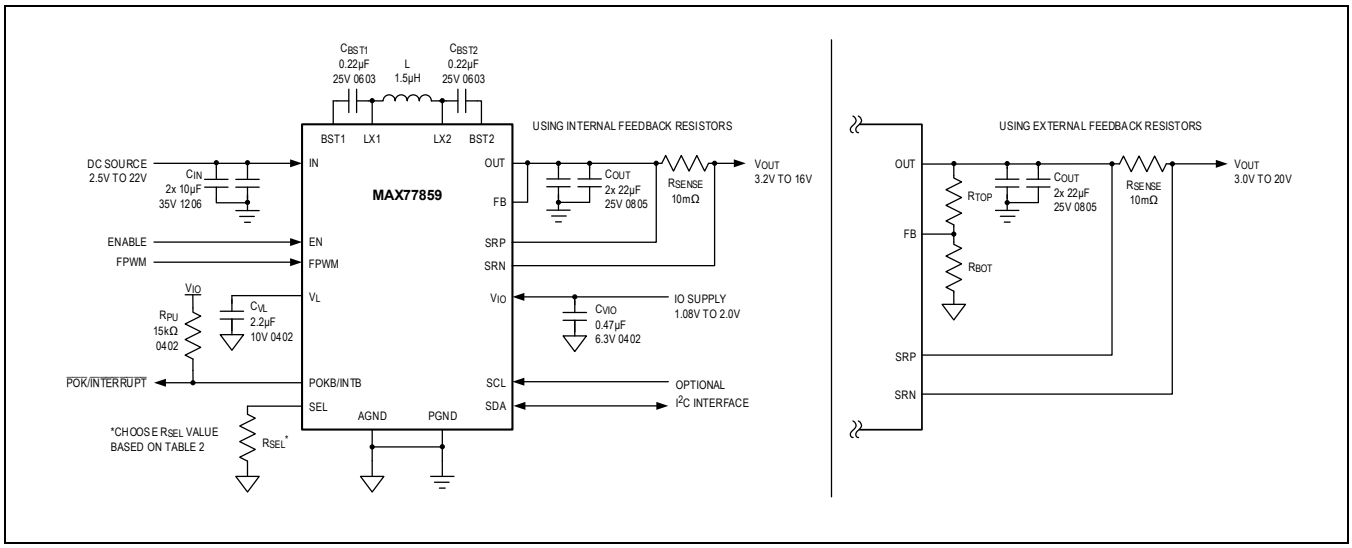


Figure 19. PCB Layout Recommendation for 42 WLP Package with 5.48mm x 5.28mm Inductor

Typical Application Circuits



Ordering Information

PART NUMBER	DEFAULT SWITHCING FREQUENCY	DEFAULT OUTPUT VOLTAGE	PPS (OUTPUT CURRENT LIMIT)	PIN-PACKAGE
MAX77859AEWO+T	1.5MHz	5V	Yes	42 WLP
MAX77859BEWO+T*			No	42 WLP
MAX77859AEFS+T*			Yes	19 FC2QFN
MAX77859BEFS+T*			No	19 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*Future product—contact factory for availability.

For other switching frequency options, please contact sales representatives for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	05/23	Release for Market Intro	—
1	05/23	Adding future product reference (*) to MAX77859BEWO+T in *Ordering Information* table.	57