Precision, 40 V, ±70 nV/°C, Low Input Bias Current, Low Offset Voltage, Low Noise, Rail-to-Rail Input/Output Operational Amplifier with Digitrim™

FEATURES

- Low offset voltage drift: ±70 nV/˚C typical
- Low offset voltage: ±5 µV typical, ±15 µV maximum
- Low voltage noise: 1 µV p-p from 0.1 Hz to 10 Hz typical
- Low voltage noise density: 5 nV/√Hz typical at f = 1 kHz
- High common-mode rejection: 144 dB typical
- Low input bias current: ±15 pA maximum
- Wide gain bandwidth product: 10 MHz typical
- High slew rate: 20 V/µs typical
- Low THD: -134 dB at f = 1 kHz
- Low quiescent current: 1.5 mA per amplifier typical
- Wide supply voltage operation: 6 V to 40 V, ±3 V to ±20 V
- Integrated EMI filter
- MUX-Compatible
  - Rail-to-rail high impedance inputs: Differential and Common-mode
  - Fast settling time
- Rail-to-rail output
- No phase reversal
- Heavy capacitive load drive capability: 1 nF
- Wide specified temperature range: -40°C to +125°C

APPLICATIONS

- Electronic test and measurements
- Data acquisition systems
- Automated Test Equipment
- Medical Instruments
- Multiplexed input signal chains
- Precision current measurement
- Photodiode amplifiers

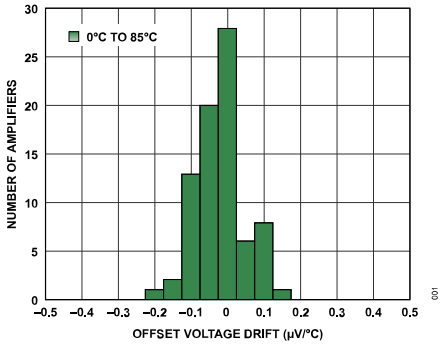

Figure 1. Ultra-Low Offset Voltage Drift for Precision Design

GENERAL DESCRIPTION

The ADA4510-2[1] is a dual, 40 V, high precision, rail-to-rail input/output operational amplifier that can be used at any point of the signal chain: sensing, conditioning, and output drive. Through the use of Analog Devices, Inc. proprietary Digitrim™ technique, the ADA4510-2 achieves best-in-class low offset drift of ±70 nV/˚C typical, ±0.5 µV/˚C maximum, and low offset voltage of ±5 µV typical, ±15 µV maximum, eliminating expensive temperature calibration costs for precision designs.

The ADA4510-2 delivers excellent DC precision and outstanding AC performance, making it a top choice for a wide variety of signal chain applications. By integrating a robust MUX-Compatible architecture, the ADA4510-2 effectively solves common system distortion and settling problems, and provides the superior accuracy required in multiplexed multi-channel precision signal chains. The ADA4510 generics are specified from −40°C to +125°C.

Table 1. Device Family Information

Part Number	Package
ADA4510-1[1]	SOT-23 (5), SOIC (8), MSOP (8)
ADA4510-2[1]	SOIC_N (8), MSOP (8)
ADA4510-4[1]	SOIC (14), TSSOP (14)

[1] Please reach out to ADA4510@analog.com for more information.

TYPICAL APPLICATION CIRCUIT

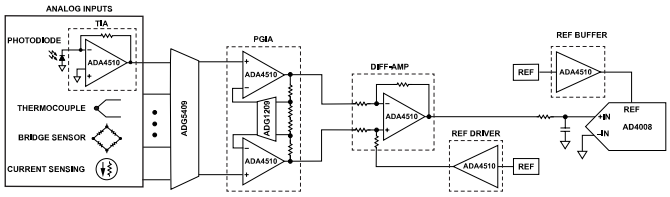

Figure 2. Multiplexed Data Acquisition Signal Chain

[1] Protected by U.S. patent number 11,329,612; other patents pending.

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SPECIFICATIONS

Supply voltage (V_{SY}) = ±3 V to ±20 V, common-mode voltage (V_{CM}) = 0 V, load resistor (R_L) = 10 kΩ to mid-supply, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±5	±15	µV
		0°C < T_A < +85°C		±7	±35	µV
		−40°C < T_A < +125°C		±20	±100	µV
		V_{CM} = (V+) − 1.5 V		TBD	TBD	µV
		0°C < T_A < +85°C			TBD	µV
		−40°C < T_A < +125°C			TBD	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
		0°C < T_A < +85°C		0.07	0.5	µV/°C
		−40°C < T_A < +125°C		0.1	0.7	µV/°C
		V_{CM} = (V+) − 1.5 V				
		0°C < T_A < +85°C		TBD	TBD	µV/°C
		−40°C < T_A < +125°C		TBD	TBD	µV/°C
Input Bias Current	I_B			2.5	15	pA
		0°C < T_A < +85°C			TBD	
		−40°C < T_A < +125°C			25	nA
Input Offset Current	I_{OS}			0.5	7	pA
		0°C < T_A < +85°C			TBD	
		−40°C < T_A < +125°C			1	nA
Input Voltage Range	IVR	Guaranteed by CMRR	V−		V+	V
Common-Mode Rejection Ratio	CMRR	V− < V_{CM} < (V+) – 3 V	TBD	144		dB
		−40°C < T_A < +125°C	TBD			dB
		V− < V_{CM} < V+	TBD	TBD		dB
		−40°C < T_A < +125°C	TBD			dB
Open-Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, (V−) + 0.3 V < V_{OUT} < (V+) − 0.3 V	TBD	140		dB
		−40°C < T_A < +125°C	TBD			dB
		R_L = 2 kΩ, (V−) + 0.9 V < V_{OUT} < (V+) − 0.9 V	TBD	126		dB
		−40°C < T_A < +125°C	TBD			dB
Input Capacitance	C_{INDM}	Differential mode		20		pF
	C_{INCM}	Common mode		2		pF
Input Resistance	R_{INDM}	Differential mode		1		TΩ
	R_{INCM}	Common mode		10		TΩ
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		1		µV p-p
		0.1 Hz to 10 Hz, V_{CM} = (V+) − 1.5 V		TBD		
Voltage Noise Density	e_N	f = 100 Hz		8.0		nV/√Hz
		f = 1 kHz		5.0		nV/√Hz
		f = 100 Hz, V_{CM} = (V+) − 1.5 V		TBD		
		f = 1 kHz, V_{CM} = (V+) − 1.5 V		TBD		
Current Noise Density	i_N	f = 10 Hz		4.0		fA/√Hz

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Swing High ((V+) - V_{OUT})	V_{OH}	R_L = 10 kΩ	TBD	70		mV
		−40°C < T_A < +125°C	TBD	110		mV
		R_L = 2 kΩ	TBD	500		mV
		−40°C < T_A < +125°C	TBD	800		mV
Output Swing Low (V_{OUT} - (V-))	V_{OL}	R_L = 10 kΩ		50	TBD	mV
		−40°C < T_A < +125°C		90	TBD	mV
		R_L = 2 kΩ		300	TBD	mV
		−40°C < T_A < +125°C		600	TBD	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < TBD V		TBD		mA
Short-Circuit Current	I_{SC}	Sourcing/sinking		55/70		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz				
		Gain = 1		19		mΩ
		Gain = 10		190		mΩ
		Gain = 100		1.9		Ω
Open-Loop Output Impedance	Z_O	f = 1 kHz to 1 MHz		190		Ω
POWER SUPPLY						
Supply Voltage ((V+) - (V-))	V_{SY}	Guaranteed by PSRR	6		40	
Power Supply Rejection Ratio	PSRR	V_{SY} = ±3 V to ±20 V	TBD	140		dB
		−40°C < T_A < +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		1.5	TBD	mA
		−40°C < T_A < +125°C			TBD	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±5 V, Gain = +1, 20% to 80%		20		V/µs
Gain Bandwidth Product	GBP	f = 100 kHz		10		MHz
−3 dB Bandwidth	−3 dB	Gain = 1		13.5		MHz
Settling Time	t_S					
To 0.01%		Gain = -1, V_{OUT} = 10 V step		1.5		µs
		Gain = -1, V_{OUT} = 5 V step		TBD		
To 0.001%		Gain = -1, V_{OUT} = 10 V step		2.1		µs
		Gain = -1, V_{OUT} = 5 V step		TBD		
Total Harmonic Distortion	THD	V_{OUT} = 10 V p-p, Gain = 1				
		1 kHz		0.00002%		
				-134		dB
		50 kHz		0.00446%		
				-87		dB
EMI REJECTION RATIO	EMIRR	EMIRR = 20 × $\log_{10}(V_{IN}/\Delta V_{OS})$, V_{IN} = 200 mV p-p				
f = 1000 MHz				67		dB
f = 2400 MHz				80		dB
CROSSTALK	X_{TALK}	V_{IN} = 4 V p-p				
		DC		165		dB
		f = 1 kHz		164		dB
		f = 100 kHz		130		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (V+ to V−)	−0.3 V to +45 V
Input Common-mode Voltage	
(+IN A, −IN A, +IN B, −IN B) to V−	−0.3 V to +45 V
(+IN A, −IN A, +IN B, −IN B) to V+	+0.3 V to −45 V
Differential Input Voltage	
+IN A to −IN A, +IN B to −IN B	±45 V
Input Current	±10 mA
Output Short Circuit Duration[1]	Thermally Limited
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Case Temperature	260°C

[1] A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

θ_{JA} is the junction to ambient, thermal resistance.

θ_{JC} is the junction to case, thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	108.5	34.12	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2017.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002-2018.

ESD Ratings for ADA4510-2

Table 5. ADA4510-2, 8-Lead SOIC_N

ESD Model	Withstand Threshold (V)	Class
HBM	TBD	1C
FICDM	TBD	TBD

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

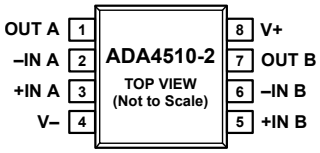

Figure 3. Pin Configuration, 8-Lead SOIC (R Suffix)

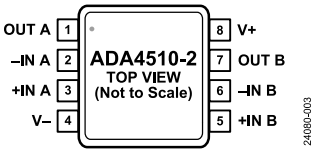

Figure 4. Pin Configuration, 8-Lead MSOP (RM Suffix)

Table 6. Pin Function Descriptions, 8-Lead SOIC and 8-Lead MSOP

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

OUTLINE DIMENSIONS

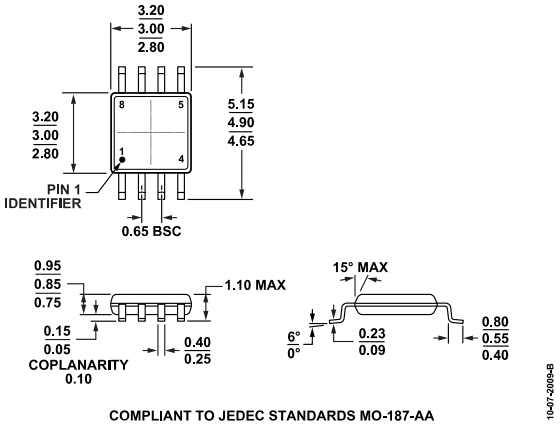

Figure 5. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

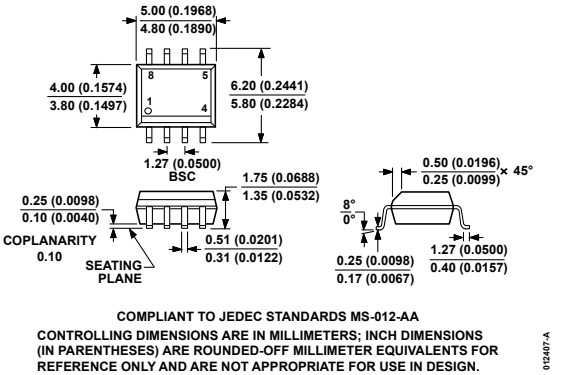

Figure 6. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions show in millimeters and (inches)